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MV1443

PCM TIMESLOT ZERO TRANSMITTER AND RECEIVER

The MV1443 combines the Timeslot Zero Transmitter and Receiver functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations and forms part of the GPS 2Mbit PCM signalling series of devices. The circuit is fabricated in CMOS and operates from a single +5V supply with all inputs and outputs being TTL compatible.

The Timeslot Zero Transmitter half of the circuit is responsible for generating the timeslot zero synchronising word of a 2Mbit PCM link in accordance with CCITT Recommendation G.704. This function is performed by alternately generating sync frames, containing the CCITT Frame Alignment Signal, and non-sync frames containing user data bits.

The Timeslot Zero Receiver function searches for the CCITT Frame Alignment signal in the incoming data stream and when this is present the receiver synchronises itself to this pattern in accordance with the Frame Alignment strategy detailed in CCITT Recommendation G.732. Once frame alignment has been achieved the Timeslot Zero Receiver produces various timing outputs for the use of external circuitry and extracts the user data bits of timeslot zero.

FEATURES

- Single +5V supply.
- All Inputs and Outputs TTL compatible.
- Transmitter generates Frame Alignment Signal in accordance with CCITT Recommendation G.704.
- Enables access to User Data Bits of Timeslot Zero.
- Receiver Frame Synchronisation carried out in accordance with CCITT Recommendation G.732.
- Provides Alarm Outputs for Reception of Corrupted Alignment word and Loss of Frame Alignment.
- Extracts the International Spare Bits from Alternate Frames or from Frames 13 and 15 of the CCITT CRC multiframe.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

ELECTRICAL RATINGS

Supply Voltage	-0.5V to +7V
Input Voltage	-0.5V to VDD +0.5V
Output Voltage	-0.5V to VDD +0.5V

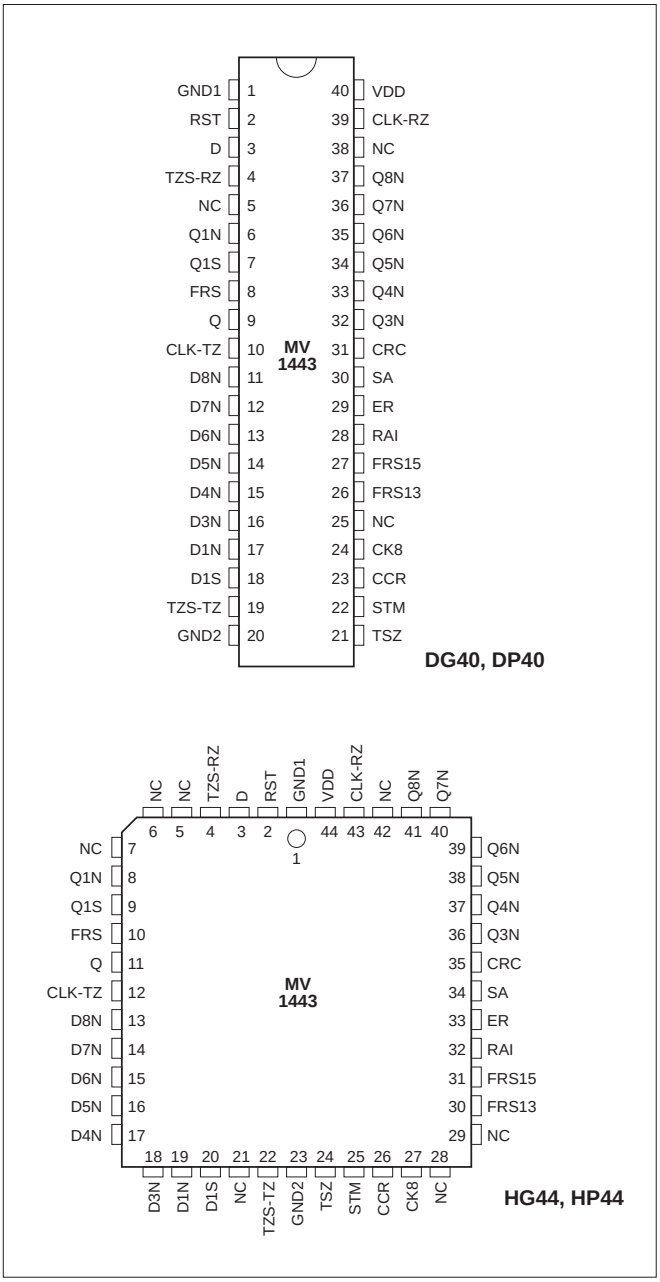


Fig. 1 Pin connections - top view

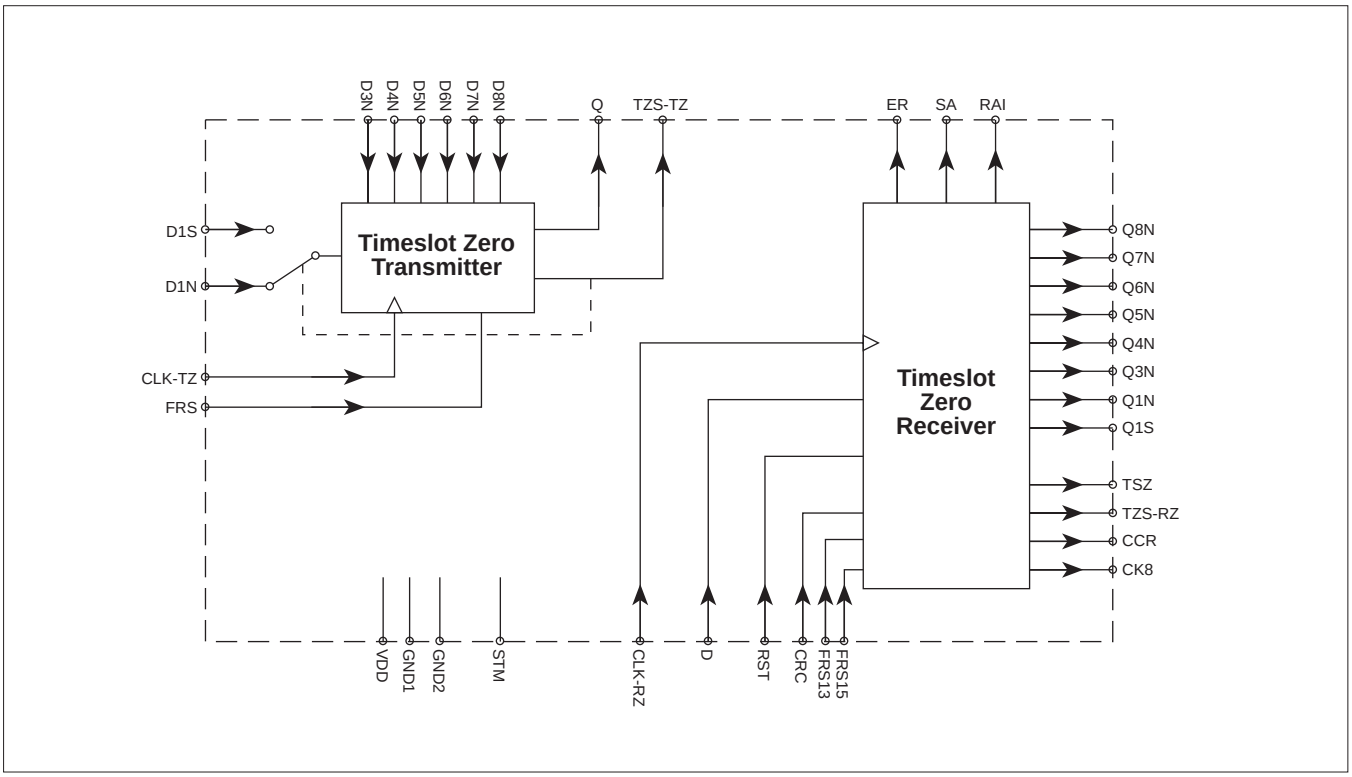


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The MV1443 combines the Timeslot Zero Transmitter and Receiver functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The block diagram of the MV1443 is shown in Fig.2 and the function of each block is now described separately.

Timeslot Zero Transmitter

The Timeslot Zero Transmitter circuit generates the timeslot zero synchronising word required by a 2.048Mbit PCM link in accordance with CCITT Recommendation G.704. During alternate frames, denoted sync frames, the CCITT Frame Alignment Signal (FAS - 0011011) is combined with the International / CRC data bit input, D1S, for bit 1 and injected on to the PCM highway via the Q output. During the other interleaved frames, denoted non-sync frames, bit 2 of timeslot zero is set to '1' to avoid imitation of the FAS and this is combined with the second International / CRC data bit, D1N, for bit 1 and the user data bits, D3N-D8N, for bits 3 to 8, and again injected on to the PCM highway.

In order to perform this function the Timeslot Zero Transmitter requires 2 timing inputs in addition to the parallel data bit inputs, pins CLK-TZ and FRS. The CLK-TZ input is a 2.048MHz clock input whilst FRS is a high going pulse, 8 clock periods long, which is required to mask timeslot zero of each frame. In addition to the PCM data stream output the Timeslot Zero Transmitter produces a timing output, TZS-TZ, which changes state one clock period after the end of Timeslot Zero and is high during the transmission of timeslot zero of sync frames.

The timing diagram of the Timeslot Zero Transmitter circuit is shown in Fig.3.

Timeslot Zero Receiver

The Timeslot Zero Receiver circuit is responsible for searching for and locking on to the CCITT Frame Alignment Signal present in timeslot zero of the PCM data stream being clocked in to its D input. This process is carried out in accordance with the loss and recovery of frame alignment strategy described in CCITT Recommendation G.732. Once frame alignment has been achieved the Timeslot Zero Receiver circuit outputs various timing reference signals for the synchronisation of external circuitry. These timing outputs will all free run if frame synchronisation is subsequently lost. In addition, a control input, RST, may be used to reset this synchronisation process, forcing the receiver out of frame alignment.

The Timeslot Zero Receiver circuit produces 4 timing outputs for use by external circuitry if required. The first of these timing outputs is TSZ which is an 8 clock period long, high going pulse masking the position of timeslot zero, similar to the FRS input of the Timeslot Zero Transmitter, and facilitates the frame alignment of external circuitry. The second timing output, TZS-RZ, is a 4KHz signal which changes state once per frame, one clock period after the end of timeslot zero, and is high during sync frames to allow sync and non-sync frames to be distinguished. The third timing output, CCR, is a low going pulse, one clock period wide, occurring during 1 bit, timeslot 1 of sync frames. The final timing output, CK8, is an 8KHz signal going low at the end of bit 7 of each timeslot zero and high at the end of bit 7 in each timeslot 16.

In addition to these timing outputs, two alarm outputs are provided to indicate errors in the incoming data stream. The first of these alarms, ER, goes high for one frame following a sync frame in which a corrupted FAS was detected when the receiver is in sync. Three consecutive alarms of this type will put the receiver out of sync. The second alarm, SA, goes high to indicate that the Timeslot Zero Receiver is out of frame alignment.

In addition to the frame synchronisation process, the Timeslot Zero Receiver is also responsible for extracting the user data bits of non-sync words and the two International / CRC bits of timeslot zero. The user data bits present in bits 3 to 8 of timeslot zero of non-sync frames are extracted and output on the Q3N-Q8N parallel data outputs. The third bit of non-sync words, Q3N, is used as the remote alarm bit in 2Mbit PCM systems and a third alarm output, RAI, is derived from this bit. This alarm is a persistence checked version of Q3N which goes high when two consecutive Q3N bits have been received high whilst the receiver is in sync. The Timeslot Zero Receiver also extracts the data present in bit 1 of timeslot zero under control of the CRC input. This input selects between CCITT CRC-4 and non-CRC-4 modes of operation. In non-CRC-4 mode, the international spare bits are extracted from bit 1 of all sync and non-sync frames and output on pins Q1S and Q1N respectively. In CRC-4 mode, these data outputs are extracted from bit 1 of frames 13 and 15 of the CCITT CRC-4 multiframe structure respectively. In order to accomplish this, two timing inputs, FRS13 and FRS15, are required in CRC-4 mode. These inputs are required to be high during bit 8 of the appropriate frame, low during bit 8 of any other non-sync frame and any state elsewhere. The timing diagrams for the Timeslot Zero Receiver are shown in Fig.4

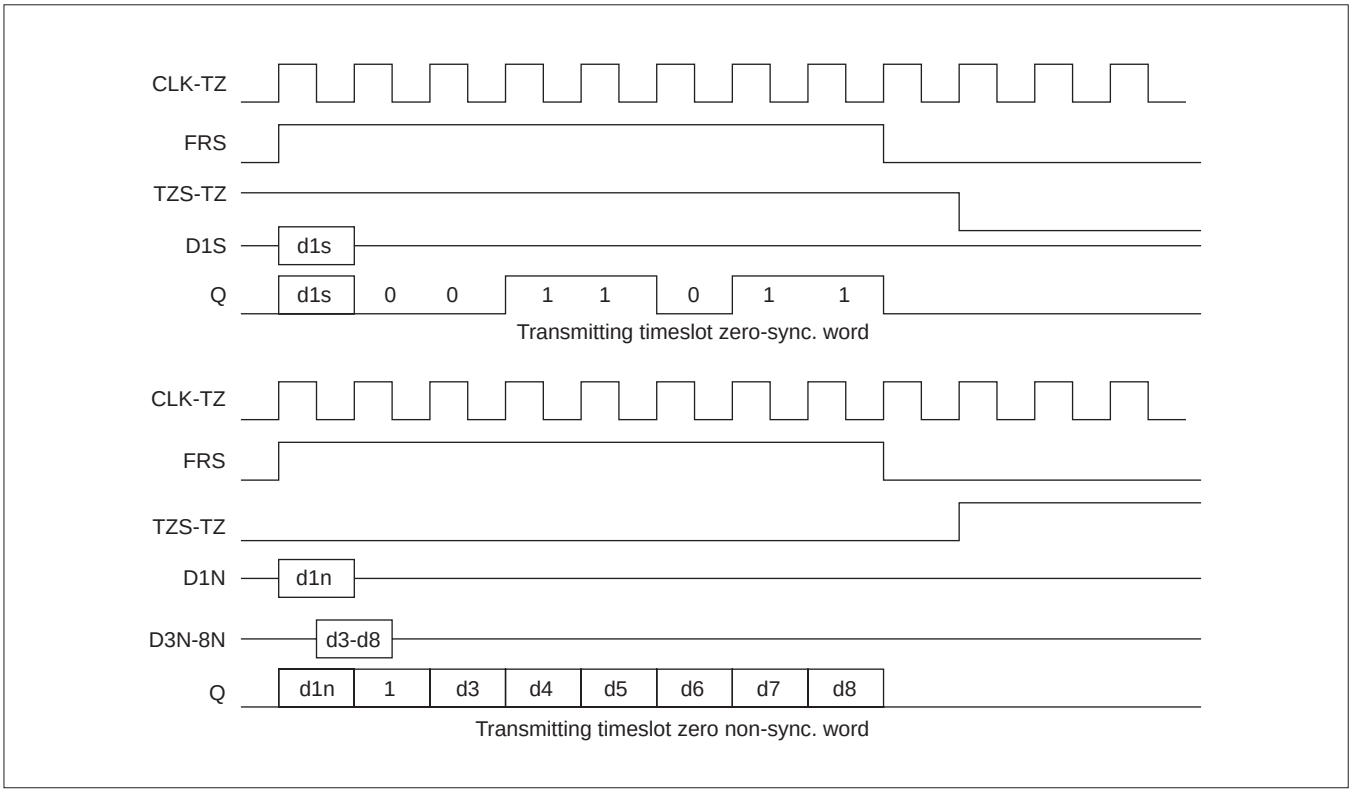
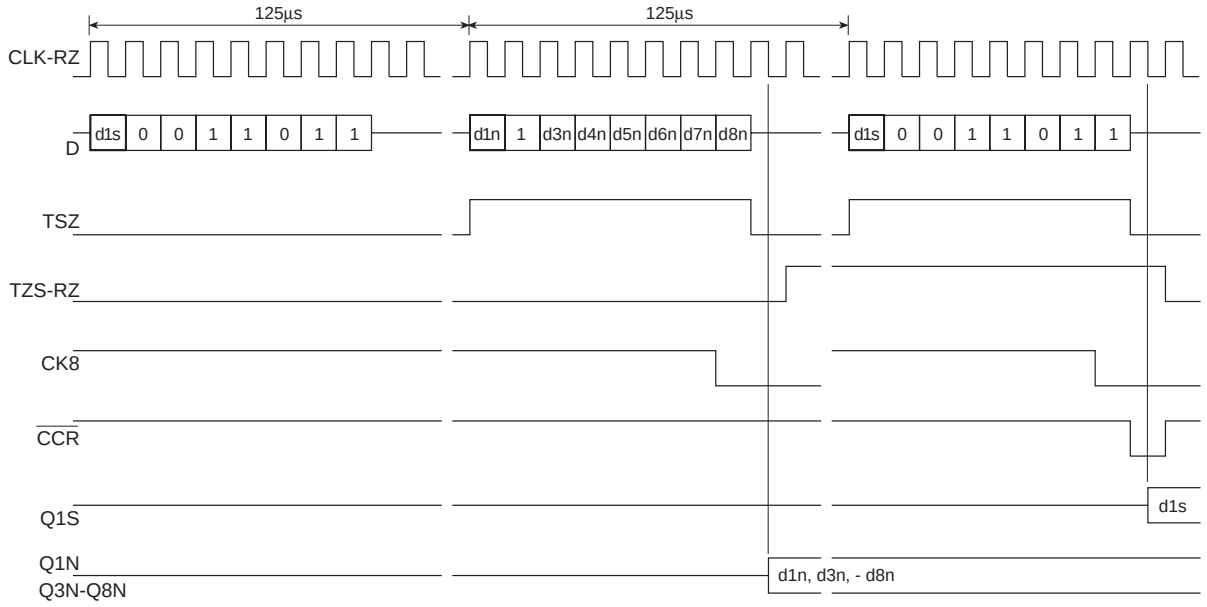
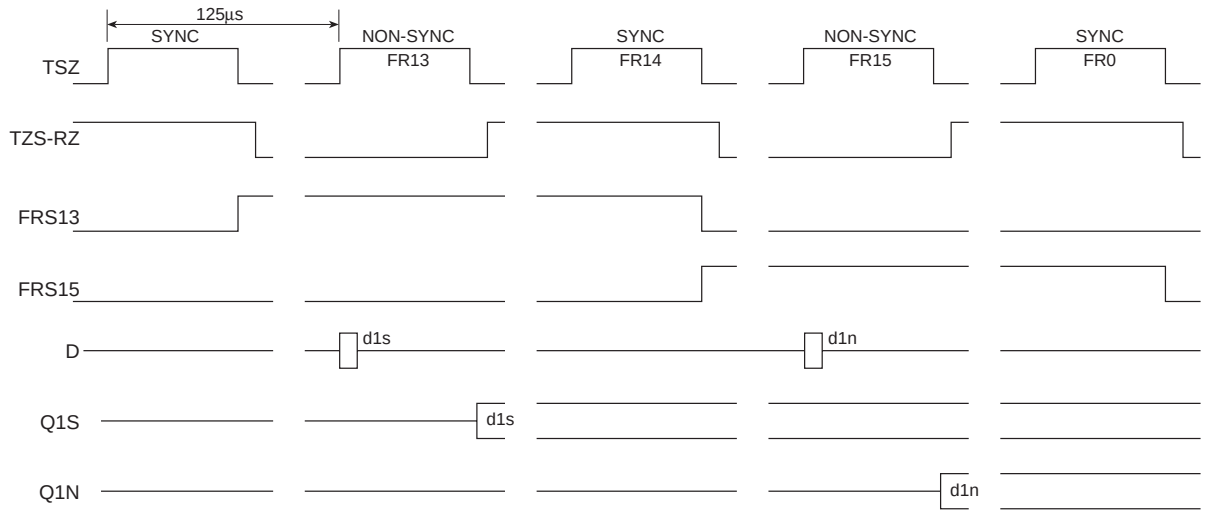


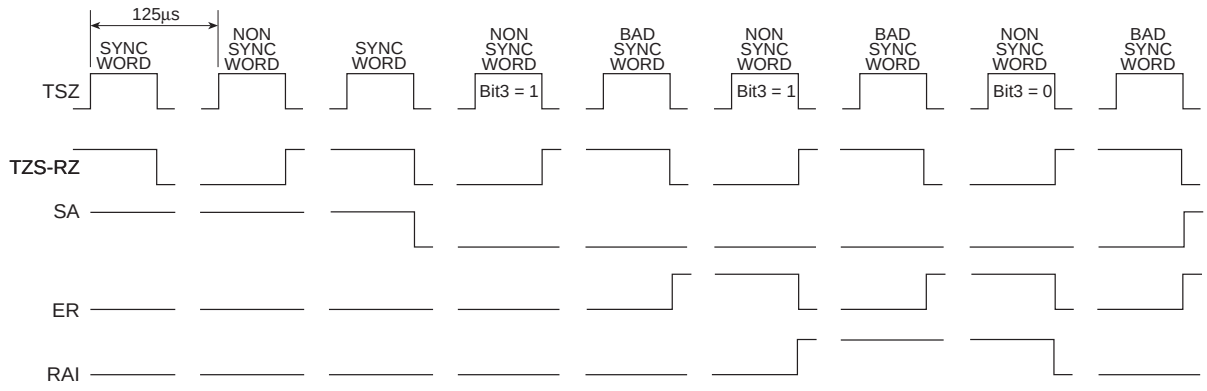
Fig. 3 Timeslot zero transmitter timing



MV1443 first coming into sync., generating timing signals (non-CRC mode)



MV1443 extracting Signalling Data (CRC mode)



MV1443 synchronisation process

Fig. 4 Timeslot zero receiver timing

PIN DESCRIPTIONS

Pin name	Pin Number		Pin Description
	DG40	HG44	
GND1	1	1	Digital Ground. 0V (Note 1)
RST	2	2	Reset Input to Timeslot Zero Receiver. A logic high on this pin straddling a falling edge of CLK-RZ will reset the state machine of the Timeslot Zero Receiver, forcing it out of frame alignment.
D	3	3	PCM Data Stream Input to Timeslot Zero Receiver. This pin is used to input the 2.048Mbit PCM data stream to the Timeslot Zero Receiver and it is this data stream which is searched for the Frame Alignment Signal. This input is latched by the falling edge of CLK-RZ.
TZS-RZ	4	4	Timeslot Zero Sync Frame Output from Timeslot Zero Receiver. This 4KHz output changes state at the end of bit 1, timeslot 1 (Note 2) of every frame and is high during timeslot zero of sync frames.
Q1N	6	8	International / CRC Data Bit Output of Timeslot Zero Receiver for Non-sync Frames. With CRC=0, this output latches data from bit 1, timeslot zero of non-sync frames. With CRC=1, this output latches data from bit 1, timeslot zero of frame 15 of the CRC-4 multiframe, under control of the FRS15 input. In either case this output changes state on the falling edge of CLK-RZ, half a clock period after the end of timeslot zero.
Q1S	7	9	International / CRC Data Bit Output of Timeslot Zero Receiver for Sync Frames. With CRC=0, this output latches data from bit 1, timeslot zero of sync frames. With CRC=1, this output latches data from bit 1, timeslot zero of frame 13 of the CRC-4 multiframe, under control of the FRS13 input. In either case this output changes state on the falling edge of CLK-RZ, half a clock period after the end of timeslot zero.
FRS	8	10	Timeslot Zero Frame Sync Input of Timeslot Zero Transmitter. This input is required to be an 8 bit long, high going pulse masking timeslot zero. This input is latched by the falling edge of CLK-TZ although the first bit of timeslot zero is output asynchronously after the rising edge of FRS is detected.
Q	9	11	Timeslot Zero Data Stream Output of Timeslot Zero Transmitter. The sync and signalling data words produced by the Timeslot Zero Transmitter are output on this pin in 8 bit bursts during timeslot zero. During any other timeslot this output is held low. Bit 1 appears immediately after the rising edges of CLK-TZ and FRS.
CLK-TZ	10	12	2.048MHz Clock Input to Timeslot Zero Transmitter.
D8N D7N D6N D5N D4N D3N	11 12 13 14 15 16	13 14 15 16 17 18	User Data Bit Inputs to Timeslot Zero Transmitter. These 6 parallel data inputs are inserted by the Timeslot Zero Transmitter into bits 8-3 of timeslot zero during non-sync words. These inputs must be set up prior to the rising edge of CLK-TZ at the end of bit 1, timeslot zero of non-sync frames.

PIN DESCRIPTIONS (continued)

Pin name	Pin Number		Pin Description
	DG40	HG44	
D1N	17	19	International / CRC Data Bit Input to Timeslot Zero Transmitter for Non-Sync Frames. The data on this pin is output on the Q pin during bit 1, timeslot zero of non-sync frames and must be set up prior to the rising edge of FRS during non-sync frames.
D1S	18	20	International / CRC Data Bit Input to Timeslot Zero Transmitter for Sync Frames. The data on this pin is output on the Q pin during bit 1, timeslot zero of sync frames and must be set up prior to the rising edge of FRS during sync frames.
TZS-TZ	19	22	Timeslot Zero Sync Frame Output from Timeslot Zero Transmitter. This 4KHz output changes state at the end of bit 1, timeslot 1 of every frame and is high during timeslot zero of sync frames.
GND2	20	23	Digital Ground. 0V (Note 1)
TSZ	21	24	Timeslot Zero Marker Output from Timeslot Zero Receiver. This timing output goes high for the 8 clock periods of timeslot zero and is low at all other times.
STM	22	25	Scan Path Test Global Mode Pin. A logic high on this pin configures the MV1443 in scan test mode. For normal operation this pin should be tied low.
CCR	23	26	Channel Reset Timing Output from Timeslot Zero Receiver. This output pulses low for a single period during bit 1, timeslot 1 of sync frames.
CK8	24	27	8KHz Clock Output from Timeslot Zero Receiver. This output goes low at the beginning of bit 8, timeslot 0 and high at the beginning of bit 8, timeslot 16.
FRS13	26	30	Frame 13 Marker Input to Timeslot Zero Receiver. This input is used by the Timeslot Zero Receiver operating in CRC-4 mode to reference the position of Frame 13. This input is required to be high during bit 8, Frame 13 of the CRC multiframe and low during bit 8 of all other non-sync frames.
FRS15	27	31	Frame 15 Marker Input to Timeslot Zero Receiver. This input is used by the Timeslot Zero Receiver operating in CRC-4 mode to reference the position of Frame 15. This input is required to be high during bit 8, Frame 15 of the CRC multiframe and low during bit 8 of all other non-sync frames.
RAI	28	32	Remote Alarm Indication Output of Timeslot Zero Receiver. This alarm output is a persistence checked version of the Q3N output. When the receiver is in sync this output will go high if 2 consecutive Q3N bits are received high. This output changes state at the beginning of bit 1, timeslot 1 of non sync frames. When the receiver is out of sync this output is forced low in the non-sync frame following the last bad sync frame, and is held low until the receiver comes back in to sync.

PIN DESCRIPTIONS (continued)

Pin name	Pin Number		Pin Description
	DG40	HG44	
ER	29	33	Sync Word Error Output of Timeslot Zero Receiver. This alarm output goes high for one frame immediately after detection of a bad timeslot zero frame alignment signal, whilst the receiver is in sync. Three consecutive errors of this type will put the receiver out of sync and the last ER pulse of this sequence will be longer than 256 periods if a valid sync word is detected during the pulse.
SA	30	34	Synchronisation Alarm Output from Timeslot Zero Receiver. This output is high whenever the receiver is out of sync and only changes state at the beginning of bit 1, timeslot 1 of sync frames.
CRC	31	35	CRC-4 Mode Select Input to Timeslot Zero Receiver. This input is used to control the extraction of the Q1N and Q1S data outputs from the incoming PCM data stream. A logic high on this input selects CRC-4 mode of operation.
Q3N Q4N Q5N Q6N Q7N Q8N	32 33 34 35 36 37	36 37 38 39 40 41	User Data Bit Outputs of Timeslot Zero Receiver. These 6 parallel data outputs are extracted from bits 3-8 of timeslot zero during non-sync frames. These outputs change state on the falling edge of CLK-RZ half a clock period after the end of timeslot zero.
CLK-RZ	39	43	2.048MHz Clock Input to Timeslot Zero Receiver.
VDD	40	44	Digital Supply Voltage. 5V

NOTES

1. In order to facilitate adequate supply decoupling, both digital ground pins should be connected to 0V.
2. The bits of a timeslot are numbered from 1 to 8 whereas the timeslots of a frame are numbered from 0 to 31 and the frames of a CCITT multiframe are numbered from 0 to 15.
3. All inputs except STM have 100K on-chip pull down resistors. The STM pin has neither pull-up nor pull-down resistor and should be tied to digital ground during normal operation.

ELECTRICAL CHARACTERISTICS

Test Conditions:

Supply Voltage VDD = 5V ± 0.5V Ambient Temperature Tamb = -40°C to +85°C

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0.0		0.8	V	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	V	
Low Level Output Voltage	V_{OL}			0.4	V	Isink=2mA
High Level Output Voltage	V_{OHT} V_{OHC}	2.4 V—-1.0			V V	Isource=2mA Isource=1mA
Input Leakage Current	I_{IL}	-10		200	uA	$V_{IN}=V_{DD}$ or V_{SS}
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock Period	t_{CP}	400			ns	See Fig. 5
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock High/LowTime	t_{CH}/t_{CL}	150			ns	See Fig. 5
TRANSMITTER						
FRS Rising Hold Time	t_{FRH}	50			ns	See Fig. 6
FRS Rising Setup Time	t_{FRS}	100			ns	See Fig. 6
FRS Falling Hold Time	t_{FFH}	100			ns	See Fig. 6
FRS Falling Setup Time	t_{FFS}	50			ns	See Fig. 6
International Data Bit Setup Time	t_{IDS}	50			ns	See Fig. 6
International Data Bit Hold Time	t_{IDH}	50			ns	See Fig. 6
User Data Setup Time	t_{UDS}	50			ns	See Fig. 6
User Data Hold Time	t_{UDH}	50			ns	See Fig. 6
Q Propagation Delay from FRS (bit 1, TS0)	t_{QPDF}			60	ns	See Fig. 6, Note 1.
Q Propagation Delay from CLK-RZ (bits 2-8	t_{QPDC}			60	ns	See Fig. 6, Note 1.
TZS-TZ Propagation Delay	t_{TTPD}			60	ns	See Fig. 6, Note 1.
RECEIVER						
Data / Control Setup Time	t_{DS}	50			ns	See Fig. 7, Note 2.
Data / Control Hold Time	t_{DH}	50			ns	See Fig. 7, Note 2.
Timing / Alarm Propagation Delay	t_{TAPD}			60	ns	See Fig. 7, Notes 1 and 3.
Data Outputs Propagation Delay	t_{DPD}			75	ns	See Fig. 7, Notes 1 and 4.

NOTES

1. All output propagation delays are measured with a 50pF load.

2. The Timeslot Zero Receiver Data / Control setup and hold time parameters, t_{DS} and t_{DH}, apply to the following inputs: D, RST, FRS13 and FRS15.

3. The Timeslot Zero Receiver Timing / Alarm Output propagation delay parameter applies to the following outputs: TSZ, TZS, CCR, CK8, ER, SA and RAI.

4. The Timeslot Zero Receiver Data Output propagation delay parameter applies to the following outputs: Q1S, Q1N, Q3N, Q4N, Q5N, Q6N, Q7N and Q8N.

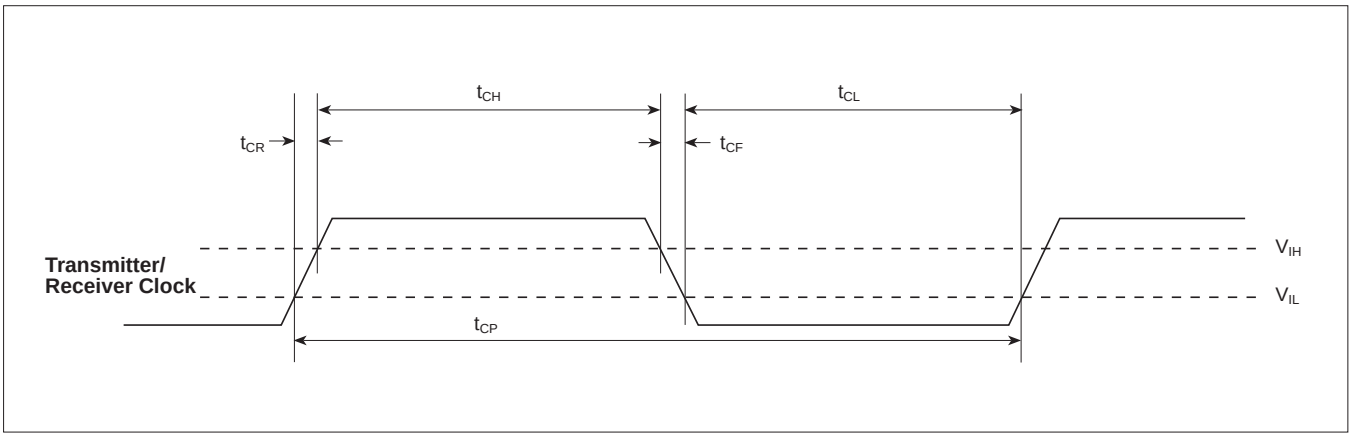


Fig. 5 Clock Timing Parameters

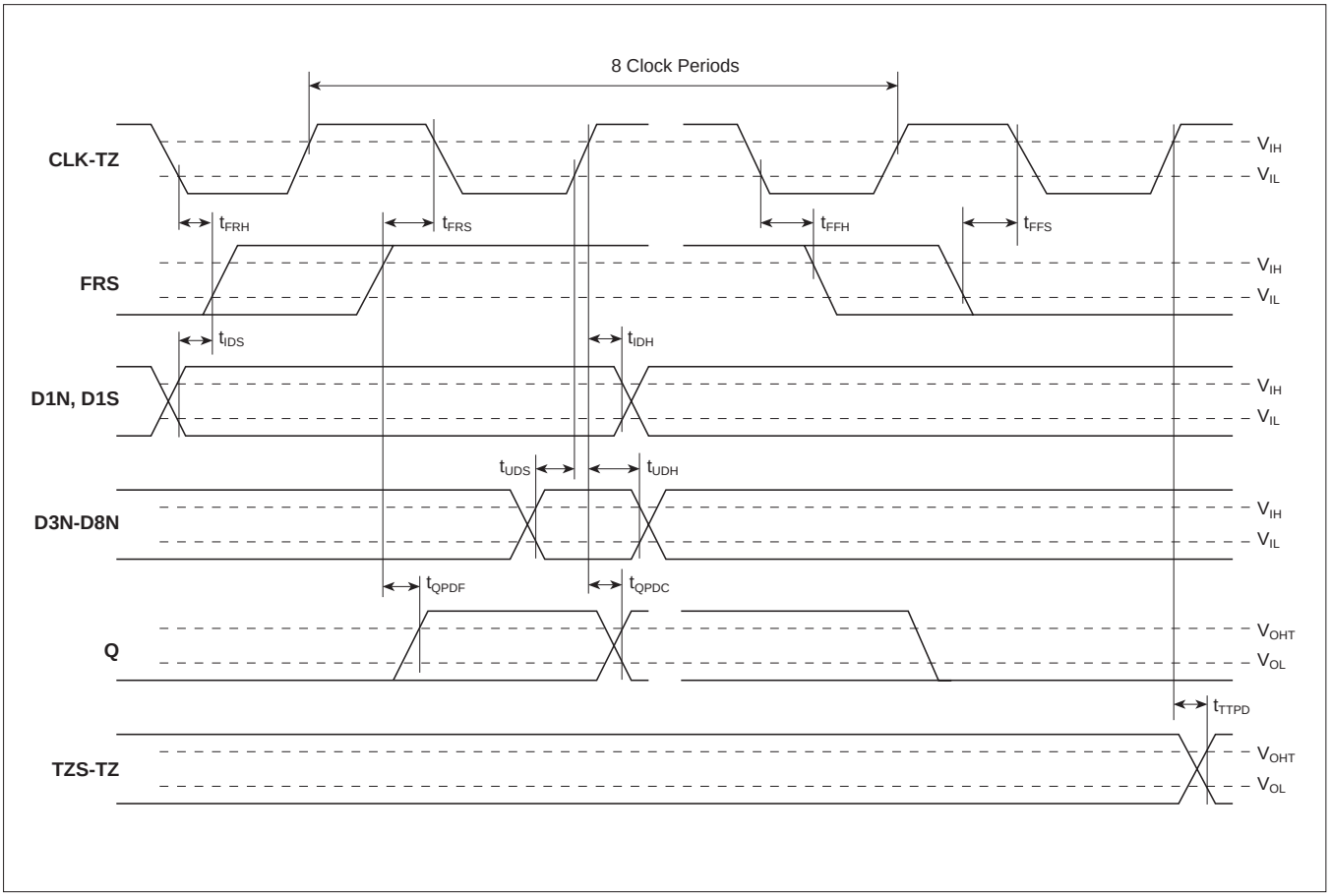


Fig. 6 Timeslot Zero Transmitter Timing

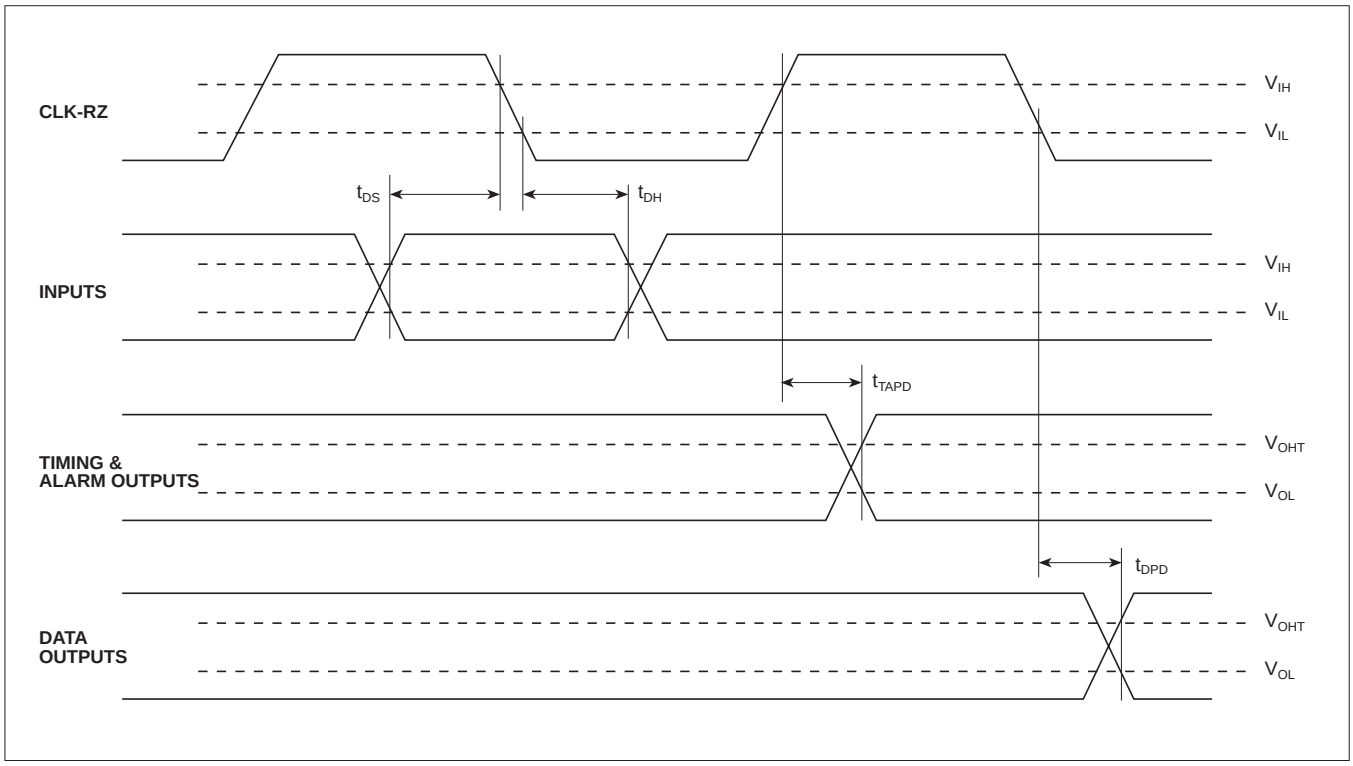


Fig. 7 Timeslot Zero Receiver Timing

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