ELECTRICAL ERASABLE PROGRAMMABLE ROM

OUTLINE

The EEPROM IC MEMORY CARD series is made up of Electrically Erasable Programmable ROM chips. Capacity is from 8K Bytes to 128K Bytes.
It is available in both NMOS and CMOS. IE series is 8 bit wide data bus.

VARIATION

Part Number	Memory Size	Description
EEC008IEC0	8K Bytes	8K x 8 bits CMOS EEPROM CARD
EEC008IEN0	8K Bytes	8K x 8 bits NMOS EEPROM CARD
EEC016IEC0	16K Bytes	16K x 8 bits CMOS EEPROM CARD
EEC016IEN0	16K Bytes	16K x 8 bits NMOS EEPROM CARD
EEC032IEC0	32K Bytes	32K x 8 bits CMOS EEPROM CARD
EEC032IEN0	32K Bytes	32K x 8 bits NMOS EEPROM CARD
EEC064IEC0	64K Bytes	64K x 8 bits CMOS EEPROM CARD
EEC128IEC0	128K Bytes	128K x 8 bits CMOS EEPROM CARD

SIZE AND WEIGHT

(1) Size : 54.0 ±0.1 mm wide by 86.0 ±0.2 mm long by 2.4 ±0.15 mm thick
(2) Thickness at the contacts : 1.80 ±0.15 mm
(3) Weight : approx. 23 grams
(4) Card type : 40 pin Card Edge

FEATURES

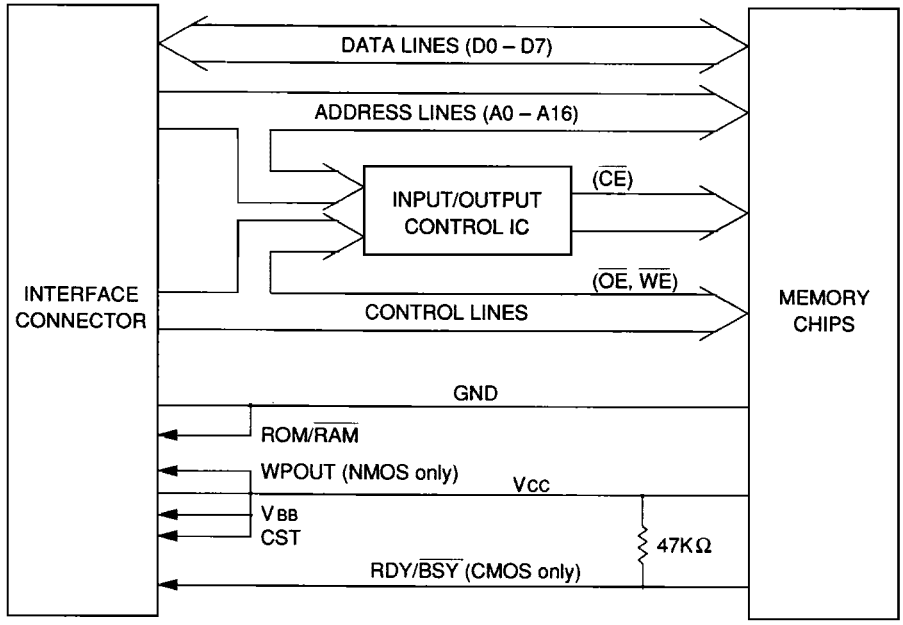
(1) Shutter Mechanism

This mechanism protects the terminals from dirt, static electricity, hand contact, etc. The shutter is opened by tabs on the connector during insertion, and is closed by built in springs when the card is removed from the connector.
(Our connector is required to operate this feature.)

(2) Polarization of the connector to the card

The IC card and our connector have a mechanism to safeguard against incorrect insertion. This mechanism protects the circuits of the unit, the connector, and the card from potential damage.

INTERFACE SIGNAL DIRECTION



(1) D0 to D7

Data input/output, 8 bit wide

(2) A0 to A16

Address inputs
Unused address lines should be "no connect".

(3) CE

Card Enable input (Active HIGH)
Memory card operates when CE is "HIGH"

(4) $\overline{OE}$

Output Enable input (Active LOW)
Memory card output data when $\overline{OE}$ is "LOW"

(5) $\overline{WE}$

Write Enable input (Active LOW)
Writing data into the card is possible when $\overline{WE}$ is "LOW"

(6) WPOUT

NMOS* : This line is connected to VCC line.
CMOS : This line is used as RDY/$\overline{BSY}$ signal. IF this line is VOL state, the card is under write operation (BUSY), if this line is VOH state, the card is accessible (READY).

(7) CST*

Output line to indicate that the card is accessible or not.
This line is connected to VCC line.

(8) ROM/$\overline{RAM}$*

This line is connected VCC or GND line.
Output line to indicate the card type.
VCC level indicates ROM : OTP (EPC, BPC), MASKROM (MRC), FLASH MEMORY (FPC)
GND level indicates RAM : SRAM (RBC), EEPROM (EEC), FLASH MEMORY (FEC)
Do never use as card VCC or GND line.

(9) VBB*

This line is connected to VCC line.

(10) VCC

Power source : +5 V ±10%.

(11) GND

Ground

Note: See the recommended interface circuit.
* Do never use as VCC or GND line.

ABSOLUTE MAXIMUM RATING

Symbol	Description	Maximum Rating	Unit
VCC	VCC Power supply	–0.5 to 7.0	V
VIN	Input Voltage	–0.5 to VCC +0.5	V
VOUT	Output Voltage	–0.5 to VCC	V
TOP	Operating Temperature	0 to 60	°C
TSTG	Storage Temperature	–20 to 60	°C
HSTG	Storage humidity	0 to 65	%
PD	Power dissipation	2	W

Note: VIN should be under 7.0 V.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

Symbol	Variation	Item	Condition	Min	Typ	Max	Unit
C1	EEC008IEC0 EEC008IEN0	A0 to A12,CE,$\overline{OE}$, $\overline{WE}$	V_{IN} = 0 V	—	6	8	pF
	EEC032IEC0 EEC032IEN0	A0 to A12,$\overline{OE}$,$\overline{WE}$		—	24	32	pF
		A13, A14, CE		—	6	8	pF
	EEC016IEC0 EEC016IEN0	A0 to A12,$\overline{OE}$,$\overline{WE}$		—	12	16	pF
		A13, CE		—	6	8	pF
	EEC064IEC0						pF
	EEC128IEC0						pF
C2	EEC008IEC0 EPC008IEN0	A0 to D7	V_{IN}/V_{OUT} = 0 V	—	10	14	pF
	EEC016IEC0 EEC016IEN0			—	20	28	pF
	EEC032IEC0 EEC032IEN0			—	40	56	pF
	EEC064IEC0						pF
	EEC128IEC0						pF

Note: The above figures are reference only.

DC RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min	Typ	Max	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High input voltage	2.2	—	V_{CC} +0.3	V
V_{IL}	Low input voltage	–0.3	—	0.6	V

DC ELECTRICAL CHARACTERISTICS
(Ta = 0 to 60°C, V_{CC} = 5 V ±10%)

Symbol	Description	Note	Condition	Min	Typ	Max	Unit
V_{OH}	High output	1	I_{OH} = –400 uA	2.4	—	—	V
V_{OL}	Low output	1	I_{OL} = 2.1 mA	—	—	0.4	V
I_{LI}	Leakage current	2	V_{IN} = 0 V to V_{CC}	–10	—	10	µA
I_{LO}	Leakage current	1	CE = V_{IL} or OE = V_{IH}, V_{OUT} = 0 V to V_{CC}	–10	—	10	µA
I_{ACT}	Active current	3	CE = V_{IH}				
			EEC008IEC0	—	—	25	mA
			EEC008IEN0	—	60	100	mA
			EEC016IEC0	—	—	25	mA
			EEC016IEN0	—	85	140	mA
			EEC032IEC0	—	—	25	mA
			EEC032IEN0	—	135	220	mA
			EEC064IEC0				mA
			EEC128IEC0				mA
I_{STB}	Standby current	4	CE = V_{IL}				
			EEC008IEC0	—	—	1	mA
			EEC008IEN0	—	25	40	mA
			EEC016IEC0	—	—	1	mA
			EEC016IEN0	—	50	80	mA
			EEC032IEC0	—	—	1	mA
			EEC032IEN0	—	100	160	mA
			EEC064IEC0				mA
			EEC064IEN0				mA
			EEC128IEC0				mA
			EEC128IEN0				mA

Notes:
1. D0 to D7
2. A0 to A16, $\overline{OE}$, $\overline{WE}$, CE
3. D0 to D7, CST = No Load//other inputs = V_{IH} or V_{IL}

OPERATING MODES

Mode	CE	$\overline{OE}$	$\overline{WE}$	WPOUT	D0 to D7	CST
READ	V_{IH}	V_{IL}	V_{IH}	V_{OH}	DATA OUTPUT	HO
WRITE	V_{IH}	V_{IH}	V_{IL}	V_{OH} to V_{OL}	DATA INPUT	HO
STANDBY	V_{IL}	*	*	V_{OH}	HZ	HO
BYTE ERASE	V_{IH}	V_{IH}	V_{IL}	**	FF DATA INPUT	HO
ALL ERASE	V_{IH}	V_{IL}	V_{IL}	V_{OH}	FF DATA INPUT	HO

Notes HZ : High Impedance
* : V_{IH} or V_{IL}
** : V_{OH} (NMOS)
: V_{OH} to V_{OL} (CMOS)
ALL ERASE MODE : Only available with NMOS EEPROM CARD
HO : V_{CC} output level

AC ELECTRICAL CHARACTERISTICS (Ta = 0 to 60°C, V_{CC} = 5 V ±10%)

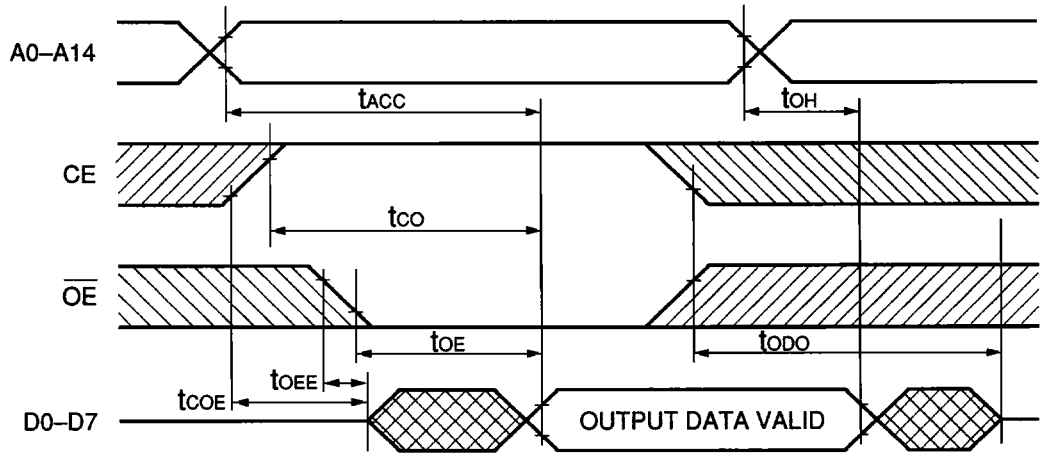
Symbol	Description	Min	Max	Unit
t_{ACC}	Address access time	—	300*	µs
t_{CE}	CE access time	—	320	µs
t_{OE}	$\overline{OE}$ access time	—	150	µs
t_{COE}	CE to enable time	10	—	µs
t_{OEE}	$\overline{OE}$ to enable time	10	—	µs
t_{ODO}	$\overline{OE}$ to disable time	—	130	µs
t_{OH}	DATA hold time	0**	—	µs

* 320 ns at EEC016, EEC032
** 20 ns at EEC016, EEC032

<< AC test conditions >>

Output load : 1 TTL gate + 100 pF (include jig)
Input pulse rise & fall time : 20 ns
Input pulse level : 0.4 V, 2.4 V
Timing measurement comparison level : Input : 0.6 V and 2.2 V
Output : 0.6 V and 2.2 V

READ TIMING



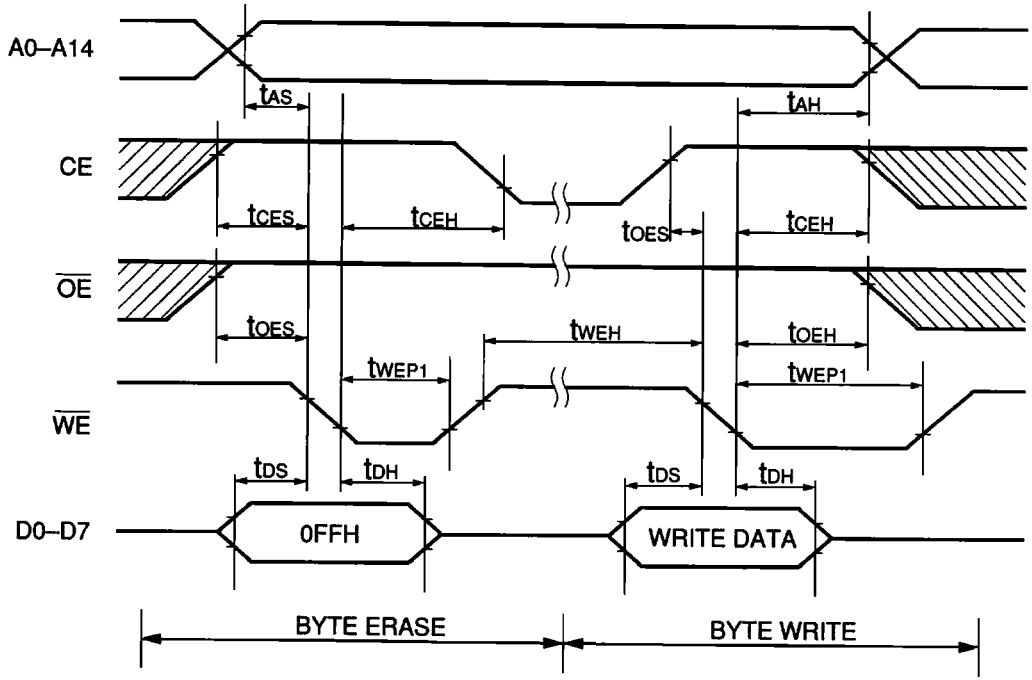
AC ELECTRICAL CHARACTERISTICS AT WRITE (BYTE MODE)
< NMOS ONLY > (V_{CC} = 5 V ±10%, Ta = 25°C ±5°C)

Symbol	Item	Min	Typ	Max	Unit
t_{AS}	Address set up time	10	—	—	ns
t_{OES}	$\overline{OE}$ set up time	0	—	—	ns
t_{DS}	Data set up time	0	—	—	ns
t_{AH}	Address hold time	100	—	—	ns
t_{DH}	Data hold time	100	—	—	ns
t_{OEH}	$\overline{OE}$ hold time	100	—	—	ns
t_{CES}	CE set up time	0	—	—	ns
t_{CEH}	CE hold time	100	—	—	ns
t_{WEP1}	$\overline{WE}$ pulse width	8	10	15	ms
t_{WEH}	$\overline{WE}$ High time	1	—	—	µs

<< AC test conditions >>

Output Load : 100 pF + 1 TTL Gate (include jig)
Input Pulse Level : 0.4 V, 2.4 V
Timing Measurement Comparison Levels : Input : 0.6 V, 2.2 V
: Output : 0.6 V, 2.2 V
Input Rise and fall : 20 ns

TIMING DIAGRAM



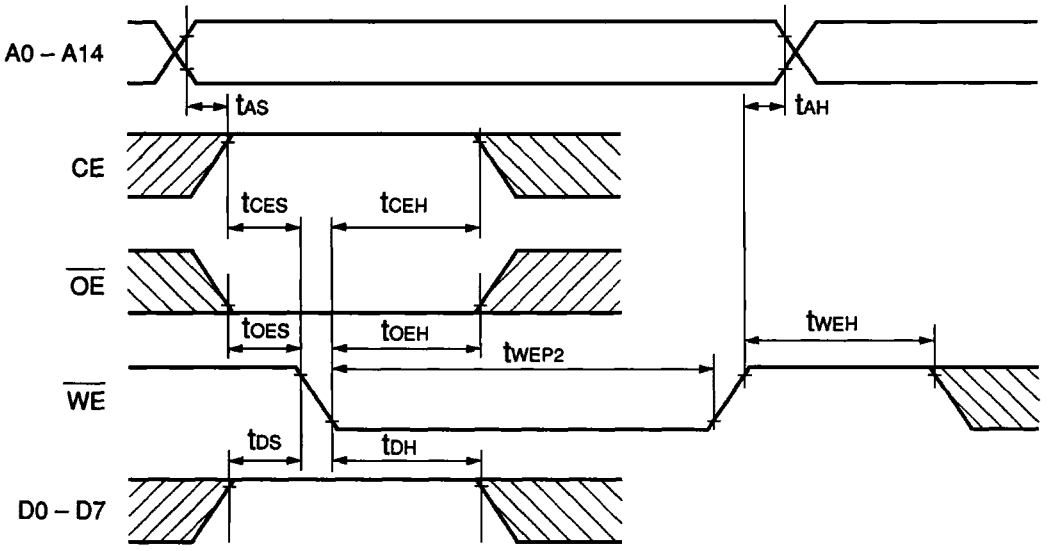
AC ELECTRICAL CHARACTERISTICS AT ALL ERASE < NMOS ONLY > $\overline{WE}$ Controlled (Ta = 0 to 60°C, V_{CC} = 5 V ±10%)

Symbol	Item	Min	Typ	Max	Unit
t_{AS}	Address set up time	10	—	—	ns
t_{AH}	Address hold time	100	—	—	ns
t_{CES}	CE set up time	0	—	—	ns
t_{CEH}	CE hold time	100	—	—	ns
t_{OES}	$\overline{OE}$ set up time	0	—	50	ns
t_{OEH}	$\overline{OE}$ hold time	100	—	—	ns
t_{WEP2}	$\overline{WE}$ pulse width	15	20	25	ms
t_{WEH}	$\overline{WE}$ high time	1	—	—	µs
t_{DS}	Data set up	0	—	—	ns
t_{DH}	Data hold time	100	—	—	ns

<< AC test conditions >>

Output Load	:	100 pF + 1 TTL Gate (include jig)
Input Pulse Level	:	0.4 V, 2.4 V
Timing Measurement Comparison Level	:	Input : 0.6 V, 2.2 V
	:	Output : 0.6 V, 2.2 V
Input Rise and fall	:	20 ns

ERASE TIMING



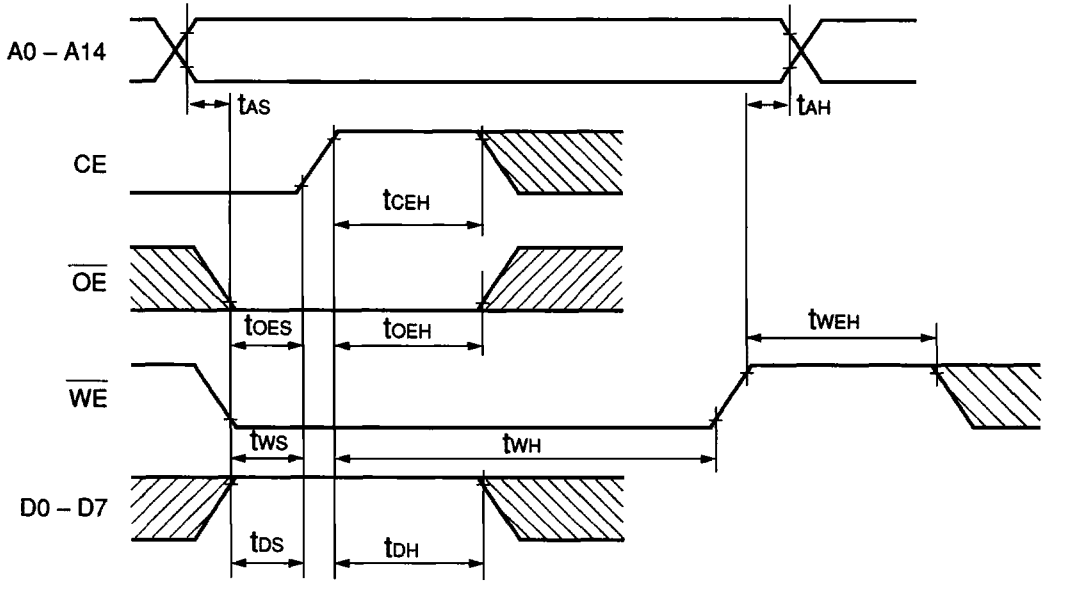
AC CHARACTERISTICS AT ALL ERASE < NMOS ONLY >
CE Controlled (Ta = 0 to 60°C, VCC = 5 V ±10%)

Symbol	Item	Min	Typ	Max	Unit
t_{AS}	Address set up time	10	—	—	ns
t_{AH}	Address hold time	100	—	—	ns
t_{CEH}	CE hold time	100	—	—	ns
t_{OES}	$\overline{OE}$ set up time	0	—	—	ns
t_{OEH}	$\overline{OE}$ hold time	100	—	—	ns
t_{WH}	$\overline{WE}$ hold time	15	20	25	ms
t_{WS}	$\overline{WE}$ set up time	0	—	—	ns
t_{DS}	Data set up	0	—	—	ns
t_{WEH}	$\overline{WE}$ high time	1	—	—	µs
t_{DH}	Data hold time	100	—	—	ns

<< AC test conditions >>

Output Load	:	100 pF + 1 TTL Gate (include jig)
Input Pulse Level	:	0.4 V, 2.4 V
Timing Measurement Comparison Level	:	Input : 0.6 V, 2.2 V
	:	Output : 0.6 V, 2.2 V
Input Rise and fall	:	20 ns

ERASE TIMING



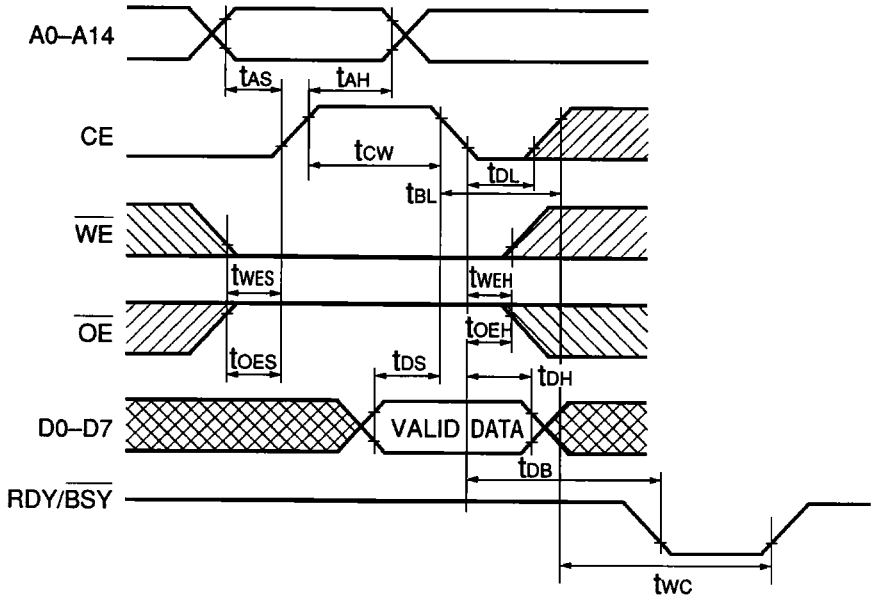
AC ELECTRICAL CHARACTERISTICS AT WRITE (BYTE MODE)
< CMOS ONLY > CE Controlled (V_{CC} = 5 V ±5%, Ta = 25°C ±5°C)

Symbol	Item	Min	Typ	Max	Unit
t_{AS}	Address set up time	10	—	—	ns
t_{OES}	$\overline{OE}$ set up time	0	—	—	ns
t_{DS}	Data set up time	100	—	—	ns
t_{AH}	Address hold time	150	—	—	ns
t_{DH}	Data hold time	40	—	—	ns
t_{OEH}	$\overline{OE}$ hold time	20	—	—	ns
t_{WES}	$\overline{WE}$ set up time	0	—	—	ns
t_{WEH}	$\overline{WE}$ hold time	20	—	—	ns
t_{CW}	CE pulse width	200	—	—	ns
t_{DL}	Data latch time	100	—	—	ns
t_{DB}	RDY/$\overline{BSY}$ delay time	120	—	—	ns
t_{BL}	BYTE load time	30	—	100	µs
t_{WC}	WRITE cycle time	—	—	15	ms

<< AC test conditions >>

Output Load : 100 pF + 1 TTL Gate (include jig)
Input Pulse Level : 0.4 V, 2.4 V
Timing Measurement Comparison Level : Input : 0.6 V, 2.2 V
: Output : 0.6 V, 2.2 V
Input Rise and fall : 20 ns

TIMING DIAGRAM



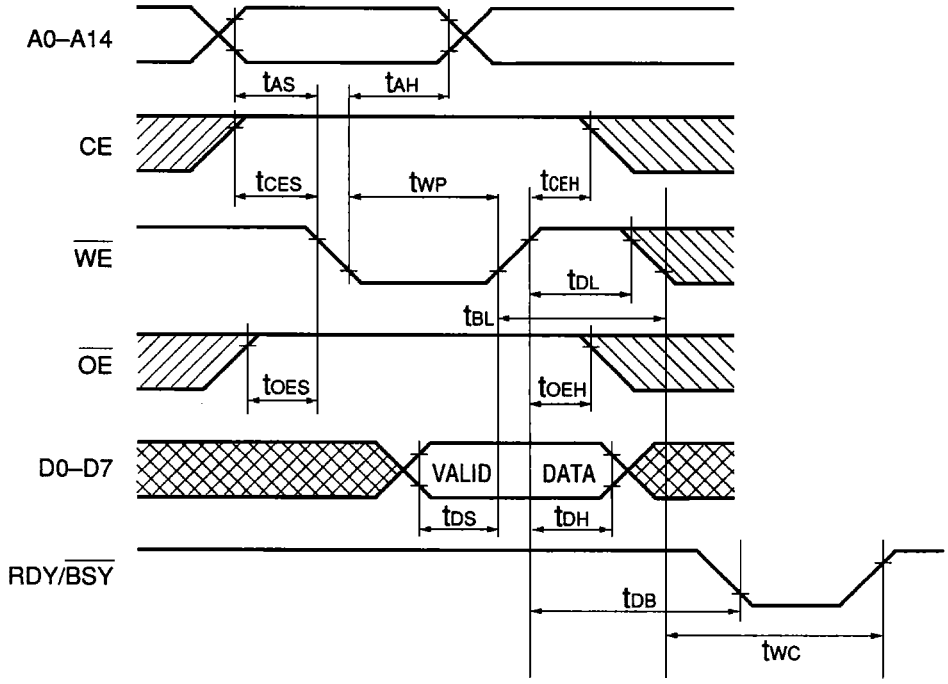
AC ELECTRICAL CHARACTERISTICS AT WRITE (BYTE MODE)
< CMOS ONLY > $\overline{WE}$ Controlled (V_{CC} = 5 V ±10%, Ta = 25°C ±5°C)

Symbol	Item	Min	Typ	Max	Unit
t_{AS}	Address set up time	10	—	—	ns
t_{CES}	CE set up time	20	—	—	ns
t_{DS}	Data set up time	100	—	—	ns
t_{AH}	Address hold time	150	—	—	ns
t_{DH}	Data hold time	30	—	—	ns
t_{CEH}	CE hold time	20	—	—	ns
t_{OES}	$\overline{OE}$ set up time	0	—	—	ns
t_{OEH}	$\overline{OE}$ hold time	0	—	—	ns
t_{WP}	$\overline{WE}$ pulse width	200	—	—	ns
t_{DL}	Data latch time	100	—	—	ns
t_{DB}	RDY/$\overline{BSY}$ delay time	120	—	—	ns
t_{BL}	BYTE load time	30	—	100	µs
t_{WC}	WRITE cycle time	—	—	15	ms

<< AC test conditions >>

Output Load : 100 pF + 1 TTL Gate (including jig)
Input Pulse Level : 0.4 V, 2.4 V
Timing Measurement Comparison Level : Input : 0.6 V, 2.2 V
: Output : 0.6 V, 2.2 V
Input Rise and fall : 20 ns

TIMING DIAGRAM



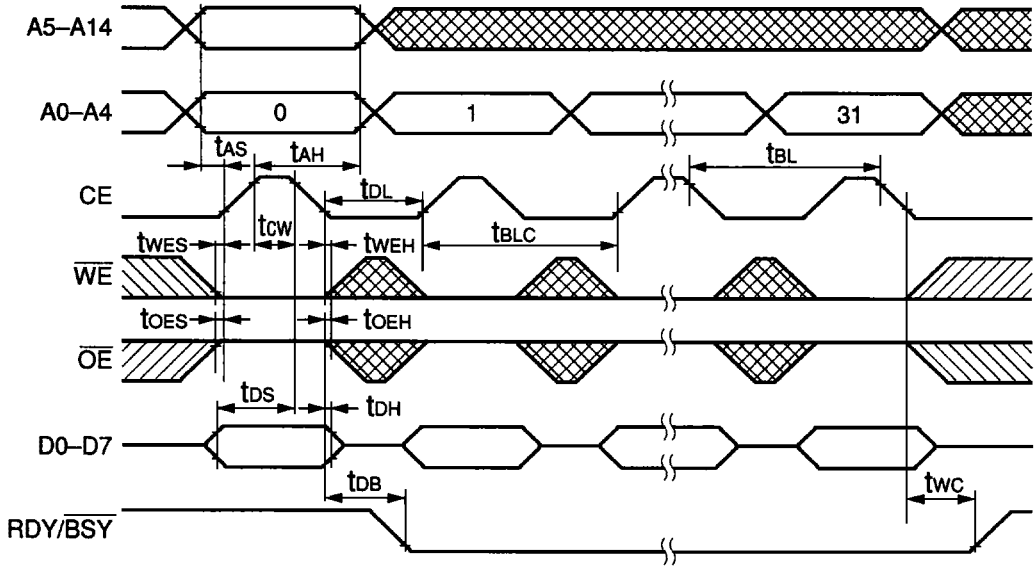
AC ELECTRICAL CHARACTERISTICS AT WRITE (PAGE MODE)
< CMOS ONLY > CE Controlled (V_{CC} = 5 V ±5%, Ta = 25°C ±5°C)

Symbol	Item	Min	Typ	Max	Unit
t_{AS}	Address set up time	10	—	—	ns
t_{OES}	$\overline{OE}$ set up time	0	—	—	ns
t_{DS}	Data set up time	100	—	—	ns
t_{AH}	Address hold time	150	—	—	ns
t_{DH}	Data hold time	50	—	—	ns
t_{OEH}	$\overline{OE}$ hold time	20	—	—	ns
t_{WES}	$\overline{WE}$ set up time	0	—	—	ns
t_{WEH}	$\overline{WE}$ hold time	20	—	—	ns
t_{CW}	CE pulse width	200	—	—	ns
t_{DL}	Data latch time	100	—	—	ns
t_{DB}	RDY/$\overline{BSY}$ delay time	120	—	—	ns
t_{BL}	Byte load time	30	—	100	µs
t_{BLC}	Byte load cycle	0.3	—	30	µs
t_{WC}	WRITE cycle time	—	—	15	ms

<< AC test conditions >>

Output Load : 100 pF + 1 TTL Gate (include jig)
Input Pulse Level : 0.4 V, 2.4 V
Timing Measurement Comparison Level : Input : 0.6 V, 2.2 V
: Output : 0.6 V, 2.2 V
Input Rise and fall : 20 ns

TIMING DIAGRAM



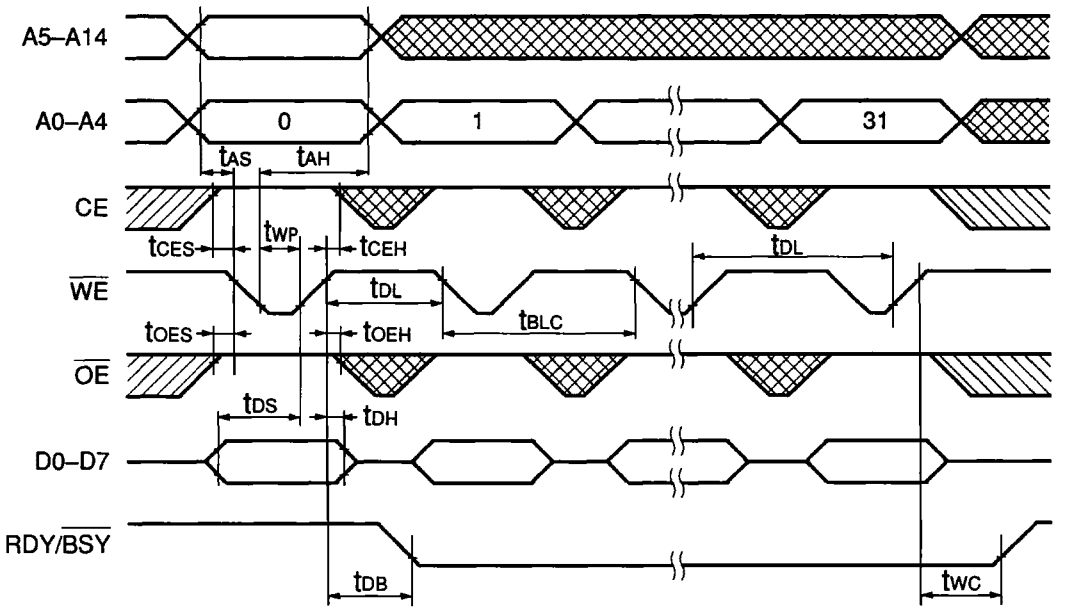
AC ELECTRICAL CHARACTERISTICS AT WRITE (PAGE MODE)
< CMOS ONLY > $\overline{WE}$ Controlled (V_{CC} = 5 V ±10%, Ta = 25°C ±5°C)

Symbol	Item	Min	Typ	Max	Unit
t_{AS}	Address set up time	10	—	—	ns
t_{OES}	$\overline{OE}$ set up time	0	—	—	ns
t_{DS}	Data set up time	100	—	—	ns
t_{AH}	Address hold time	150	—	—	ns
t_{DH}	Data hold time	30	—	—	ns
t_{OEH}	$\overline{OE}$ hold time	0	—	—	ns
t_{CES}	CE set up time	20	—	—	ns
t_{CEH}	CE hold time	20	—	—	ns
t_{WP}	$\overline{WE}$ pulse width	200	—	—	ns
t_{DL}	Data latch time	100	—	—	ns
t_{DB}	RDY/$\overline{BSY}$ delay time	120	—	—	ns
t_{BL}	Byte load time	30	—	100	µs
t_{BLC}	Byte load cycle	0.3	—	30	µs
t_{WC}	WRITE cycle time	—	—	15	ms

<< AC test conditions >>

Output Load : 100 pF + 1 TTL Gate (include jig)
Input Pulse Level : 0.4 V, 2.4 V
Timing Measurement Comparison Level : Input : 0.6 V, 2.2 V
: Output : 0.6 V, 2.2 V
Input Rise and fall : 20 ns

TIMING DIAGRAM



PIN ASSIGNMENT

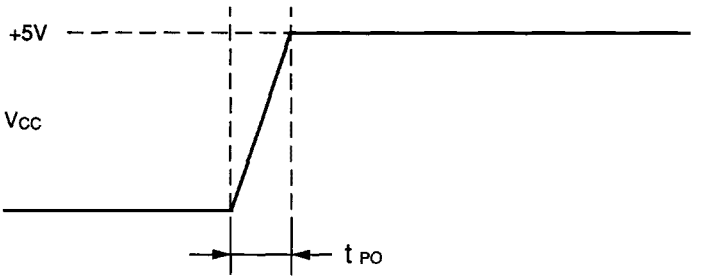
Pin #	Name	Pin #	Name
1	VCC	21	CE
2	VBB**	22	OE
3	A0	23	D0
4	A1	24	D1
5	A2	25	D2
6	A3	26	D3
7	A4	27	D4
8	A5	28	D5
9	A6	29	D6
10	A7	30	D7
11	A8	31	N/C
12	A9	32	N/C
13	A10	33	N/C
14	A11	34	N/C
15	A12*	35	N/C
16	A13*	36	N/C
17	A14*	37	WPOUT***
18	A15*	38	CST**
19	A16*	39	ROM/$\overline{\text{RAM}}$**
20	$\overline{\text{WC}}$	40	GND

Notes: *A12 : 8 KB, 16 KB, 32 KB, 64 KB, 128 KB
*A13 : 16 KB, 32 KB, 64 KB, 128 KB
*A14 : 32 KB, 64 KB, 128 KB
*A15 : 64 KB, 128 KB
*A16 : 128 KB
Unused address lines should be N/C (No Connect).
** : Output signal line. (Connect to VCC or GND inside the card)
Do never use as VCC or GND line.
***WPOUT : NMOS This line is connected to VCC line.
Do never use as VCC line.
CMOS This line is used as RDY/$\overline{\text{BSY}}$ signal.

NOTE

POWER - UP ON VCC

CMOS ONLY



tPO should be greater than 10u Second

Please ensure that power - up time is greater than 10u second, or risk the possibility of data loss.