ISD5216

8 TO 16 MINUTES

VOICE RECORD/PLAYBACK DEVICE

WITH INTEGRATED CODEC

1. GENERAL DESCRIPTION

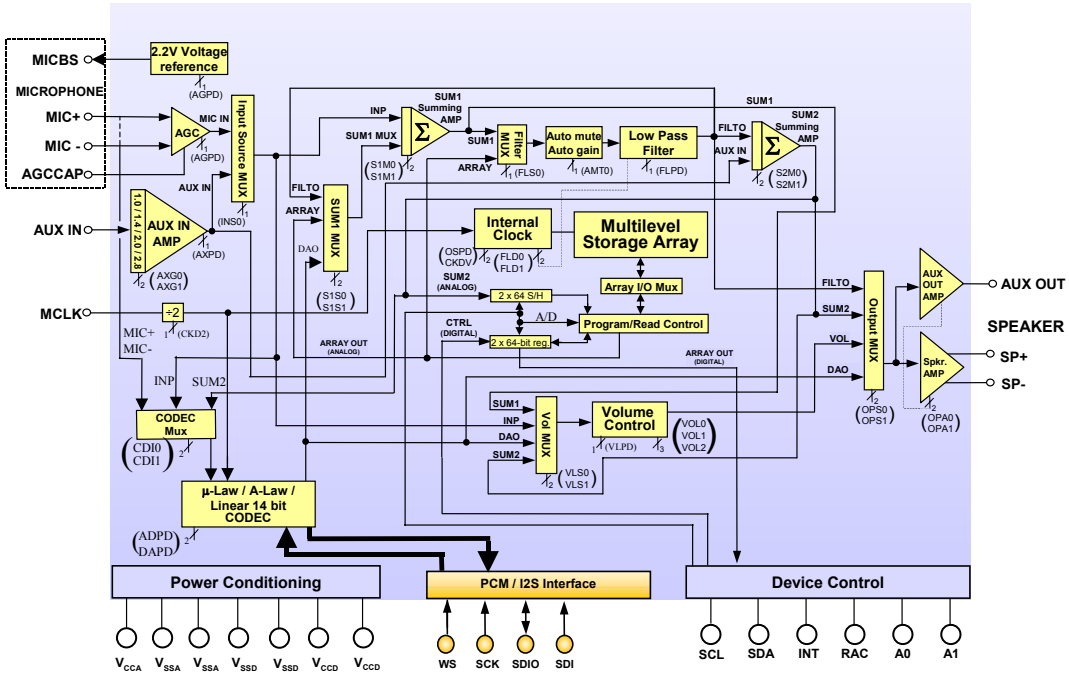
The ChipCorder ISD5216 is an 8 to 16 minute Voice and Data Record and Playback system with integrated Voice band CODEC. The device works on a single 2.7V to 3.3V supply, and has fully integrated system functions, including: AGC, microphone preamplifier, speaker driver, memory and CODEC. The CODEC meets the PCM conformance specification of the G.714 recommendation. Its μ-Law and A-Law compander meets the specification of the ITU-T G.711 recommendation.

2. FEATURES

- Single Supply 2.7 to 3.3 Volt operation
- Voice and digital data record and playback system on a single chip
- Industry-leading sound quality
- Low voltage operation
- Message management
- Fully integrated system functions
- Flexible architecture
- Nonvolatile message storage
- Configurable ChipCorder sampling rates of 4 kHz, 5.3kHz, 6.4 kHz and 8kHz
- 8, 10, 12 and 16 minutes duration
- External or internal Voice recorder clock
- I^2C serial interface (400kHz)
- Configurable analog paths
- 2.2V Microphone Bias Pin
- 100 year message retention (typical)
- 100K analog record cycles (typical)
- 10K digital record cycles (typical)
- Full-duplex (not in I^2S mode) single channel speech CODEC with:
  - External 13.824 MHz, 27.648 MHz, 20.48 MHz or 40.96 MHz master clock
  - I^2S and PCM digital audio interface ports
  - Serial transfer data rate from 64 to 3072 Kbps
  - Short and Long frame sync formats
  - 2s complement and signed magnitude data format
  - Complete μ-Law and A-Law companding
  - Linear 14 bit $\Delta\Sigma$ PCM CODEC-filter for A/D and D/A converter
  - 8 kHz or 44.1 kHz – 48 kHz digital audio sampling rate options
  - Analog receive and transmit gain adjust
  - Configurable setup through the I^2C interface

3. BLOCK DIAGRAM

I5216 Block Diagram



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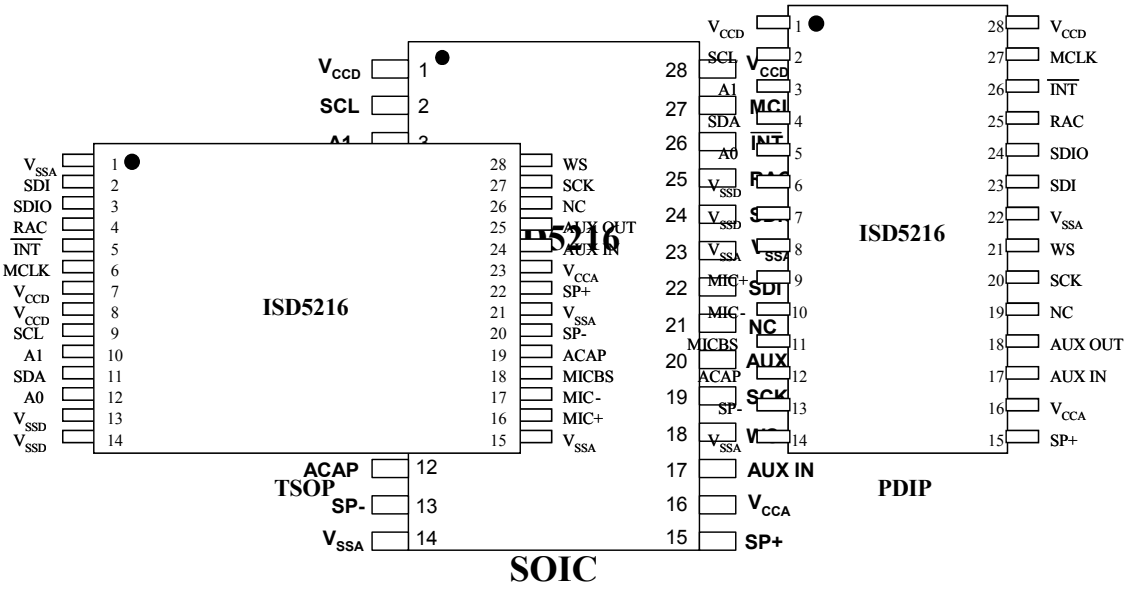
5. PIN CONFIGURATION

ISD5216 Pin Layout



Please note that the pin assignments are different for the PDIP and the SOIC packages.

6. PIN DESCRIPTION

Pin Name	Pin No. 28-pin TSOP	Pin No. 28-pin PDIP	Pin No. 28-pin SOIC	Functionality
RAC	4	25	25	Row Address Clock; an open drain output. The RAC pin goes LOW T_{RACLO}[1] before the end of each row of memory, and returns HIGH at exactly the end of each row of memory.
$\overline{INT}$	5	26	26	Interrupt Output; an open drain output indicating that a set EOM bit has been found during Playback, or that the chip is in an Overflow (OVF) condition. This pin remains LOW until a Read Status command is executed.
MCLK	6	27	27	This pin allows the internal clock of the Voice record/playback system to be externally driven for enhanced timing precision. This pin is grounded for most applications. It is required for the CODEC operation.
SCL	9	2	2	Serial Clock Line is part of the I^2C serial bus. It is used to clock the data into and out of the I^2C interface.
SDA	11	4	4	Serial Data Line is part of the I^2C serial bus. Data is passed between devices on the bus over this line.
A0	12	5	7	Input pin that supplies the LSB for the I^2C Slave Address.
A1	10	3	3	Input pin that supplies the LSB +1 bit for the I^2C Slave Address.
MIC+	16	9	10	Differential positive Input to the microphone amplifier.
MIC-	17	10	9	Differential negative Input to the microphone amplifier.
MICBS	18	11	8	Microphone Bias Voltage
ACAP	19	12	12	AGC Capacitor connection. Required for the on-chip AGC amplifier.
SP+	22	15	15	Differential Positive Speaker Driver Output.
SP-	20	13	13	Differential Negative Speaker Driver Output. When the speaker outputs are in use, the AUX OUT output is disabled.
AUX IN	24	17	17	Auxiliary Input.
AUX OUT	25	18	20	Auxiliary Output. This is one the analog outputs for the device. When this output is in use, the SP+ and SP- outputs are disabled.
SDI	2	23	22	Serial Digital Audio PCM Input.
SDIO	3	24	24	Serial Digital Audio PCM Output or I^2S Input/Output.
WS	28	21	18	Digital audio PCM Frame sync (FS) or I^2S Word Sync (WS).
SCK	27	20	19	Digital audio PCM or I^2S Serial Clock.
V_{CCD}	7,8	1,28	1,28	Positive Digital Supply pins. These pins carry noise generated by internal clocks in the chip. They must be carefully bypassed to Digital Ground to ensure correct device operation.
V_{SSD}	13,14	6,7	5,6	Digital Ground pins.
V_{SSA}	1,15,21	8,14,22	11,14,23	Analog Ground pins.
V_{CCA}	23	16	16	Positive Analog Supply pin. This pin supplies the low level audio sections for the device. It should be carefully bypassed to Analog Ground to ensure correct device operation.
NC	26	19	21	No Connection

[1] See parameters section of the datasheet.

7. FUNCTIONAL DESCRIPTION

The ISD5216 ChipCorder Product provides high quality, fully integrated, single-chip Record/Playback solutions for 8- to 16-minute messaging applications that are ideal for use in PBX systems, cellular phones, automotive communications, GPS/navigation systems, and other portable products. The ISD5216 product is an enhancement to the ISD5116 architecture, providing: 1) A full-duplex Voice CODEC with μ-Law and A-Law compander using the I^2S and PCM interface ports; 2) A 2.2V microphone bias supply for reduced noise coupling. This supply can also be used to power down the external microphone with the system.

Analog functions and audio gating have also been integrated into the ISD5216 product to allow for easy interfacing with integrated chip sets on the market. Audio paths have been designed to enable full duplex conversation record, voice memo and answering machine (including outgoing message playback).

Logic Interface Options of 2.0V and 3.0V are supported by the ISD5216 to accommodate both portable communication (2.0- and 3.0-volt required) and automotive product customers (5.0-volt required).

Like other ChipCorder products, the ISD5216 integrates the sampling clock, anti-aliasing and smoothing filters, and multi-level storage array on a single chip. For enhanced voice features, the ISD5216 eliminates external circuitry by integrating automatic gain control (AGC), a power amplifier/speaker driver, volume control, summing amplifiers, analog switches, and a Voice CODEC. Input level adjustable amplifiers are also included, providing a flexible interface for multiple applications.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Winbond's patented multilevel storage technology. Voice and audio signals are stored directly into solid-state memory in their natural, uncompressed form, providing superior quality voice and music reproduction.

SPEECH/SOUND QUALITY

The ISD5216 ChipCorder product can be software configured to operate at 4.0, 5.3, 6.4, and 8.0 kHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration decreases the sampling frequency and bandwidth, which affects sound quality. The "*Input Sample Duration*" table below compares filter pass band and product durations.

DURATION

To meet end-system requirements, the ISD5216 device is a single-chip solution, which provides 8 to 16 minutes of voice record and playback, depending on the sample rates defined by the customer's software.

Input Sample Rate to Duration Input Sample

Rate (kHz)	Duration[1] (Minutes)	Typical Filter Pass Band (kHz)
8.0	8 min 3 sec	3.7
6.4	10 min 4 sec	2.9
5.3	12 min 9 sec	2.5
4.0	16 min 6 sec	1.8

[1] Minus any pages selected for digital storage

FLASH STORAGE

One of the benefits of Winbond's ChipCorder technology is the use of on-chip nonvolatile memory, which provides zero-power message storage. A message is retained for up to 100 years (typically) without power. In addition, the device can be re-recorded over 10,000 times (typically) for digital messages and over 100,000 times (typically) for analog messages.

Memory space can be allocated to either digital or analog storage, when recording. The system micro controller stores this information in the Message Address Table.

MICROCONTROLLER INTERFACE

The **ISD5216** is controlled through an I^2C 2-wire interface. This synchronous serial port allows commands, configurations, address data, and digital data to be loaded to the device, while allowing status, digital data and current address information to be read back from the device. In addition to the serial interface, two other pins can be connected to the microcontroller for enhanced interface: the RAC timing pin and the $\overline{INT}$ pin for interrupts to the controller. Communications with all of the internal registers is through the serial bus, as well as digital memory Read and Write operations.

PROGRAMMING

The ISD5216 series is also ideal for playback-only applications, whereas single or multiple messages may be played back when desired. Playback is controlled through the I^2C port. Once the desired message configuration is created, duplicates can easily be generated via a Winbond or third-party programmer. For more information on available application tools and programmers, please see the Winbond web site at http://www.winbond-usa.com/.

AUDIO PATHS

The ISD5216 has extremely powerful audio routing functionality where all audio signals can be routed and multiplexed to multiple destinations. A few examples are

- Simultaneous recording of microphone input and CODEC DAC output for recording both parties of a phone call.

7.1. MEMORY ORGANIZATION

The ISD5216 memory array is arranged as 1888 rows (or pages) of 2048 bits, for a total memory of 3,866,624 bits. The primary addressing for the 2048 pages is handled by 11 bits of address data in the analog mode. At the 8 kHz sample rate, each page contains 256 milliseconds of audio. Thus, at 8 kHz there is actually room for 8 minutes and 3 seconds of audio.

A memory page is 2048 bits organized as thirty-two 64-bit "blocks" when used for digital storage. The contents of a page are either analog or digital. This is determined by instruction (op code) at the time the data is written. A record of what is analog and what is digital, and where, is stored by the system microcontroller in the message address table (MAT). The MAT is a table kept in the microcontroller memory that defines the status of each message “block.” It can be stored back into the ISD5216 if the power fails or the system is turned off. Use of this table allows for efficient message management. Segments of messages can be stored wherever there is available space in the memory array.

When a page is used for analog storage, the same 32 blocks are present, but there are 8 EOM (End-of-Message) markers. This means that for each 4 blocks there is an EOM marker at the end. Thus, when recording, the analog recording will stop at any one of eight positions. At 8 kHz, this results in a resolution of 32 msec when ENDING an analog recording. Beginning an analog recording is limited to the 256 msec resolution provided by the 11-bit address. A recording does not immediately stop when the Stop command is issued, but continues until the 32-millisecond block is filled. Then a bit is placed into the EOM memory to develop the interrupt that signals a message is finished playing in the Playback mode.

Digital data is sent and received, serially, over the I^2C interface. The data is serial-to-parallel converted and stored in one of two alternating (commutating) 64-bit shift registers. When an input register is full, it becomes the register that is parallel written into the array. The prior write register becomes the new serial input register. A mechanism is built in to ensure there is always a register available for storing new data.

Storing data in the memory is accomplished by accepting data, one byte at a time, and issuing an acknowledgement. If data is coming in faster than it can be written, then the chip will not issue an acknowledgement to the host microcontroller until it is ready.

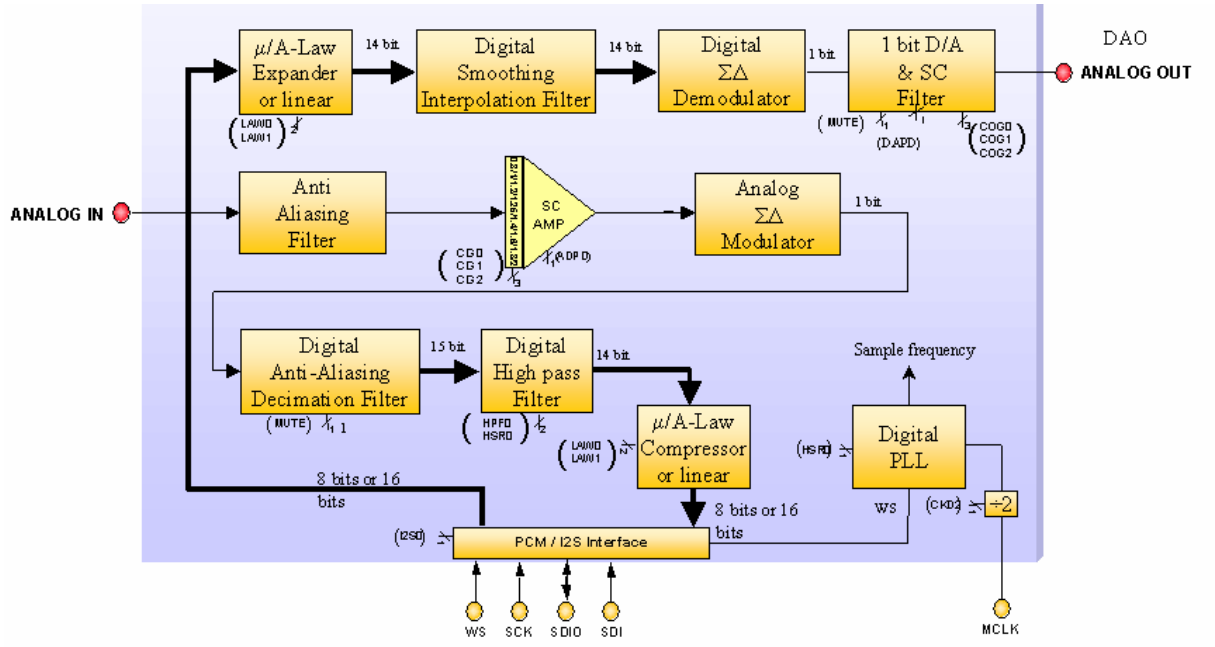
The read mode is the opposite of the write mode. Data is read into one of two 64-bit registers from the array and serially sent to the I^2C port. (See Digital Mode on page 26 for details).

7.2. CODEC

The CODEC built into the ISD5216 supports both the I^2S and PCM digital interface using μ-Law and A-Law companding as well as 2’s complement and signed magnitude data. The CODEC meets the PCM conformance specification of the G.714 recommendation. Its μ-Law and A-Law compander meets the specification of the ITU-T G.711 recommendation.

The CODEC operates in full duplex in PCM mode and half duplex in I^2S mode. Operating the CODEC requires an external master clock running at 13.824 MHz, 20.48 MHz, 27.648 MHz or 40.96 MHz. This provides a sampling frequency ranging from 8kHz to 48kHz.

The following diagram shows the functional blocks in the CODEC:



7.2.1. Analog Input to Digital Output Path

A 200 kHz anti-aliasing filter processes the analog input signal before entering the amplifier for the A/D converter. The gain of this amplifier is adjustable through the configuration registers bits (CIG2 – CIG0) for a gain from 0.80 to 2.00.

The Sigma Delta modulator is a Linear 14 bit ΣΔ modulator running at a sampling frequency determined by the external clock input and the internal clock dividers (CKD2, CKDV). The standard telecom frequency of 8kHz and digital audio of 44.1kHz and 48 kHz as well as intermediate frequencies as shown in the table on the next page are supported. The A/D converter can be turned off to save power and reduce noise by setting the A/D power down bit (ADPD).

The A/D converter feeds a 3.4 kHz digital anti aliasing filter which can be muted to suppress noise, the mute bit controls both the A/D and D/A filter simultaneously. The following high pass filter is enabled by bit (HPF0) in the configuration register. The High Sampling Rate bit (HSR0) needs to be set to enable operation at 44.1kHz – 48 kHz.

The digital audio signal can be companded using μ - Law and A-Law companding or go to the output uncompressed using 2's complement or signed magnitude output selected with bits (LAW1 – LAW0) in the configuration registers.

Finally the digital output interface is selected to be either full-duplex PCM or half duplex I^2S using the interface selector bit (I^2S0) in the configuration register. The PCM interface uses the SDIO and SDI pins, the half-duplex I^2S format uses the SDIO pin as both input and output.

7.2.2. Digital Input to Analog Output Path

The digital input interface must be selected to either PCM or I^2S using the interface selector bit (I^2S0) in the configuration register. The compression format must also be selected with bits (LAW1 – LAW0) in the configuration registers.

The external clock input signal on pin MCLK and the internal clock dividers must be set to values supporting the selected digital input signal.

The digital smoothing and interpolation filter runs at 3.4 kHz and feeds the ΣΔ D/A converter that can be switched off to conserve power and reduce noise using the D/A power down bit (DAPD).

The analog output amplifier gain is controlled from configuration registers bits (COG2 – COG0) from -8 dB to +6 dB.

7.2.3. CODEC External Clock Configuration

The ISD5216 has two Master Clock configuration bits that allow four possible Master Clock frequencies. Bits CKD2 and CKDV set the Master Clock Division ratios. These are bits D12 and D8 of CFG2, respectively. The combination of these bits, with the sample rate bit HSR0, also set the CODEC sample frequency as shown in the following table.

Master Clock Possible Settings

F_{MCLK}	HSR0 (D5) (CFG2)	CKD2 (D12) (CFG2)	CKDV (D8) (CFG2)	F_{SCODEC}
13.824 MHz	0	0	0	8 kHz
20.48 MHz	0	0	1	11.852 kHz*
27.648 MHz	0	1	0	8 kHz
40.96 MHz	0	1	1	11.852 kHz*
13.824 MHz	1	0	0	32 kHz*
20.48 MHz	1	0	1	44.1 - 48 kHz
27.648 MHz	1	1	0	32 kHz*
40.96 MHz	1	1	1	44.1-48 kHz

**not tested*

7.2.4. ChipCorder Analog Array Sampling Frequency With External Clock

If an external master clock is used, the clock dividers must be set according to the following table to get the filter cut-off frequency and sample rate setup correctly. The duty cycle on the input clock is not critical when CKD2 is set to ONE as the clock is immediately divided by two internally. See the *Analog Structure (Right Half)* description on page 32.

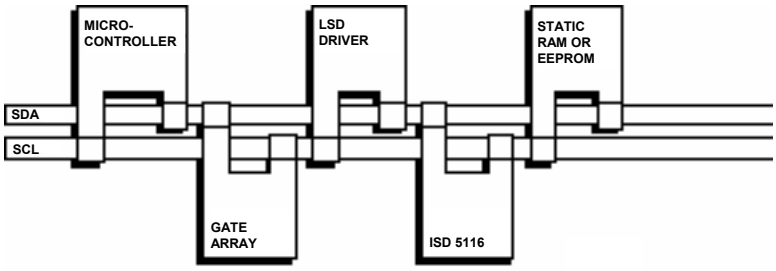
F_{MCLK}	FLD 1	FLD0	CKD2	CKDV	Sample Rate	Filter Knee
13.824 MHz	0	0	0	0	8.0 kHz	3.7 kHz
20.48 MHz	0	0	0	1	8.0 kHz	3.7 kHz
27.648 MHz	0	0	1	0	8.0 kHz	3.7 kHz
40.96 MHz	0	0	1	1	8.0 kHz	3.7 kHz
13.824 MHz	0	1	0	0	6.4 kHz	2.9 kHz
20.48 MHz	0	1	0	1	6.4 kHz	2.9 kHz
27.648 MHz	0	1	1	0	6.4 kHz	2.9 kHz
40.96 MHz	0	1	1	1	6.4 kHz	2.9 kHz
13.824 MHz	1	0	0	0	5.3 kHz	2.5 kHz
20.48 MHz	1	0	0	1	5.3 kHz	2.5 kHz
27.648 MHz	1	0	1	0	5.3 kHz	2.5 kHz
40.96 MHz	1	0	1	1	5.3 kHz	2.5 kHz
13.824 MHz	1	1	0	0	4.0 kHz	1.8 kHz
20.48 MHz	1	1	0	1	4.0 kHz	1.8 kHz
27.648 MHz	1	1	1	0	4.0 kHz	1.8 kHz
40.96 MHz	1	1	1	1	4.0 kHz	1.8 kHz

7.3. I²C INTERFACE

The I²C interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the interface bus is not busy.

7.3.1. System configuration

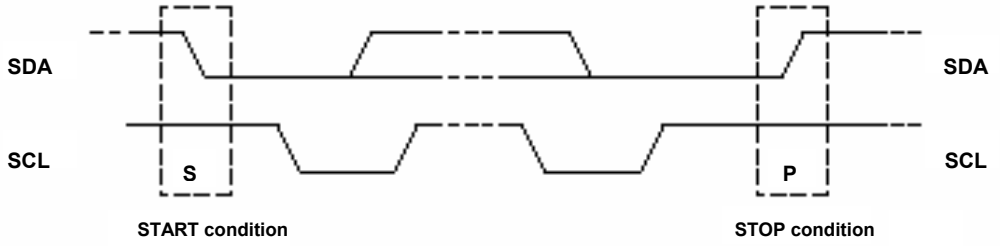
A device generating a message is a 'transmitter'; a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices that are controlled by the master are the 'slaves'.



Example of an I²C-bus configuration using two microcontrollers

7.3.2. Start and stop conditions

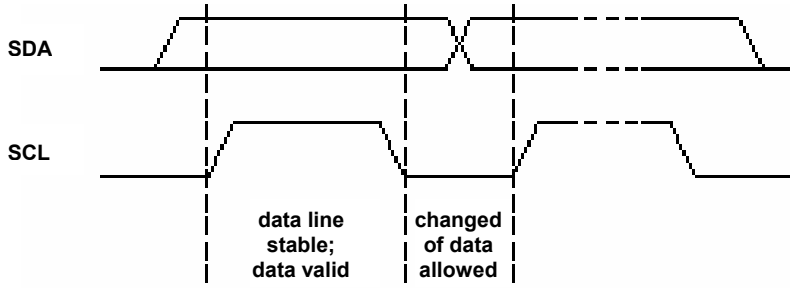
Both data and clock lines remain HIGH when the interface bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P)



Definition of START and STOP conditions

7.3.3. Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as a control signal. The same timing applies to both read and write.

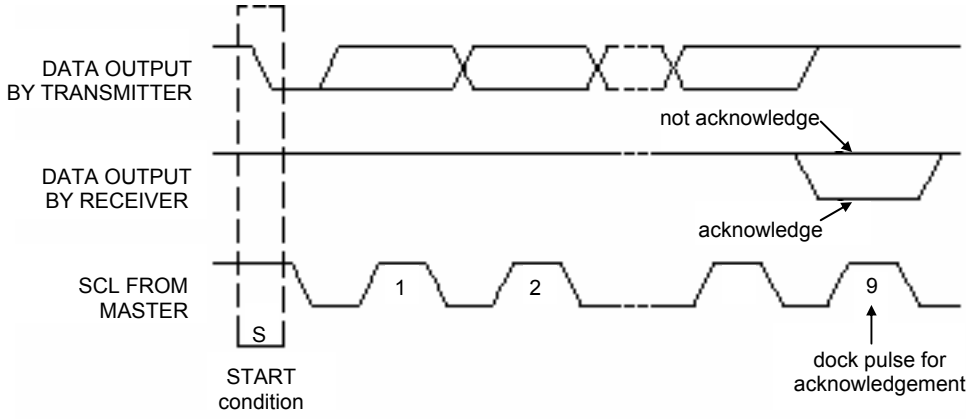


Bit transfer on the I²C-Bus

7.3.4. ACKNOWLEDGE

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the interface bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. In addition, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.



Acknowledge on the I²C-bus

7.3.5. Additional ISD5216 flow control

The I²C Interface in the ISD5216 differs from the standard implementation in the way the SCL line is also used for flow control. The ISD5216 will hold the clock line low until it is ready to accept another command/data. The SCL line must be implemented as a bi-directional line like the SDA line.

For example, the sequence of sending the slave address will be as follows:

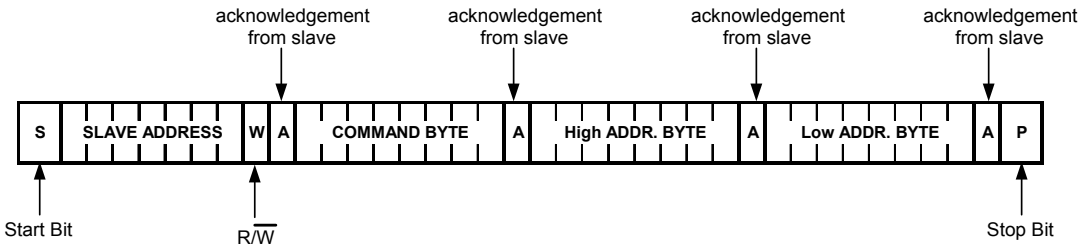
1. Send one byte 10000000 {Slave Address, R/W = 0} 80h.
2. Wait for slave to acknowledge (ACK)
3. Next time the clock is pulled high by the master, wait for SCL to actually go high.

7.3.6. I²C Protocol Addressing

Since the I²C protocol allows multiple devices on the bus, each device must have an address. This address is known as a "Slave Address". A Slave Address consists of 7 bits, followed by a single bit that indicates the direction of data flow. This single bit is 1 for a Write cycle, which indicates the data is being sent from the current bus master to the device being addressed. This single bit is a 0 for a Read cycle, which indicates that the data is being sent from the device being addressed to the current bus master.

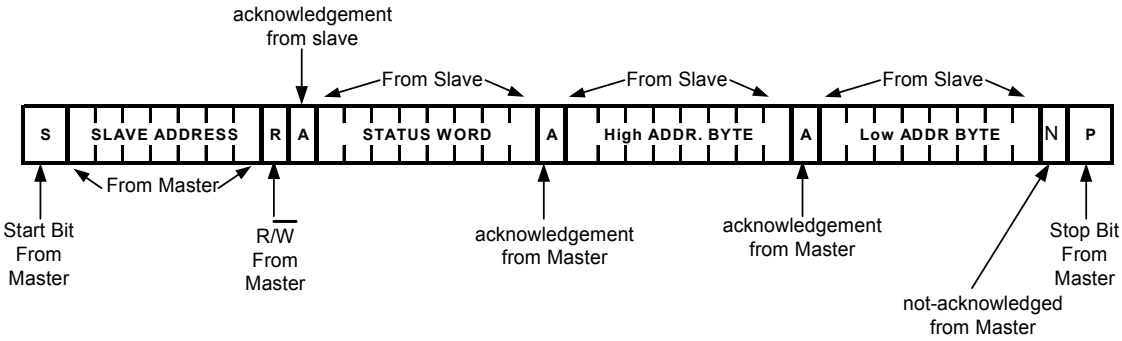
Before any data is transmitted on the I²C interface, the current bus master must address the slave it wishes to transfer data to or from. The Slave Address is always sent out as the 1st byte following the Start Condition sequence. An example of a Master transmitting an address to a ISD5216 slave is shown below. In this case, the Master is writing data to the slave and the R/W bit is "0", i.e. a Write cycle. All the bits transferred are from the Master to the Slave, except for the indicated Acknowledge bits.

Master Transmits to Slave Receiver (Write) Mode



A common procedure in the ISD5216 is the reading of the Status Bytes. The Read Status condition in the ISD5216 is triggered when the Master addresses the chip with its proper Slave Address, immediately followed by the R/W bit set to a "0" and without the Command Byte being sent. This is an example of the Master sending to the Slave, immediately followed by the Slave sending data back to the Master. The "N" not-acknowledge cycle from the Master ends the transfer of data from the Slave.

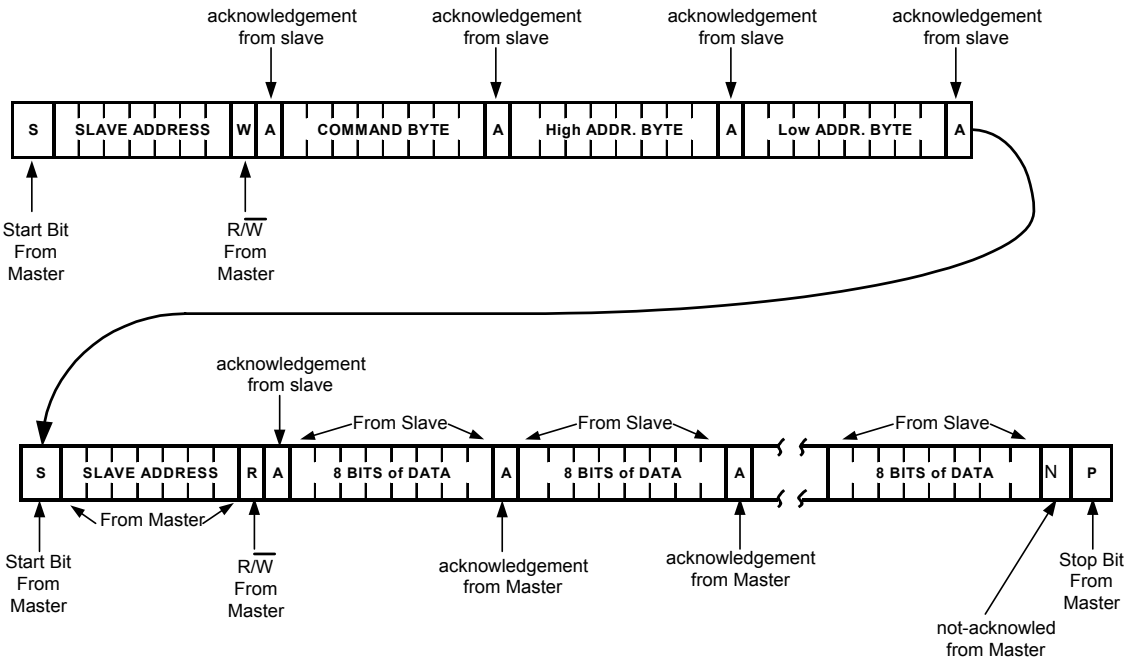
Master Reads from Slave immediately after first byte (Read Mode)



Another common operation in the ISD5216 is the reading of digital data from the chip's memory array at a specific address. This requires the I^2C interface Master to first send an address to the ISD5216 Slave device, and then receive data from the Slave in a single I^2C operation. To accomplish this, the data direction R/W bit must be changed in the middle of the command. The following example shows the Master sending the Slave address, then sending a Command Byte and 2 bytes of address data to the ISD5216, and then immediately changing the data direction and reading some number of bytes from the chip's digital array. An unlimited number of bytes can be read in this operation. The "N" not-acknowledge cycle from the Master forces the end of the data transfer from the Slave. The following example details the transfer explained in the section on page 22 of this datasheet.

Master Reads from the Slave after setting data address in Slave

(Write data address, READ Data)



7.3.7. I²C Slave Address

The ISD5216 has a 7 bit slave address of <100 00xy> where x and y are equal to the state, respectively, of the external address pins A1 and A0. Because all data bytes are required to be 8 bits, the LSB of the address byte is the Read/Write selection bit that tells the slave whether to transmit or receive data. Therefore, there are eight possible slave addresses for the ISD5216. To use more than four ISD5216 devices in an application requires some external switching of the I²C link.

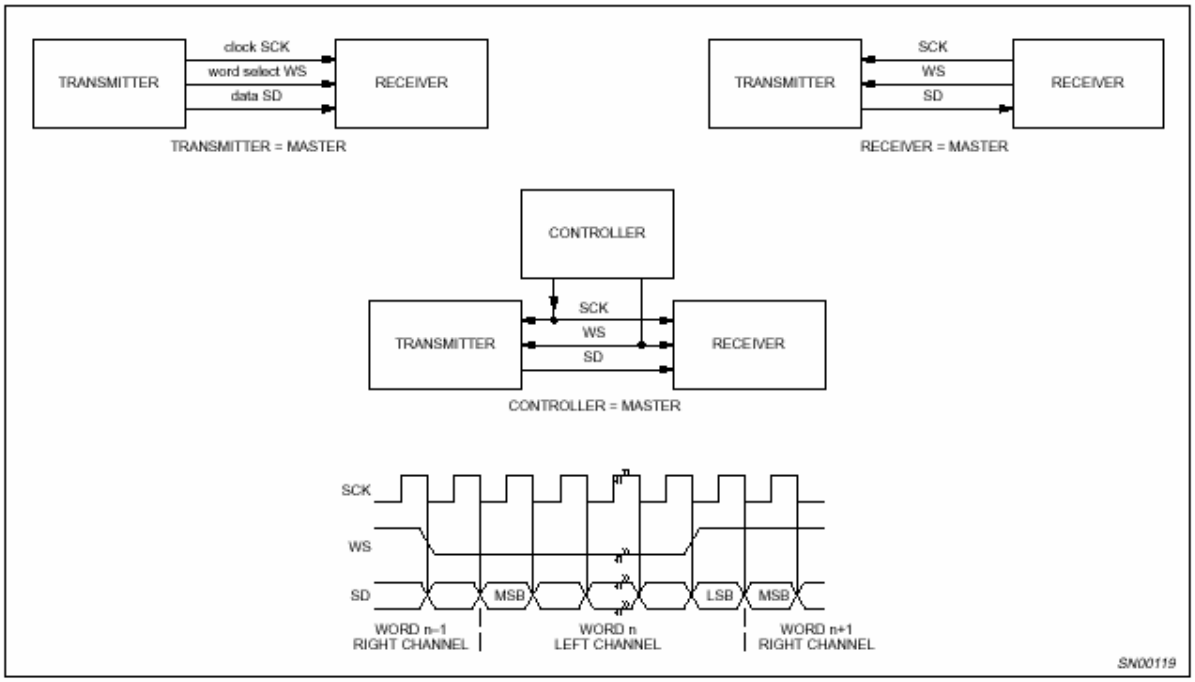
A1	A0	Slave Address	R/W\ Bit	HEX Value
0	0	<100 00 00>	0	80
0	1	<100 00 01>	0	82
1	0	<100 00 10>	0	84
1	1	<100 00 11>	0	86
0	0	<100 00 00>	1	81
0	1	<100 00 01>	1	83
1	0	<100 00 10>	1	85
1	1	<100 00 11>	1	87

7.4. I2S SERIAL INTERFACE

As shown in the following figure, the bus has three lines:

- continuous serial clock (SCK)
- word select (WS)
- serial data (SDIO)and the device generating SCK and WS is the master.

Simple System Configurations and Basic Interface Timing



7.4.1. Serial Data

Serial data is transmitted in two's complement with the MSB first. The MSB is transmitted first because the transmitter and receiver may have different word lengths. It isn't necessary for the transmitter to know how many bits the receiver can handle, nor does the receiver need to know how many bits are being transmitted.

When the system word length is greater than the transmitter word length, the word is truncated (least significant data bits are set to '0') for data transmission. If the receiver is sent more bits than its word length, the bits after the LSB are ignored. On the other hand, if the receiver is sent fewer bits than its word length, the missing bits are set to zero internally. And so, the MSB has a fixed position, whereas the position of the LSB depends on the word length. The transmitter always sends the MSB of the next word one clock period after the WS changes.

Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when

transmitting data that is synchronized with the leading edge (see the timing specifications at the back of this data sheet).

Note that the specifications are defined by the transmitter speed. The specification of the receiver has to be able to match the performance of the transmitter.

7.4.2. Word Select

The word select line indicates the channel being transmitted:

• WS = 0; channel 1 (left)

• WS = 1; channel 2 (right)

WS may change either on a trailing or leading edge of the serial clock, but it doesn't need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The WS line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word (see figure *Timing for I^2S Transmitter* on previous page.)

7.4.3. Timing

In the I^2S format, any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input. This means, taking into account the propagation delays between master clock and the data and/or word-select signals, the total delay is simply the sum of:

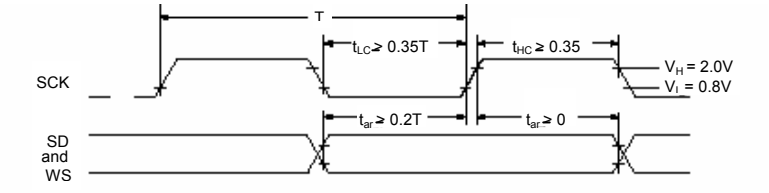
• the delay between the external (master) clock and the slave's internal clock; and

• the delay between the internal clock and the data and/or word-select signals.

For data and word-select inputs, the external to internal clock delay is of no consequence because it only lengthens the effective set-up time (see figure *Timing for I^2S Transmitter* on previous page.) The major part of the time margin is to accommodate the difference between the propagation delay of the transmitter, and the time required to set up the receiver.

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device. This means that higher data rates can be used in the future.

Timing for I^2S Receiver



T = clock period

T_R = minimum allowed clock period for transmitter

$T > T_R$

Note that the specifications are defined by the transmitter speed. The specification of the receiver has to be able to match the performance of the transmitter.

7.5. CONTROL REGISTERS

The ISD5216 is controlled by loading commands to, or reading commands from the internal command, configuration and address registers. The Command byte sent is used to start and stop recording, write or read digital data and perform other functions necessary for the operation of the device.

7.5.1. Command Byte

Control of the ISD5216 is implemented through an 8-bit command byte that is sent after the 7-bit device address and the 1-bit Read/Write selection bit. The 8 bits are:

- Global power up bit (PU)
- DAB bit: determines whether device is performing an analog or digital function
- 3 function bits: these determine which function the device is to perform in conjunction with the DAB bit.
- 3 register address bits: these determine if and when data is to be loaded to a register

C7	C6	C5	C4	C3	C2	C1	C0
PU	DAB	FN2	FN1	FN0	RG2	RG1	RG0
	Function Bits				Register Bits		

7.5.2. Function Bits

The command byte function bits are detailed in the table to the right. C6, the DAB bit, determines whether the device is performing an analog or digital function. The other bits are decoded to produce the individual commands. Note that not all decode combinations are currently used; they are reserved for future use. Out of 16 possible codes, the ISD5216 uses 7 for normal operation. The other 9 are No Ops.

Command Bits				Function
C6	C5	C4	C3	
DAB	FN2	FN1	FN0	
0	0	0	0	STOP (or do nothing)
0	1	0	1	Analog Play
0	0	1	0	Analog Record
0	1	1	1	Analog MC
1	1	0	0	Digital Read
1	0	0	1	Digital Write
1	0	1	0	Erase (row)

7.5.3. Register Bits

The register load may be used to modify a command sequence (such as load an address) or used with the null command sequence to load a configuration or test register. Not all registers are accessible to the user. [The remaining three codes are No Ops.]

RG2	RG1	RG0	Function
C2	C1	C0	
0	0	0	No action
0	0	1	Load Address
0	1	0	Load CFG0
0	1	1	Load CFG1
1	0	1	Load CFG2

7.5.4. OPCODE Command Byte Table

		Pwr	Function Bits				Register Bits		
OPCODE	**HEX**	**PU**	**DAB**	**FN2**	**FN1**	**FN0**	**RG2**	**RG1**	**RG0**
COMMAND BIT NUMBER	**CMD**	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
POWER UP	80	1	0	0	0	0	0	0	0
POWER DOWN	00	0	0	0	0	0	0	0	0
STOP (DO NOTHING) STAY ON	80	1	0	0	0	0	0	0	0
STOP (DO NOTHING) STAY OFF	00	0	0	0	0	0	0	0	0
LOAD ADDRESS	81	1	0	0	0	0	0	0	1
LOAD CFG0	82	1	0	0	0	0	0	1	0
LOAD CFG1	83	1	0	0	0	0	0	1	1
LOAD CFG2	85	1	0	0	0	0	1	0	1
RECORD ANALOG	90	1	0	0	1	0	0	0	0
RECORD ANALOG @ ADDR	91	1	0	0	1	0	0	0	1
PLAY ANALOG	A8	1	0	1	0	1	0	0	0
PLAY ANALOG @ ADDR	A9	1	0	1	0	1	0	0	1
MSG CUE ANALOG	B8	1	0	1	1	1	0	0	0
MSG CUE ANALOG @ ADDR	B9	1	0	1	1	1	0	0	1
ERASE DIGITAL PAGE	D0	1	1	0	1	0	0	0	0
ERASE DIGITAL PAGE @ ADDR	D1	1	1	0	1	0	0	0	1
WRITE DIGITAL	C8	1	1	0	0	1	0	0	0
WRITE DIGITAL @ ADDR	C9	1	1	0	0	1	0	0	1
READ DIGITAL	E0	1	1	1	0	0	0	0	0
READ DIGITAL @ ADDR	E1	1	1	1	0	0	0	0	1
READ STATUS REGISTER	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

7.5.5. Power-up

The ISD5216 must be powered up before sending any other commands. Wait for Tpud time before sending the next command.

7.5.6. Read Status

When the device is polled with the Read Status command, it will return three bytes of data. The first byte is the status byte, the next is the upper address byte and the last is the lower address byte. The status register is one byte long and its bit function is:

BIT#	NAME	FUNCTION
7	EOM	Indicates whether an EOM interrupt has occurred.
6	OVF	Indicates whether an overflow interrupt has occurred.
5	READY	Indicates the internal status of the device – if READY is LOW no new commands should be sent to device.
4	PD	Device is powered down if PD is HIGH.
3	PRB	Play/Record mode indicator. HIGH=Play/LOW=Record.
2 1 0	DEVICE_ID	An internal device ID. This is 001 for the ISD5216.

The lower address byte will always return the block address bits as zero, either in digital or analog mode.

It is good practice to read the status register after a Write or Record operation to ensure that the device is ready to accept new commands. Depending upon the design and the number of pins available on the controller, the polling overhead can be reduced. If $\overline{INT}$ and RAC are tied to the microcontroller, the controller does not have to poll as frequently to determine the status of the ISD5216

7.5.7. Attaching an Address to a Command

In the I^2C write mode, the device can accept data sent after the command byte. If a register load option is selected, the next two bytes are loaded into the selected register. The format of the data is MSB first, as specified by the I^2C standard. Thus to load DATA<15:0> into the device, DATA<15:8> is sent first, the byte is acknowledged, and DATA<7:0> is sent next. The address register consists of two bytes. The format of the address is as follows:

ADDRESS<15:0> = PAGE_ADDRESS<10:0>, BLOCK_ADDRESS<4:0>

If an analog function is selected, the block address bits must be set to 00000. Digital Read and Write are block addressable.

7.5.8. Playback Mode

The command sequence for an analog playback operation from a given address is the Slave Address (80h), the Command Byte (A9h) for Play Analog @ Address, and the two address bytes. If The Play Analog (A8h) is sent, playback starts from the current address pointer. The current address pointer is returned when the three status bytes are read.

7.5.9. Record Mode

The command sequence for an Analog Record is a four byte sequence consisting of the Slave Address (80h), the Command Byte (91h) for Record Analog @ Address, and the two address bytes. If The Record Analog (90h) is sent, recording starts from the current address pointer.

7.5.10. Message Cueing

Message cueing allows the user to skip through messages, without having to know the actual physical location of each message. This operation is used during playback. In this mode, the messages are skipped 512 times faster than in normal playback mode. This operation will stop when an EOM marker is reached. Then, the internal address counter will be pointing to the next message.

7.6. DIGITAL MODE

7.6.1. Writing Data

The Digital Write function allows the user to select a portion of the array to be used as digital memory. The partition between analog and digital memory is left up to the user. A page can only be either Digital or Analog, but not both. The minimum addressable block of memory in the digital mode is 1 block, or 64 bits, when reading or writing. The address sent to the device is the 11-bit row (or page) address with the 5-bit scan (or block) address. However, one must send a Digital Erase before attempting to change digital data on a page. This means that even when changing only one of the 32 blocks, all 32 will need to be rewritten to the page.

After the address is entered, the data is sent in one-byte packets followed by an I^2C acknowledge generated by the chip. Data for each block is sent MSB first. The data transfer is ended when the master generates an I^2C STOP condition. If only a partial block of data is sent before the STOP condition, zero is “written” in the remaining bytes; that is, they are left at the erase level. An erased page (row) will be read as all zeros. The device can buffer up to two blocks of data.

If the device is unable to accept more data due to the internal write process, the SCL line will be held LOW indicating, to the master, to halt data transfer. If the device encounters an overflow condition, it will respond by generating an interrupt condition and an I^2C Not Acknowledge signal after the last valid byte of data. Once data transfer is terminated, the device needs up to two cycles (64 us) to complete its internal write cycle before another command is sent. If an active command is sent before the internal cycle is finished, the ISD5216 will hold SCL LOW until the current command is finished.

7.6.2. Reading Data

The Digital Read command utilizes the combined I^2C command format. That is, a command is sent to the chip using the write data direction. Then the data direction is reversed by sending a repeated start condition and the slave address with R/W set to one. After this, the slave device (ISD5216) begins to send data to the master until the master generates a Not Acknowledge. If the part encounters an overflow condition, the INT pin is pulled LOW. No other communication with the master is possible due to the master generating ACK signals.

As with Digital Write, Digital Read can be done a “block” at a time. Thus, only 64 bits need to be read in each Digital Read command sequence.

7.6.3. Erasing Data

The Digital Erase command can only erase an entire page at a time. This means that the D0 or D1 command only needs to include the 11-bit page address; the 5-bit for block address are left at 00000.

Once a page has been erased, each block may be written separately, 64 bits at a time. But, if a block has been previously written, then the entire page of 2048 bits must be erased in order to re-write (or change) a block.

While erasing data, the RAC pin will have a pulse at the end of each erased page, when the stop erase command is sent, the device will stop erasing at the end of the current page. To erase a single page, the stop command should be sent immediately after the start erase command. To erase multiple pages, count pulses on the RAC pin and send the stop command after n-1 RAC pulses have been detected where n is the number of pages to erase.

A sequence might look like:

- read the entire page
- store it in RAM
- change the desired bit(s)
- erase the page
- write the new data from RAM to the entire page

7.6.4. Load Configuration Registers

To load the configuration registers, send the LOAD CFG command followed by the two configuration bytes with the most significant byte first.

The following tables provide a summary of the bits. There are three configuration registers: CFG0, CFG1 and CFG2. Thus, there are six 8-bit bytes to be loaded during the set-up of the device.

CFG0

Bit no.	Signal	Description
D0 (LSB)	VLPD	Power down the Volume Control.
D1	OPA0	Power down Speaker driver and/or Auxiliary output.
D2	OPA1	Power down Speaker driver and/or Auxiliary output.
D3	OPS0	Select speaker output multiplexer.
D4	OPS1	Select speaker output multiplexer.
D5	CDI0	Analog to digital converter input selector.
D6	CDI1	Analog to digital converter input selector.
D7	AMT0	Compress the filter signal.
D8	OSPD	Power down the internal ChipCorder oscillator.
D9	INS0	Select Microphone input or Auxiliary input.
D10	AXPD	Power down Auxiliary input amplifier.
D11	AXG0	Auxiliary input amplifier gain setting.
D12	AXG1	Auxiliary input amplifier gain setting.
D13	CIG0	Input gain setting for the Analog to digital converter.
D14	CIG1	Input gain setting for the Analog to digital converter.
D15 (MSB)	CIG2	Input gain setting for the Analog to digital converter.

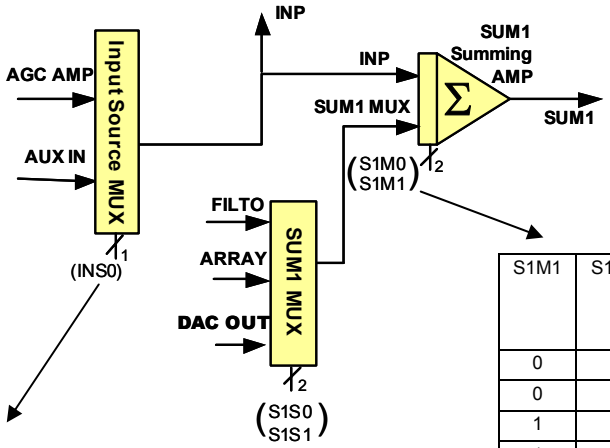
CFG1

Bit no.	Signal	Description
D0 (LSB)	AGPD	Power down the Microphone AGC
D1	FLPD	Power down the Filter
D2	FLD0	Set the duration and sample rate of the ChipCorder
D3	FLD1	Set the duration and sample rate of the ChipCorder
D4	FLS0	Select the filter input signal
D5	S2M0	Select Sum Amplifier 2 input
D6	S2M1	Select Sum Amplifier 2 input
D7	S1M0	Select Sum Amplifier 1 input
D8	S1M1	Select Sum Amplifier 1 input
D9	S1S0	Select Sum Amplifier 1 multiplexer
D10	S1S1	Select Sum Amplifier 1 multiplexer
D11	VOL0	Volume Control Setting
D12	VOL1	Volume Control Setting
D13	VOL2	Volume Control Setting
D14	VLS0	Select Volume Control input
D15 (MSB)	VLS1	Select Volume Control input

CFG2

Bit no.	Signal	Description
D0 (LSB)	ADPD	Power down the Analog to Digital converter
D1	DAPD	Power down the Digital to Analog converter
D2	LAW0	Select digital μ-Law or A-Law input/output format
D3	LAW1	Select digital μ-Law or A-Law input/output format
D4	I2S0	Select the I2S interface
D5	HSR0	Enable the high sample rate mode
D6	HPF0	Enable High Pass Filter
D7	MUTE	Mute the CODEC A/D and D/A path
D8	CKDV	Divide MCLK by 2560 or 1728 for 8 kHz ChipCorder sample rate
D9	COG0	Output gain setting for the Digital to Analog converter
D10	COG1	Output gain setting for the Digital to Analog converter
D11	COG2	Output gain setting for the Digital to Analog converter
D12	CKD2	Divide MCLK frequency by 2 or 1
D13	-	Reserved
D14	-	Reserved
D15 (MSB)	-	Reserved

7.7. ISD5216 ANALOG STRUCTURE (LEFT HALF) description



S1M1	S1M0	This summing amp allows the signal from the input mux or sum 1 mux to be selected or added together. Set the amp to OFF to switch off completely
0	0	BOTH
0	1	SUM1 MUX ONLY
1	0	INP Only
1	1	POWER DOWN

INSO	Select whether to send the AUX input or the microphone signal to the summing amp
0	AGC AMP
1	AUX IN AMP

S1S1	S1S0	Select whether to send the FILTO signal, the MLS playback signal or the output of the CODEC DAC to the summing amp. Set to OFF to disable the signal
0	0	DAC OUT (DAO)
0	1	ARRAY
1	0	FILTO
1	1	OFF

Configuration Register CFG0, CFG1 and CFG2. The bits described on this page are highlighted.

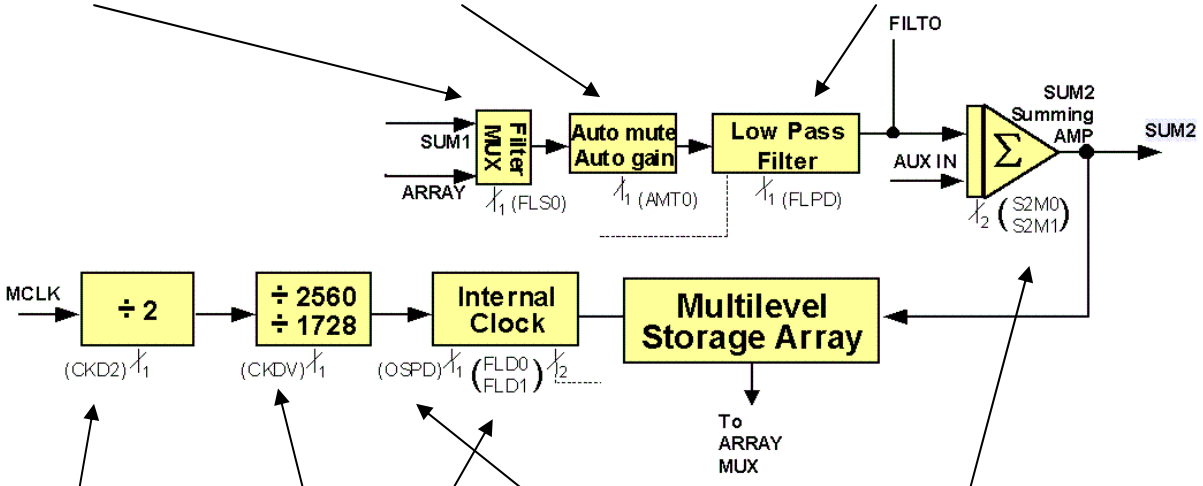
CIG2	CIG1	CIG0	AXG1	AXG0	AXPD	INS0	OSPD	AMT0	CDI1	CDI0	OPS1	OPS0	OPA1	OPA0	VLPD		*CFG0*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD		*CFG1*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
X	X	X	CKD2	COG2	COG1	COG0	CKDV	MUTE	HPF0	HSR0	I2S0	LAW1	LAW0	DAPD	ADPD		*CFG2*

ISD5216 ANALOG STRUCTURE (Right Half) description

FLS0	Select input from MLS array or sum 1 amp
0	SUM1
1	ARRAY

AMT0	Switch on or off the auto gain circuit
0	Uncompressed
1	Compressed

FLPD	Control power to the low pass filter
0	Power Up
1	Power Down



S2M1	S2M0	SOURCE
0	0	BOTH
0	1	AUX IN ONLY
1	0	FILTO ONLY
1	1	Power Down

FLD1	FLD0	SAMPLE RATE	PASS BAND
0	0	8 KHz	3.7 KHz
0	1	6.4 KHz	2.9 KHz
1	0	5.3 KHz	2.5 KHz
1	1	4.0 KHz	1.8 KHz

CKD2	Divide Master Clock by 1 or 2
0	Divide by 1
1	Divide by 2

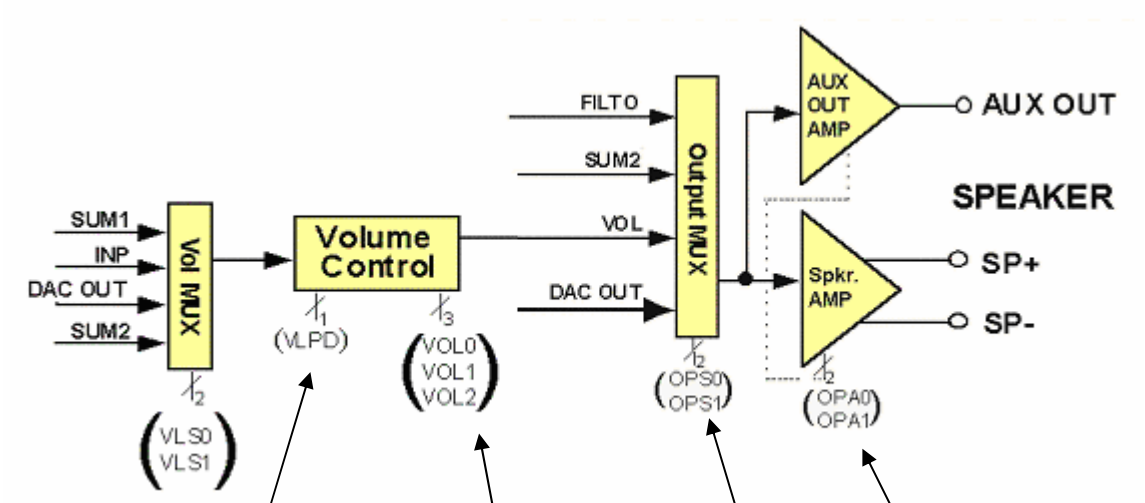
CKDV	Divide Master Clock by 1728 or 2560
0	Divide by 1728
1	Divide by 2560

OSPD	Power Up Internal Oscillator
0	Power up
1	Power Down

Configuration Register CFG0, CFG1 and CFG2. The bits described on this page are highlighted.

CIG2	CIG1	CIG0	AXG1	AXG0	AXPD	INS0	OSPD	AMT0	CDI1	CDI0	OPS1	OPS0	OPA1	OPA0	VLPD		CFG0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD		CFG1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
X	X	X	CKD2	COG2	COG1	COG0	CKDV	MUTE	HPF0	HSR0	I2S0	LAW1	LAW0	DAPD	ADPD		CFG2

7.7.1 Speaker, AUX OUT and Volume Control Description



VLPD	Switch volume control on or off
0	Power Up
1	Power Down

OPA1	OPA0	State of the speaker output	State of aux out
0	0	Power Down	Power Down
0	1	3.6 V_{P-P} @ 150 Ω	Power Down
1	0	23.5 mW @ 8 Ω	Power Down
1	1	Power Down	1 V_{P-P} Max @ 5 KΩ

VLS1	VLS0	Select input source to the volume mux
0	0	DAC OUT
0	1	SUM2
1	0	SUM1

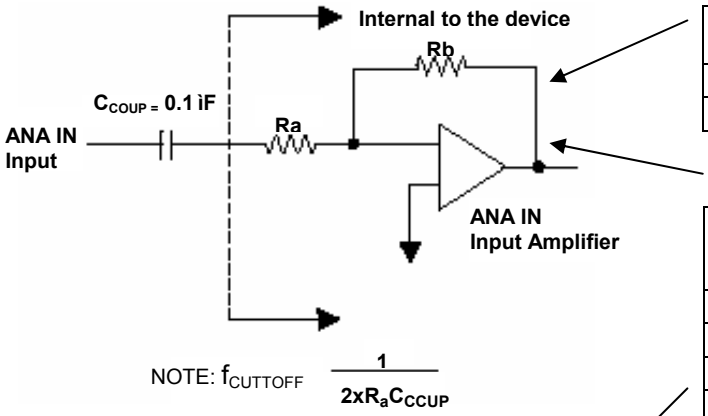
VOL2	VOL1	VOL 0	Attenuation
0	0	0	0 dB
0	0	1	4 dB
0	1	0	8 dB
0	1	1	12 dB
1	0	0	16 dB
1	0	1	20 dB
1	1	0	24 dB
1	1	1	28 dB

OPS1	OPS0	Select input source to the analog output mux
0	0	VOL
0	1	DAC OUT
1	0	FILTO
1	1	SUM2

Configuration Register CFG0, CFG1 and CFG2. The bits described on this page are highlighted.

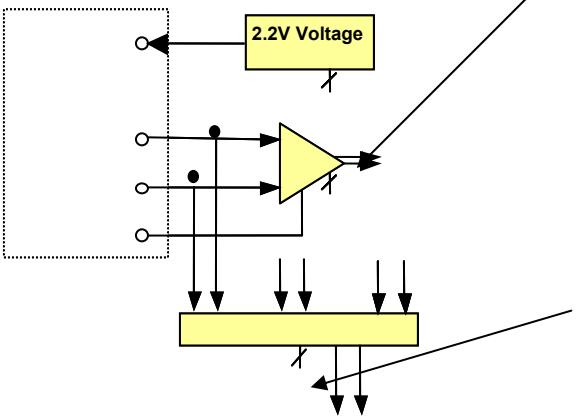
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CIG2	CIG1	CIG0	AXG1	AXG0	AXPD	INS0	OSPD	AMT0	CDI1	CDI0	OPS1	OPS0	OPA1	OPA0	VLPD	*CFG0*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	*CFG1*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
X	X	X	CKD2	COG2	COG1	COG0	CKDV	MUTE	HPF0	HSR0	I2S0	LAW1	LAW0	DAPD	ADPD	*CFG2*

7.7.2. Microphone and Auxiliary Inputs



AXPD	Power up the AUX in input amplifier
0	Power Up
1	Power Down

AXG1	AXG0	Gain (dB) of the aux input amplifier
0	0	0
0	1	3
1	0	6
1	1	9



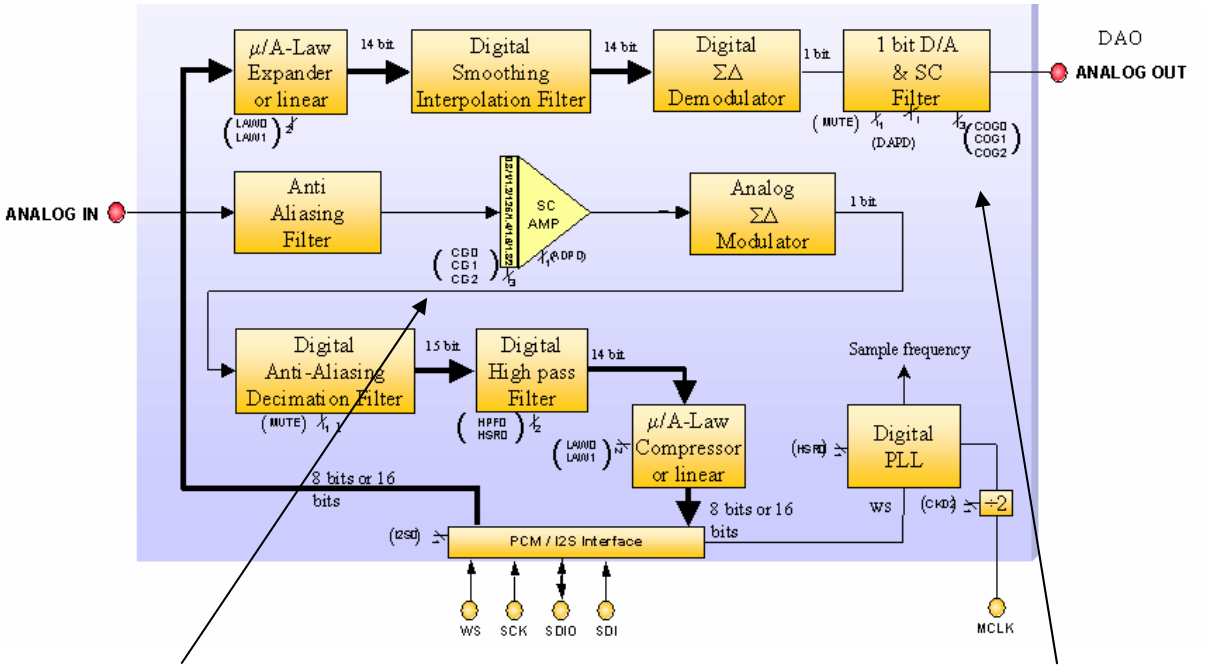
AGPD	Power up the AGC control and the MIC bias voltage
0	Power Up
1	Power Down

CDI1	CDI0	Select input to the CODEC A/D converter
0	0	INP
0	1	SUM2
1	0	MIC
1	1	No Input

Configuration Register CFG0, CFG1 and CFG2. The bits described on this page are highlighted.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
CIG2	CIG1	CIG0	AXG1	AXG0	AXPD	INS0	OSPD	AMT0	CDI1	CDI0	OPS1	OPS0	OPA1	OPA0	VLPD		*CFG0*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD		*CFG1*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
X	X	X	CKD2	COG2	COG1	COG0	CKDV	MUTE	HPF0	HSR0	I2S0	LAW1	LAW0	DAPD	ADPD		*CFG2*

7.7.3. CODEC Configuration (First Page)



CIG2	CIG1	CIG0	ADC GAIN
0	0	0	0.80
0	0	1	1.00
0	1	0	1.20
0	1	1	1.25
1	0	0	1.40
1	0	1	1.60
1	1	0	1.80
1	1	1	2.00

COG2	COG1	COG0	DAC GAIN (dB)
0	0	0	0
0	0	1	+2
0	1	0	+4
0	1	1	+6
1	0	0	-8
1	0	1	-6
1	1	0	-4
1	1	1	-2

Configuration Register CFG0, CFG1 and CFG2. The bits described on this page are highlighted.

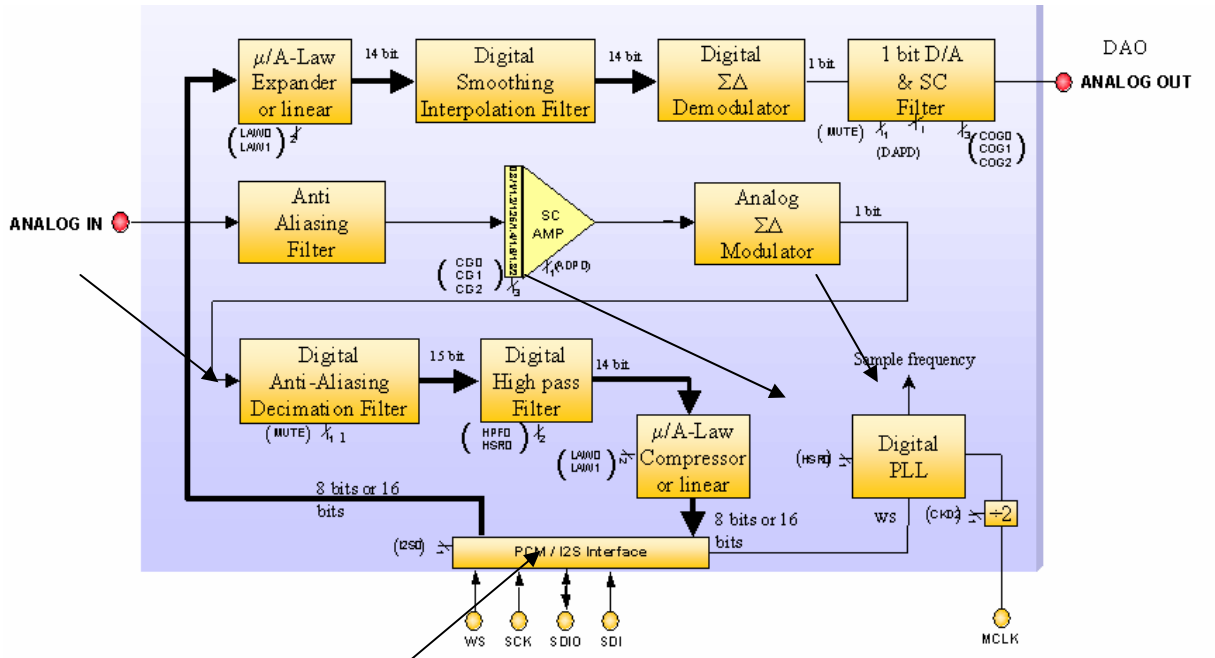
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CIG2	CIG1	CIG0	AXG1	AXG0	AXPD	INS0	OSPD	AMT0	CDI1	CDI0	OPS1	OPS0	OPA1	OPA0	VLPD	*CFG0*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	*CFG1*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
X	X	X	CKD2	COG2	COG1	COG0	CKDV	MUTE	HPF0	HSR0	I2S0	LAW1	LAW0	DAPD	ADPD	*CFG2*

LAW1	LAW0	Data Format
0	0	Two's Complement
0	1	A-Law
1	0	μ - Law
1	1	Signed Magnitude

MUTE	State
0	Unmuted
1	muted

DAPD	Power up the CODEC DAC
0	Power Up
1	Power Down

CODEC Configuration (Second Page)



ADPD	CODEC ADC
0	Power Up
1	Power Down

I2S0	Digital Interface
0	PCM
1	I2S

HPF0	High Pass Filter
0	Bypassed
1	Enabled

HSR0	Sample Rate Mode
0	Low
1	High

Configuration Register CFG0, CFG1 and CFG2. The bits described on this page are highlighted.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CIG2	CIG1	CIG0	AXG1	AXG0	AXPD	INS0	OSPD	AMT0	CDI1	CDI0	OPS1	OPS0	OPA1	OPA0	VLPD	*CFG0*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	*CFG1*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
X	X	X	CKD2	COG2	COG1	COG0	CKDV	MUTE	HPF0	HSR0	I2S0	LAW1	LAW0	DAPD	ADPD	*CFG2*

7.8. PIN DETAILS

7.8.1. Power and Ground Pins

V_{CCA}, V_{CCD} (Voltage Inputs)

To minimize noise, the analog and digital circuits in the Winbond ISD5216 device use separate power busses. These +3 V busses lead to separate pins. Tie the V_{CCD} pins together as close as possible, and decouple both supplies as near to the package as possible.

V_{SSA}, V_{SSD} (Ground Inputs)

The Winbond ISD5216 series utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close to the package as possible, and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pin is less than 3Ω. The backside of the die is connected to V_{SSD} through the substrate resistance. In a chip-on-board design, the die attach area must be connected to V_{SSD}.

NC (No Connect)

These pins should not be connected to the board at any time. Connection of these pins to any signal, ground or $V_{CC,}$ may result in incorrect device behavior or cause damage to the device.

7.8.2. Digital I/O Pins:

SCL (SERIAL CLOCK LINE)

The Serial Clock Line is a bi-directional clock line. It is an open-drain line requiring a pull-up resistor to Vcc. It is driven by the "master" chips in a system and controls the timing of the data exchanged over the Serial Data Line.

SDA (SERIAL DATA LINE)

The Serial Data Line carries the data between devices on the I^2C interface. Data must be valid on this line when the SCL is HIGH. State changes can only take place when the SCL is LOW. This is a bi-directional line requiring a pull-up resistor to Vcc.

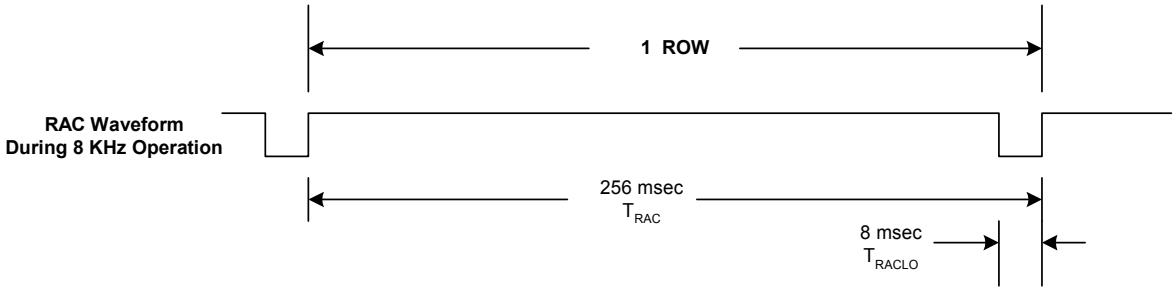
A0, A1 (Address Pins)

These two pins are normally strapped for the desired address that the Winbond ISD5216 will have on the I^2C serial interface. If there are four of these devices on the bus, then each must be strapped differently in order to allow the master device to address them individually. The possible addresses range from 80h to 87h, depending upon whether the device is being written to, or read from, by the host.

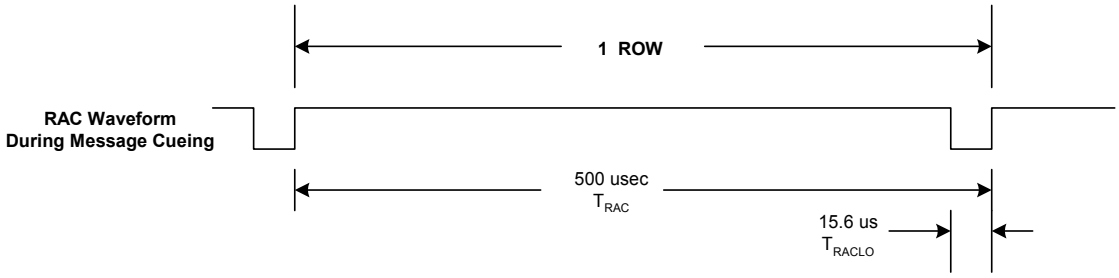
The Winbond ISD5216 has a 7-bit slave address of which only A0 and A1 are pin programmable. The eighth bit (LSB) is the R/W bit. Thus, the address will be 1000 0xy0 or 1000 0xy1

RAC (ROW ADDRESS CLOCK)

RAC is an open drain output pin that normally marks the end of a row. At the 8 kHz sample frequency the duration of this period is 256 ms. there are 1888 pages of memory in the Winbond ISD5216 device. RAC stays HIGH for 248 ms and goes LOW for the remaining 8 ms before it reaches the end of the page.

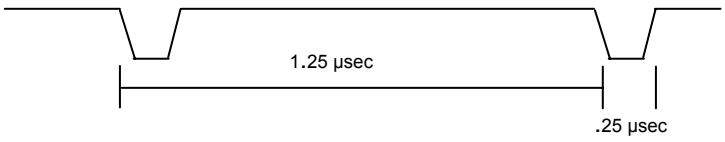


The RAC pin remains HIGH for 500 µsec and stays LOW for 15.6 µsec under the Message Cueing mode. See the *Timing Parameters* table on page 63 for RAC timing information at other sample rates. When a record command is first initiated, the RAC pin remains HIGH for an extra T_{RACLO} period in order to load sample and hold circuits internal to the device. The RAC pin can be used for message management techniques.



RAC Waveform

During Digital Erase



INT (Interrupt)

INT is an open drain output pin. The Winbond ISD5216 Interrupt pin goes LOW and stays LOW when an Overflow (OVF) or End of Message (EOM) marker is detected. Each operation that ends in an EOM or OVF generates an interrupt, including the message cueing cycles. The interrupt is cleared by a READ STATUS instruction that gives a status byte on the SDA line.

MCLK (Master Clock Input)

The Master clock input for the Winbond ISD5216 product has an internal pull-down device. Normally, the Winbond ISD5216 ChipCorder section is operated at one of four internal rates selected for its internal oscillator by the Sample Rate Select bits. If the internal oscillator is powered down (configuration bit OSPD set to ONE), the device is clocked through the MCLK pin as shown in the section *ISD5216 Analog Structure (right half)* description on page 32. If an external clock is not used, this input should be connected to V_{SSD}.

7.8.3. CODEC Iinterface Pincs

SCK

Bit clock for PCM or I2S audio data

WS

The Word Sync (Frame Sync) signal is used to differentiate between data for left and right channel in I^2S. For PCM it signals the beginning of the word.

SDIO

For PCM, this is the output signal from the CODEC, it should be connected to the input pin of the receiving device.

In I^2S mode, this is a bi-directional pin that should be connected to the bi-directional I^2S data pin on the other device connected to the I^2S bus.

SDI

This pin is only used when the CODEC is in PCM mode, this signal provides digital audio input to the CODEC it should be connected to the output pin of the transmitting device.

7.8.4. ANALOG I/O PINS

MIC+, MIC- (Microphone Input +/-)

The microphone inputs transfer the voice signal to the on-chip AGC preamplifier, or directly to the CODEC INPUT MUX, depending on the selected path. The AGC circuit has a range of 45 dB in order to deliver a nominal 694 mV p-p into the storage array from a typical electret microphone output of 2 to 20 mV p-p. The input impedance is typically 20 kΩ differential and 13.3 kΩ differential when the CODEC INPUT MUX MICIN path is selected.

The MICBS pin provides a 2.2V bias voltage for the external microphone only when the AGC is powered up. Using this regulated bias voltage results in less supply noise coupling into the MIC+ and

MIC- pins compared to the situation in which the external microphone is powered up through the power supply. It also saves current during power down.

ACAP (AGC Capacitor)

This pin provides the capacitor connection for setting the parameters of the microphone AGC circuit. It should have a 4.7 µF capacitor connected to ground. It cannot be left floating. This is because the capacitor is also used in the playback mode for the AutoMute circuit or when signal compression is chosen (AMT0 is set to ONE). This circuit reduces the amount of noise present in the output during quiet pauses. Tying this pin to ground gives maximum gain. Tying it to V_{CCA} gives minimum gain for the AGC amplifier, but cancels the AutoMute function. Connect the capacitor to low noise ground as ground noise directly affects the microphone performance

SP +, SP- (Speaker +/-)

This is the speaker differential output circuit. It is designed to drive an 8Ω speaker connected across the speaker pins, up to a maximum of 23.5 mW RMS power. This stage has two selectable gains, 1.32 and 1.6, which can be chosen through the configuration registers. These pins are biased to approximately 1.2 VDC and, if used single-ended, must be capacitively coupled to their load. Do **NOT** ground the unused pin.

AUX OUT (Auxiliary Output)

The AUX OUT is an additional audio output pin to be used, for example, to drive the speaker circuit in a "car kit." It drives a minimum load of 5 kΩ and up to a maximum of 1 V p-p. The AC signal is superimposed on approximately 1.2 VDC bias and must be capacitively coupled to the load.

AUX IN (Auxiliary Input)

The AUX IN is an additional audio input to the Winbond *ISD5216*, such as from the microphone circuit in a mobile phone "car kit." This input has a nominal 694 mV p-p level at its minimum gain setting (0 dB). (See *Aux In Amplifier Gain Settings Table* below). Additional gain is available in 3 dB steps (controlled by the I^2C interface) up to 9 dB.

0TLP Input V_{P-P} (2)	Gain Setting	Gain (1) (dB)	Gain (1)	Array In/Out V_{P-P}	Speaker Out V_{P-P} (3)
0.694	00	0	1.00	0.694	0.694
0.491	01	3	1.41	0.694	0.694
0.347	10	6	2.00	0.694	0.694
0.245	11	9	2.82	0.694	0.694

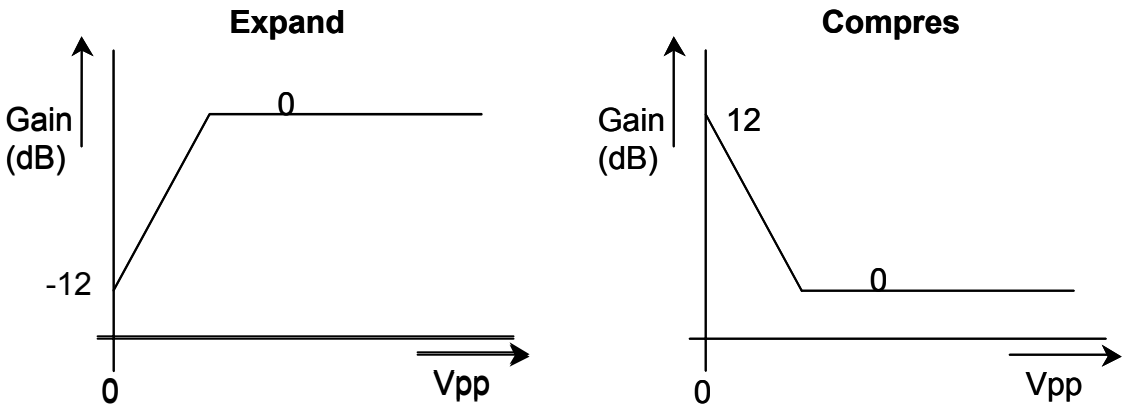
1. *Gain from AUX IN to ARRAY IN*
2. *0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping*
3. *Differential*

7.9. AUTO MUTE AND AUTO GAIN FUNCTIONS

During playback, the signal passes through the Automatic Attenuator before it is filtered. The Automatic Attenuator will attenuate all signals at the noise level in order to reduce the noise during quiet pauses.

During record, low level input signals are brought up by the Auto Gain function if the configuration bit D7 of CFG0 (AMT0) is set. This improves the signal to noise ratio of recorded low level input signals. If the configuration bit CFG0<7> (AMT0) is set to ZERO, all input levels are recorded with the same gain setting. The attack and release time of the Auto Gain and Auto Mute functions is set by the capacitor on the ACAP pin. The AGC cannot be used if the Auto Gain or Auto Mute function is enabled.

Tattack ≈ 0,1504 x Vpeak Trelease ≈ 6.58 x Vpeak @ Cattcap=4.7 μF



7.10 PROGRAMMING THE ISD 5216

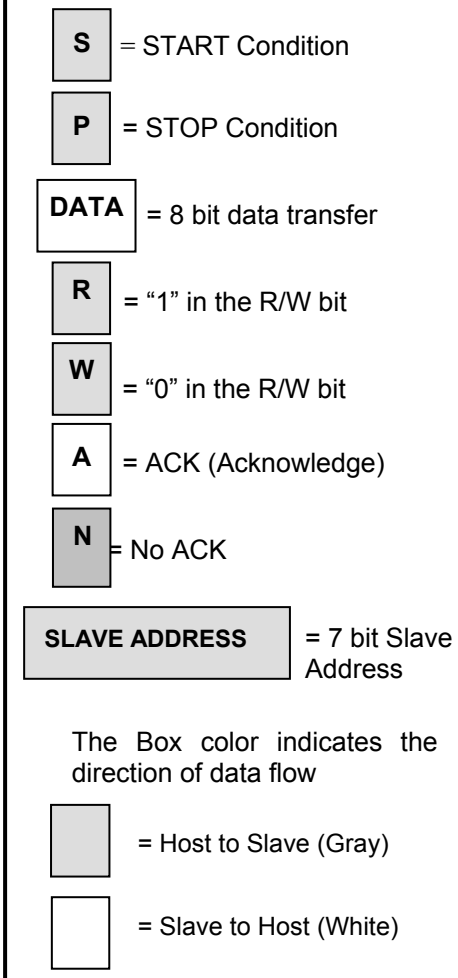
7.10.1. Sending a byte on the I2C interface

When reading or writing a byte of data on the I²C bus, two different mechanisms for flow control are used, the first is the standard ACK that the slave or master sends after reading or writing a byte, but the ISD5216 also uses flow control by holding the clock line (SCL) low until the chip is ready to transmit data,

For example, the sequence of sending the slave address will be as follows:

1. Send one byte 10000000 {Slave Address, R/W = 0} 80h.
2. Slave ACK.
3. Next time the clock is pulled high by the master, wait for SCL to actually go high.

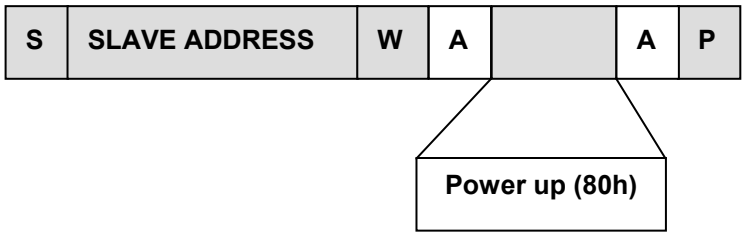
Conventions used in I²C Data Transfer Diagrams



7.10.2. POWER-UP SEQUENCE

This sequence prepares the *ISD5216* for an operation to follow, and waits for the Tpud time before sending the next command sequence.

1. Send I²C Start.
2. Send one byte 10000000 {Slave Address, R/W = 0} 80h.
3. Send one byte 10000000 {Command Byte = Power Up} 80h.
4. Send I²C Stop.



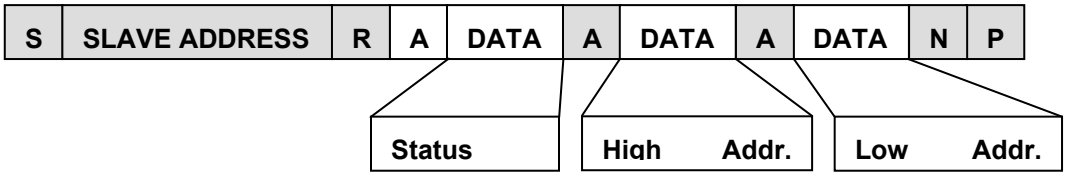
7.10.3. Read Status command

The read status command is a read request from the Host processor to the ISD5216 without delivering a Command Byte. The Host supplies all of the clocks (SCL). The ISD5216 drives the data line (SDA). During the read commands, to read status, send the following sequence.

1. Host executes I²C START
2. Send Slave Address with R/W bit = "1" (Read) 81h.
3. Read one byte of data and send ACK, the read data is the status byte
4. Read one byte of data and send ACK, the read data is the upper address byte
5. Read one byte of data and send NACK, the read data is the lower address byte
6. Host sends I²C STOP

Note: The processor could have sent an I²C STOP after the Status Word data transfer, and thus aborted the transfer of the Address bytes

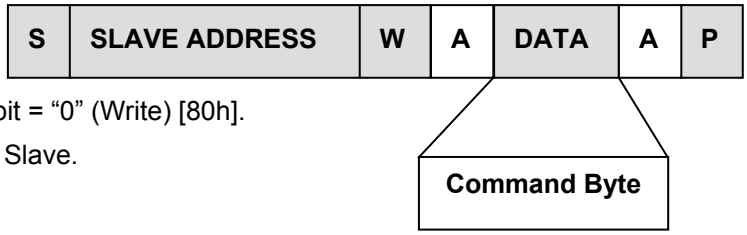
A graphical representation of this operation is found below. See the caption box above for more explanation.



7.10.4. Load Command Byte Register (Single Byte Load):

A single byte may be written to the Command Byte Register in order to power up the device, start or stop Analog Record (if no address information is needed), or perform a Message Cueing function. The Command Byte Register is loaded as follows:

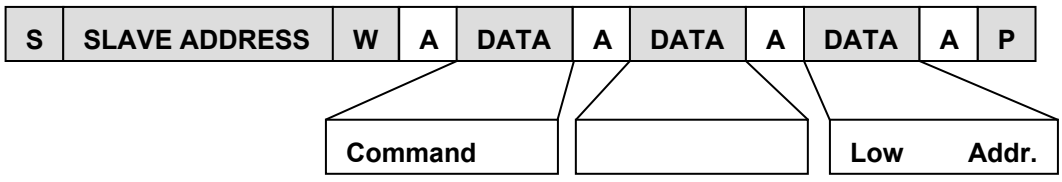
1. Host executes I^2C START.
2. Send Slave Address with R/W bit = “0” (Write) [80h].
3. Host sends a command byte to Slave.
4. Host executes I^2C STOP.



7.10.5. Load Command Byte Register (Address Load):

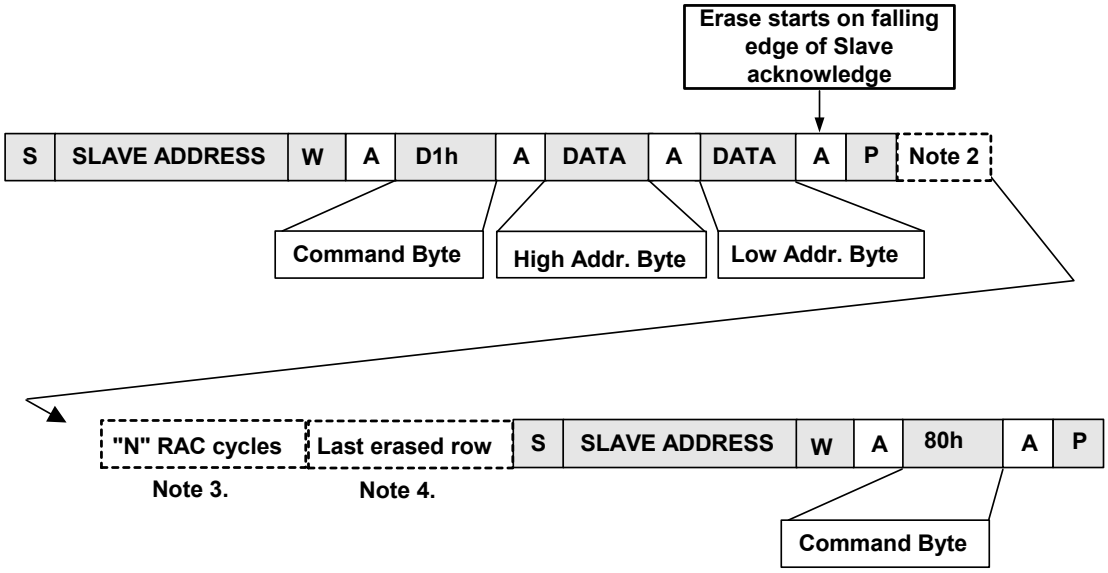
For the normal addressed mode the Registers are loaded as follows:

1. Host executes I^2C START.
2. Send Slave Address with R/W bit = “0” (Write).
3. Host sends a byte to Slave - (Command Byte).
4. Host sends a byte to Slave - (High Address Byte).
5. Host sends a byte to Slave - (Low Address Byte).
6. Host executes I^2C STOP.



7.10.6. Digital Erase

1. Host executes I²C START.
2. Send Slave Address with /W bit = “0” (Write).
3. Send Digital Erase command (d1h)
4. Send high address byte (00h)
5. **Send low address byte (a0h) - erase row 5 in this example. Erase operations must be addressed on a page boundary. The 5 LSB bits of the Low Address Byte will be ignored.**
6. Host executes I²C STOP.
7. Wait until the desired number of pages have been erased. There will be a pulse on the RAC pin for each page that is erased. After the stop command (described below) has been received, erasing will stop at the end of the page currently being erased. To erase one page only, issue the stop command immediately after the start erase command.
8. Host executes I²C START.
9. Send Slave Address with /W bit = “0” (Write).
10. Send the Stop command (c0h).
11. Host executes I²C STOP



Notes:

1. **I²C bus is released while erase proceeds. Other devices may use the bus until it is time to execute the STOP command that causes the end of the Erase operation.**
2. **Host processor must count RAC cycles to determine where the chip is in the erase process, one row per RAC cycle. RAC pulses LOW for 0.25 microsecond at the end of each erased row. The erase of the “next” row begins with the rising edge of RAC. See the Digital Erase RAC timing diagram on page 46.**
3. **4.When the erase of the last desired row begins, the following STOP command (Command Byte = 80 hex) must be issued. This command must be completely given, including receiving the ACK from the Slave before the RAC pin goes HIGH .25 microseconds before the end of the row.**

7.10.7. Digital Write

1. Send I2C START.
2. Send Slave Address with /W bit = “0” (Write).
3. Send Digital Write command (c9h)
4. Send high address byte (00h)
5. Send low address byte (a0h) - erase row 5 in this example.
6. Write all bytes that needs to be written
7. Send I2C STOP.
8. Read status byte, see example above, until ready bit is set.

7.10.8. Digital Read

1. Send I^2C START.
2. Send Slave Address with /W bit = “0” (Write).
3. Send Digital Read command (e1h)
4. Send high address byte (00h)
5. Send low address byte (a0h) - erase row 5 in this example.
6. Send I^2C START.
7. Send Slave Address with /W bit = “1” (Read).
8. Send I^2C Read commands until all bytes have been read.
9. After the last byte has been read, send NACK.
10. Send I2C STOP.

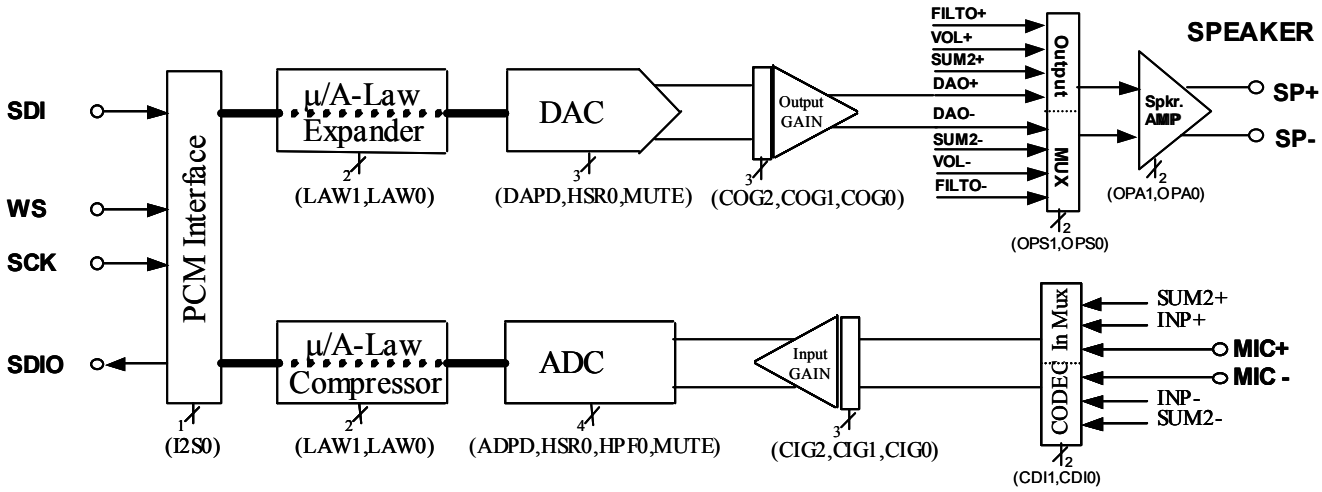
7.10.9. Feed Through Mode

To set up the device for the various paths requires loading the three 16-bit Configuration Registers with the correct data. For example, in the Feed Through Mode, the device only needs to be powered up and a few paths selected. This mode enables the **ISD5216** to connect to a cellular or cordless baseband phone chip set without affecting the audio source or destination. There are two paths involved: the transmit path and the receive path. The transmit path connects the Winbond chip’s microphone source through to the digital audio input on the baseband chip set. The receive path connects the baseband chip set’s digital output through to the speaker driver on the Winbond chip. This allows the Winbond chip to substitute for Analog to Digital and Digital to Analog conversion, and incidentally gain access to the audio, both to and from the baseband chip set.

To setup the environment described above, a series of commands need to be sent to the ISD5216. First, the chip needs to be powered up as described in *Power-Up Sequence* on page 25. Then the Configuration Registers need to be filled with the specific data to connect the desired paths. In the case of the Feed Through Mode, most of the chip can remain powered down. **The Feed Through Mode** diagram illustrates the affected paths.

The following example shows the setup for a full-duplex feed-through path at 8 kHz sampling rate. The twos complement data format is enabled. The High Pass filter is also enabled. The Master Clock input is running at 13.824MHz.

To select the Feed Through mode, the following control bits must be configured in the ISD5216 configuration register



1. **Connect the microphone to the CODEC input -** Bits CDI1 and CDI0 control the state of the CODEC INPUT MUX. These are the D6 and D5 bits, respectively, of Configuration Register 0 (CFG0) and they should be set to ONE and ZERO.
2. **Power up the ADC**—Bit ADPD controls the power up state of ADC. This is bit D0 of CFG2 and it should be a ZERO to power up the ADC.
3. **Set the CODEC input gain** - The input gain setting will depend on the input level at the MIC+/- pins and can be set by the CODEC INPUT GAIN Bits CIG2, CIG1 and CIG0. These are the D15, D14 and D13 bits, respectively, of Configuration Register 0 (CFG0).
4. **Set audio interface** - Set the interface mode to PCM-interface by setting bit I^2S0, bit D4 of CFG2, to ZERO. This will also enable full duplex mode.
5. **Set data format**- Set the digital data format through bits LAW1 and LAW0. These are bits D3 and D2 of CFG2, respectively.
6. **Set Master Clock Division** - Set the Master Clock division ratios as described in *Set Master Clock Division Ratio* on page 25.
7. **Power up the DAC —** Bit DAPD controls the power up state of the DAC. This is bit D1 of CFG2 and should be a ZERO to power up the DAC.
8. **Send DAC output to speaker** - Select the DAC path through the OUTPUT MUX—Bits OPS0 and OPS1 control the state of the OUTPUT MUX. These are bits D3 and D4, respectively, of CFG0 and they should be set to the state where D3 is ONE and D4 is ZERO to select the DAC path.
9. **Power up the Speaker Amplifier**—Bits OPA0 and OPA1 control the state of the Speaker and AUX amplifiers. These are bits D1 and D2, respectively, of CFG0. They should be set to the state where D1 is ONE and D2 is ZERO. This powers up the Speaker Amplifier and configures it for a higher gain setting (for use with a piezo speaker element) and also powers down the AUX output stage.

10. **Power down the Volume Control Element**—Bit VLPD controls the power up state of the Volume Control. This is bit D0 of CFG0 and it should be set to a ONE to power down this stage.
11. **Power down the internal oscillator**—Bit PDOS controls the power up state of the internal ChipCorder oscillator. This is bit D8 of CFG0 and it should be set to a ONE to power down this oscillator
12. **Power down the AUX IN amplifier**—Bit AXPD controls the power up state of the AUX IN input amplifier. This is bit D10 of CFG0 and it should be set to a ONE to power down this stage.
13. **Power down the SUM1 and SUM2 Mixer amplifiers**—Bits S1M0 and S1M1 control the SUM1 mixer and bits S2M0 and S2M1 control the SUM2 mixer. These are bits D7 and D8 in CFG1, and bits D5 and D6 in CFG1, respectively. All four bits should be set to a ONE in order to power down these two amplifiers.
14. **Power down the FILTER stage**—Bit FLPD controls the power up state of the FILTER stage in the device. This is bit D1 in CFG1 and should be set to a ONE to power down the stage.
15. **Power down the AGC amplifier**—Bit AGPD controls the power up state of the AGC amplifier. This is bit D0 in CFG1 and should be set to a ONE to power down this stage.
16. **Don't Care bits**—All other bits are not used in Feed Through Mode. Their bits may be set to either level. In this example, we will set all the "Don't Care" bits to a ZERO.

This setup should result in the following configuration register values:

CFG0=0010 0101 0100 1011 (hex 254B)

CFG1=0000 0001 1110 0011 (hex 01E3).

CFG2=0000 0000 0100 0000 (hex 0040).

The three registers must be loaded with CFG0 first followed by CFG1 and CFG2. The internal set up for these registers will take effect synchronously, with the rising edge of SCL.

7.10.10. Call Record

The call record mode adds the ability to record the incoming phone call. In most applications, the ISD5216 would first be set up for Feed Through Mode as described above. When the user wishes to record the incoming call, the set up of the chip is modified to add that ability. For the purpose of this explanation, we will use the 6.4 kHz ChipCorder sample rate during recording.

The block diagram of the ISD5216 shows that the Multilevel Storage array is always driven from the SUM2 SUMMING amplifier. The path traces back from there, through the LOW PASS Filter, the FILTER MUX, the SUM1 SUMMING amplifier, the SUM1 MUX, back to the origin CODEC. Feed Through Mode has already powered up the CODEC, so we only need to power up and enable the path to the Multilevel Storage array from that point:

1. **Setup the feed through mode described in the previous section**
2. **Select the CODEC path through the SUM1 MUX**—Bits S1S0 and S1S1 control the state of the SUM1 MUX. These are bits D9 and D10, respectively, of CFG1 and they should be set to the state where both D9 and D10 are ZERO to select the CODEC path.
3. **Select the SUM1 MUX input (only) to the S1 SUMMING amplifier**—Bits S1M0 and S1M1 control the state of the SUM1 SUMMING amplifier. These are bits D7 and D8, respectively, of CFG1 and they should be set to the state where D7 is ONE and D8 is ZERO to select the SUM1 MUX (only) path.
4. **Select the SUM1 SUMMING amplifier path through the FILTER MUX—**Bit FLS0 controls the state of the FILTER MUX. This is bit D4 of CFG1 and it must be set to ZERO to select the SUM1 SUMMING amplifier path.
5. **Deselect the signal compression**-Bit AMT0 controls the signal compression. This is bit D7 of CFG0 and it must be set to ZERO.
6. **Power up the LOW PASS FILTER**—Bit FLPD controls the power up state of the LOW PASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.
7. **Select the 6.4 kHz sample rate**—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 6.4 kHz sample rate, D2 must be set to ONE and D3 set to ZERO.
8. **Select the LOW PASS FILTER input (only)** *to the S2 SUMMING amplifier*—Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6, respectively, of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

The configuration settings in the call record mode are:

CFG0=0100 0100 0000 1011 (hex 440B).

CFG1=0000 0000 1100 0101 (hex 00C5).

CFG2=0000 0000 0100 0000 (hex 0040).

7.10.11. Memo Record

The Memo Record mode sets the chip up to record from the local microphone into the chip's Multilevel Storage Array. A connected cellular telephone or cordless phone chip set may remain powered down since they are not active in this mode. The path to be used is microphone input to AGC amplifier, then through to the INPUT SOURCE MUX, to the SUM1 SUMMING amplifier. From there, the path goes through the FILTER MUX, the LOW PASS FILTER, the SUM2 SUMMING amplifier, then to the MULTILEVEL STORAGE ARRAY. In this example, we will select the 5.3 kHz sample rate. The rest of the chip may be powered down.

1. **Power up the AGC amplifier** - Bit AGPD controls the power up state of the AGC amplifier. This is bit D0 of CFG1 and must be set to ZERO to power up this stage.

2. **Select the AGC amplifier through the INPUT SOURCE MUX**—Bit INS0 controls the state of the INPUT SOURCE MUX. This is bit D9 of CFG0 and must be set to a ZERO to select the AGC amplifier.

3. **Select the INPUT SOURCE MUX (only) to the S1 SUMMING amplifier**—Bits S1M0 and S1M1 control the state of the SUM1 SUMMING amplifier. These are bits D7 and D8, respectively, of CFG1 and they should be set to the state where D7 is ZERO and D8 is ONE to select the INPUT SOURCE MUX (only) path.

4. **Select the SUM1 SUMMING amplifier path through the FILTER MUX**—Bit FLS0 controls the state of the FILTER MUX. This is bit D4 of CFG1 and it must be set to ZERO to select the SUM1 SUMMING amplifier path.

5. **Deselect the signal compression-**Bit AMT0 controls the signal compression. This is bit D7 of CFG0 and it must be set to ZERO.

6. **Power up the LOW PASS FILTER**—Bit FLPD controls the power up state of the LOW PASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.

7. **Select the 5.3 kHz sample rate**—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 5.3 kHz sample rate, D2 must be set to ZERO and D3 set to ONE.

8. **Select the LOW PASS FILTER input (only)** to the S2 SUMMING amplifier – BITS S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6, respectively, of CFG1, set D5 to ZERO and D6 to ONE to select the LOW PASS FILTER (only) path.

9. **Power up the Internal Oscillator**—Bit OSPD controls the power up state of the Internal Oscillator. This is bit D8 of CFG0 and it must be set to ZERO to power up the Internal Oscillator.

To set up the chip for Memo Record, the configuration registers are set up as follows:

CFG0=0000 0100 0000 0001 (hex 0401).

CFG1=0000 0001 0100 1000 (hex 0148).

CFG2=0000 0000 0000 0011 (hex 0003).

7.10.12. Memo and Call Playback

This mode sets the chip up for local playback of recorded messages. The playback path is from the MULTILEVEL STORAGE ARRAY to the FILTER MUX, then to the LOW PASS FILTER stage. From there, the audio path goes through the SUM2 SUMMING amplifier to the VOLUME MUX, through the VOLUME CONTROL then to the SPEAKER output stage. We will assume that we are driving a piezo speaker element and that this audio was recorded at 8 kHz. All unnecessary stages will be powered down.

1. **Select the MULTILEVEL STORAGE ARRAY path through the FILTER MUX**—Bit FLS0, the state of the FILTER MUX. This is bit D4 of CFG1 and must be set to ONE
2. **Power up the LOW PASS FILTER**—Bit FLPD controls the power up state of the LOW PASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO.
3. **Select the 8.0 kHz sample rate**—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable 8.0 kHz sample rate, D2 and D3 must be set to ZERO.
4. **Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier** —Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6, respectively, of CFG1. Set D5 to ZERO and D6 to ONE to select the LOW PASS FILTER (only) path.
5. **Select the SUM2 SUMMING amplifier path through the VOLUME MUX**—Bits VLS0 and VLS1 control the VOLUME MUX stage. These bits are D14 and D15, respectively, of CFG1. Set D14 to ONE and D15 to ZERO to select the SUM2 SUMMING amplifier.
6. **Power up the VOLUME CONTROL LEVEL**—Bit VLPD controls the power-up state of the VOLUME CONTROL attenuator. This is Bit D0 of CFG0. Set this bit to a ZERO.
7. **Select a VOLUME CONTROL LEVEL**—Bits VOL0, VOL1 and VOL2 control the state of the VOLUME CONTROL LEVEL. These are bits D11, D12, and D13, respectively, of CFG1. A binary count of 000 through 111 controls the amount of attenuation through that stage. To set an attenuation of –12 dB, D11 should be set to ONE, D12 should be set to ONE, and D13 should be set to a ZERO.
8. **Select the VOLUME CONTROL path through the OUTPUT MUX**—These are bits D3 and D4, respectively, of CFG0. Set D3 to ZERO and D4 is a ZERO to select the VOLUME CONTROL.
9. **Power up the SPEAKER amplifier and select the HIGH GAIN mode**—Bits OPA0 and OPA1 control the state of the speaker (SP+ and SP–) and AUX OUT outputs. These are bits D1 and D2 of CFG0. Set D1 to ONE and D2 to ZERO to power-up the speaker outputs in the HIGH GAIN mode and to power-down the AUX OUT.
10. **Power up the Internal Oscillator**—Bit OSPD controls the power up state of the Internal Oscillator. This is bit D8 of CFG0 and it must be set to ZERO to power up the Internal Oscillator.

To set up the chip for Memo or Call Playback, the configuration registers are set up as follows:

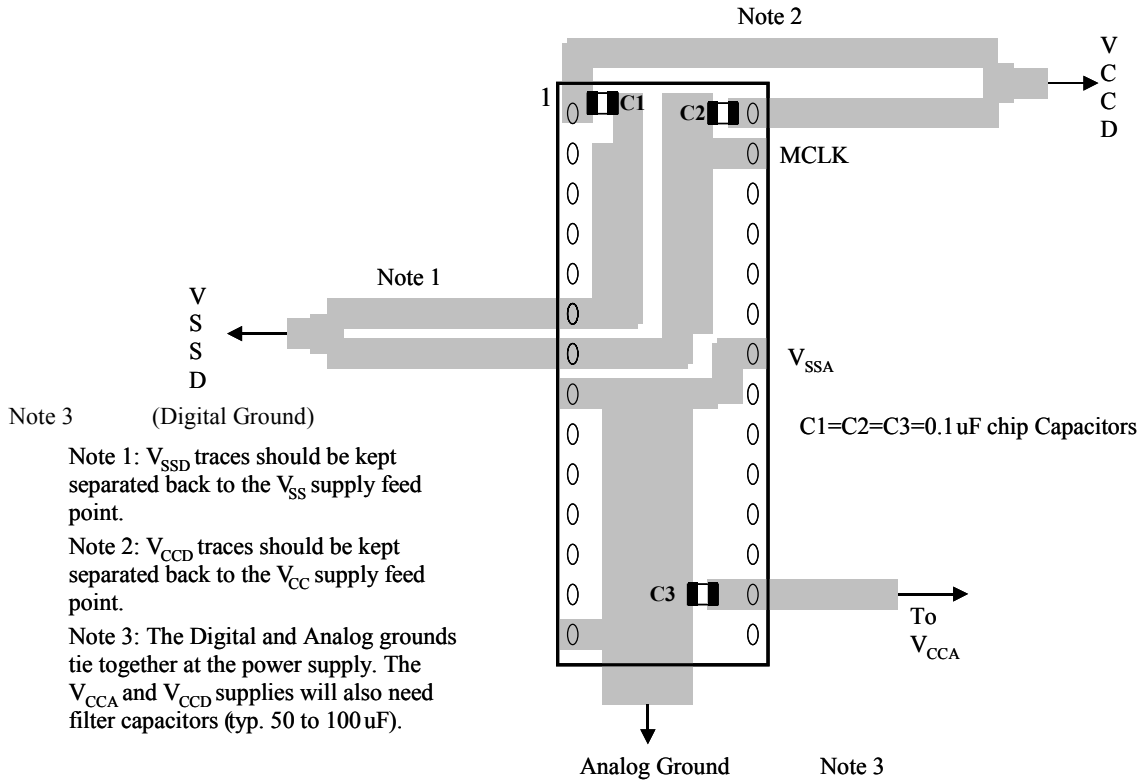
CFG0 = 0010 0100 0010 0010 (hex 2422).

CFG1 = 0101 1001 1101 0001 (hex 59D1).

CFG2 = 0000 0000 0000 0011 (hex 0003).

7.11. SAMPLE PC LAYOUT FOR PDIP

The PDIP package is illustrated from the top. PC board traces and the three chip capacitors are on the bottom side of the board.



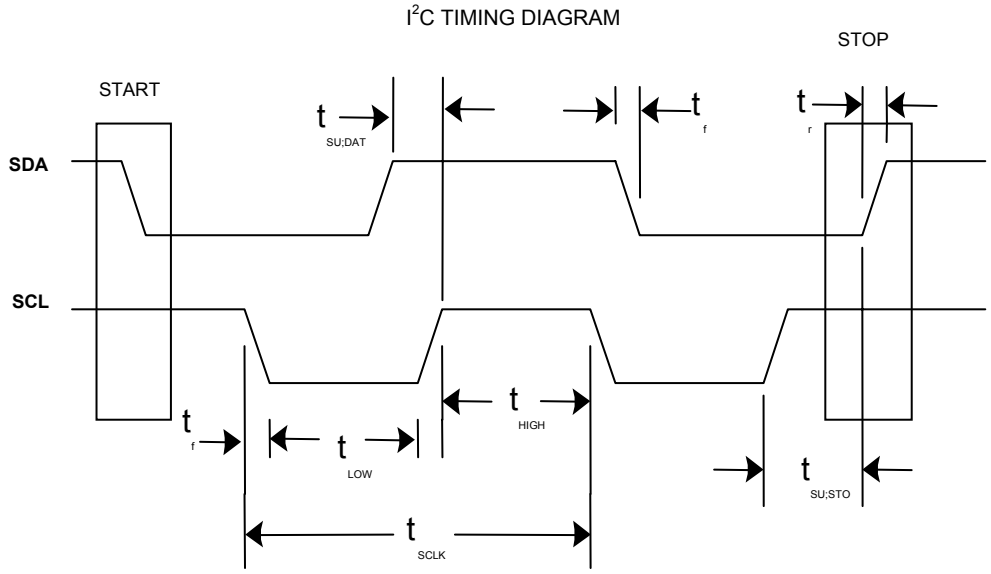
Note 1: V_{SSD} traces should be kept separated back to the V_{SS} supply feed point.

Note 2: V_{CCD} traces should be kept separated back to the V_{CC} supply feed point.

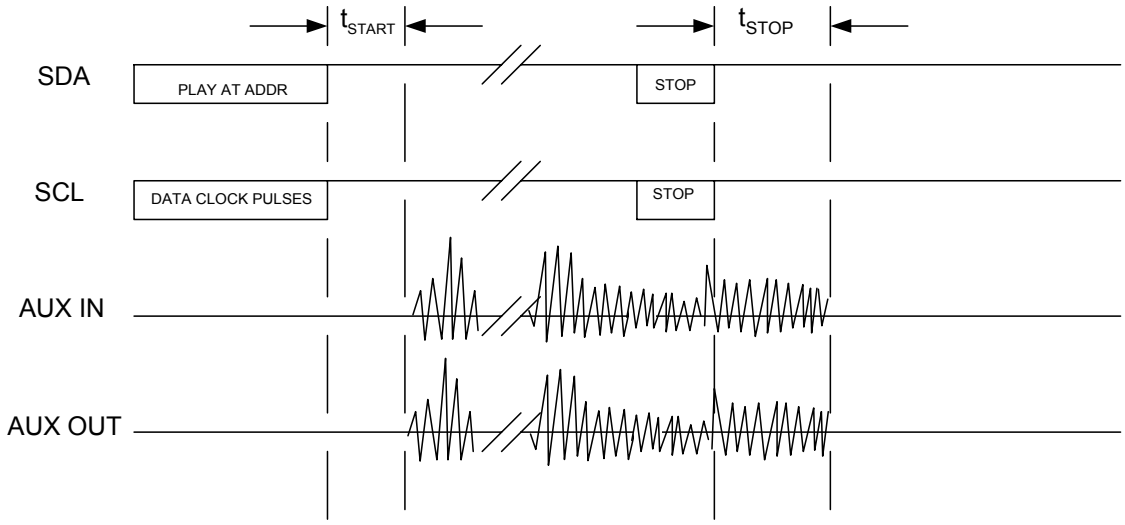
Note 3: The Digital and Analog grounds tie together at the power supply. The V_{CCA} and V_{CCD} supplies will also need filter capacitors (typ. 50 to 100 uF).

8. TIMING DIAGRAMS

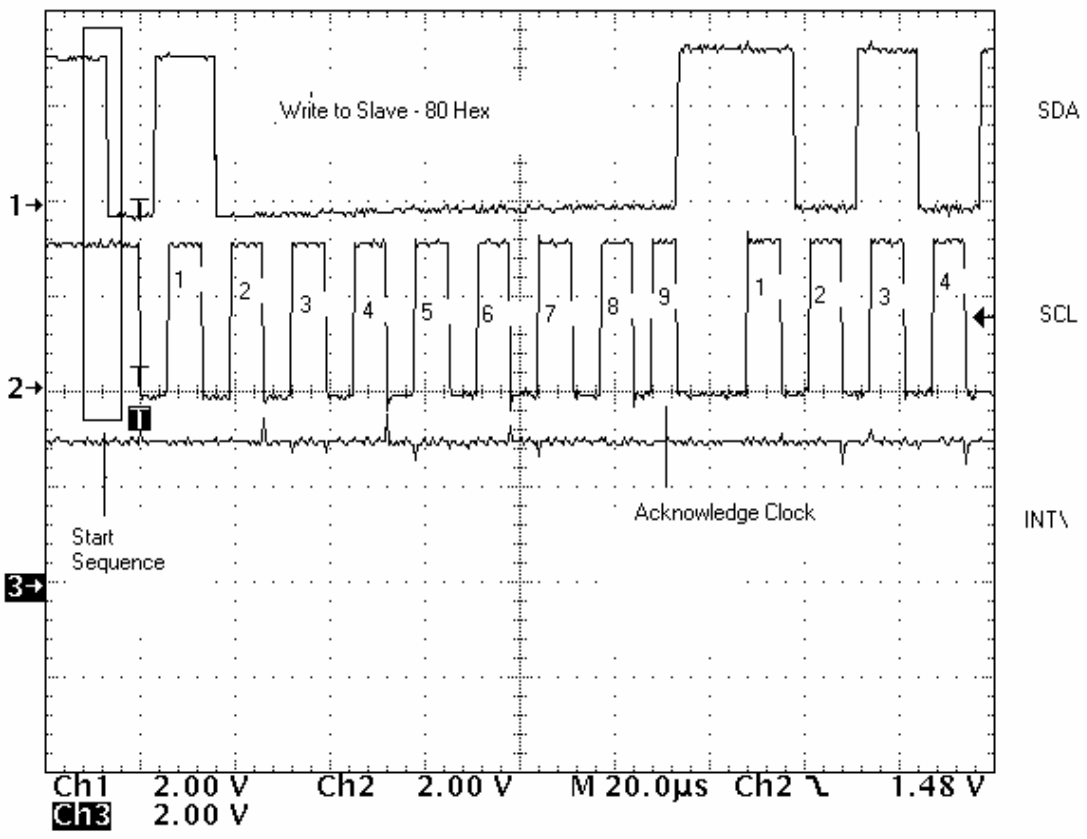
I²C TIMING DIAGRAM



PLAYBACK AND STOP CYCLE



Example of power up command ON THE I2C BUS



I²C INTERFACE TIMING

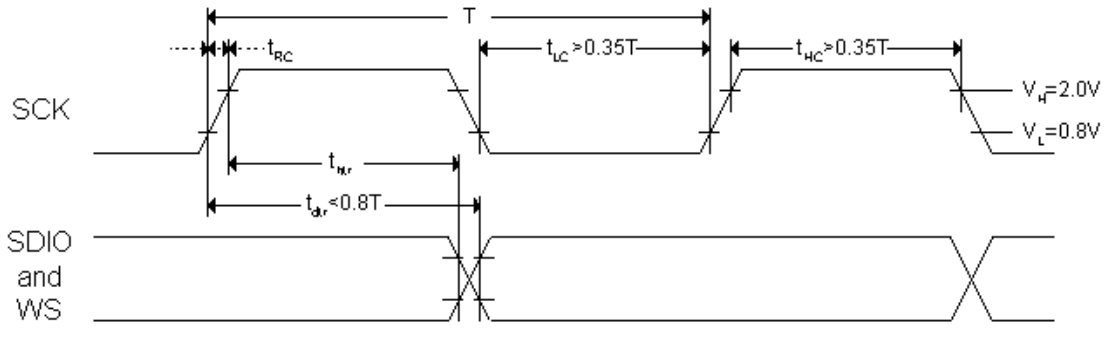
PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;\,STA}$	4.0	-	0.6	-	ns
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	ns
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	ns
Set-up time for a repeated START condition	$t_{SU;\,STA}$	4.7	-	0.6	-	ns
Data set-up time	$t_{SU;\,DAT}$	250	-	100(1)	-	ns
Rise time of both SDA and SCL signals	t_r	-	1000	$20 + 0.1C_b$(2)	300	ns
Fall time of both SDA and SCL signals	t_f	-	300	$20 + 0.1C_b$(2)	300	ns
Set-up time for STOP condition	$t_{SU;\,STO}$	4.0	-	0.6	-	ns
Bus-free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	ns
Capacitive load for each bus line	C_b	-	400	-	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1\ V_{DD}$	-	$0.1\ V_{DD}$	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2\ V_{DD}$	-	$0.2\ V_{DD}$	-	V

1. *A Fast-mode I²C-interface device can be used in a Standard-mode I²C-interface system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal.*

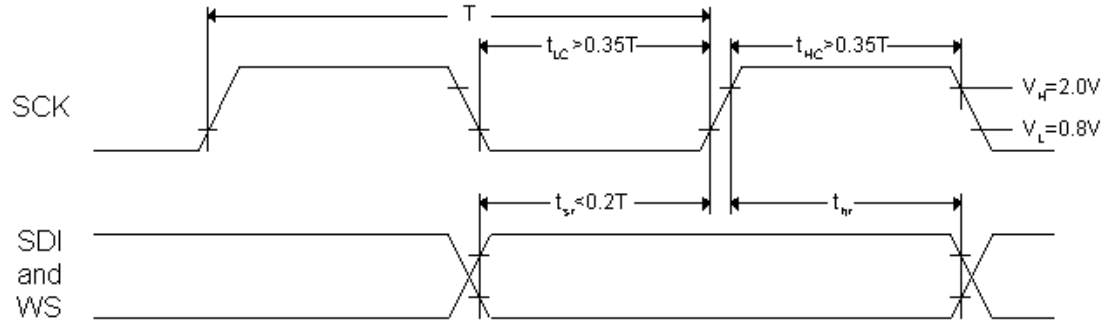
   If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line; $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C -interface specification) before the SCL line is released.

2. *C_b = total capacitance of one bus line in pF. If mixed with HS mode devices, faster fall-times are allowed.*

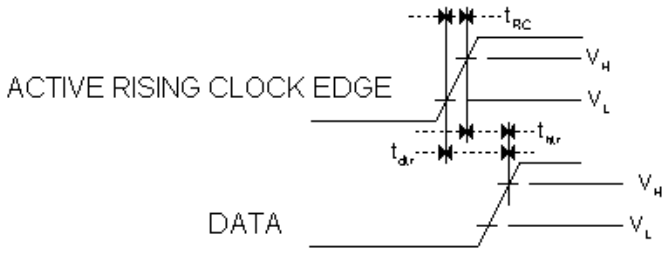
I²S TIMING DIAGRAMS



Timing For I²S Transmitter



Timing For I²S Receiver



Clock rise-time definition with respect to the voltage levels

CODEC Parameters

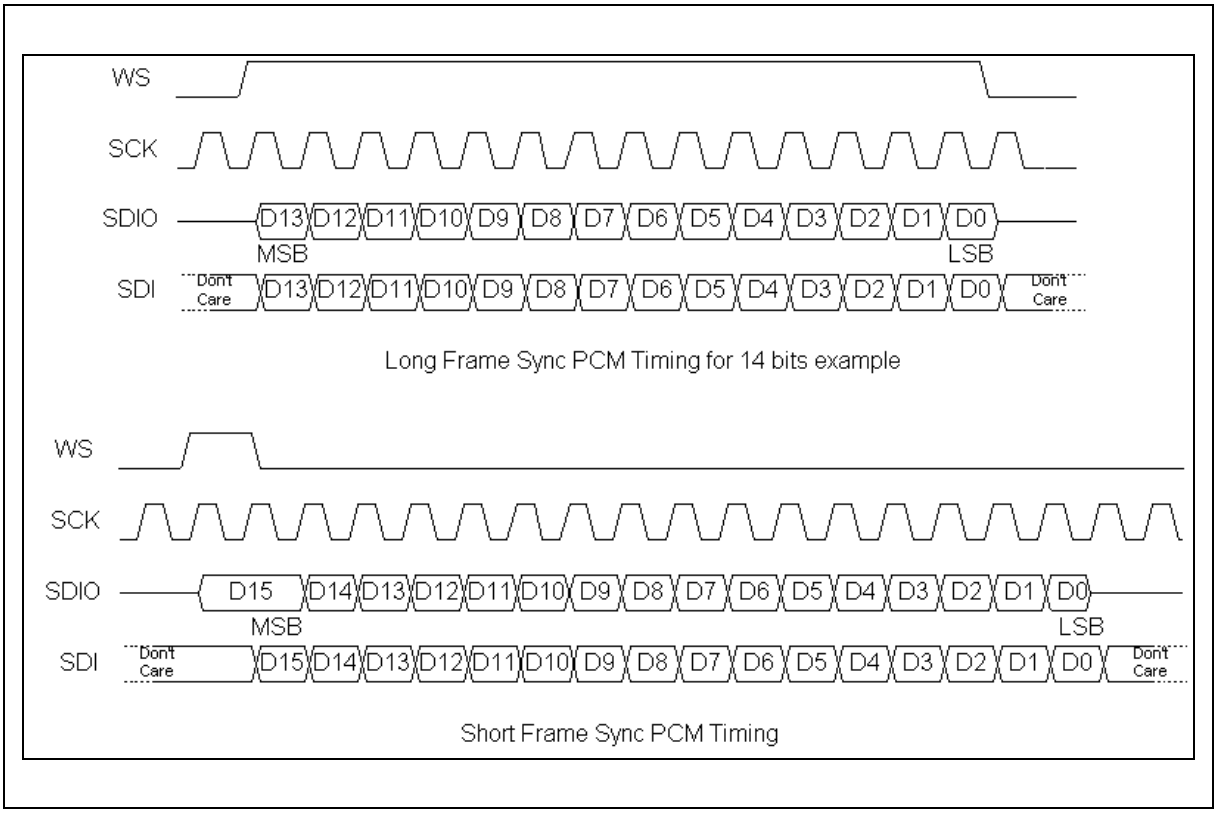
The internal CODEC meets the specification of the ITU-T G.714 recommendation in 8 kHz sampling mode. This specification is verified, using the MIC+/- and SPEAKER+/- pins as analog input and output.

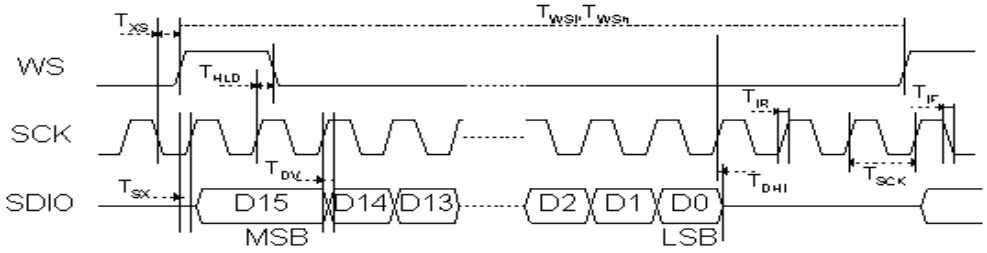
The CODEC μ/A-Law Compander meets the specification of the ITU-T G.711 μ/A-Law companding recommendation

Symbol	Parameters	Min	Typ	Max	Units	Conditions
L_{ABS}	Absolute level				Vrms	0 dBm0 = -2.5dBm @ 600 Ω
T_{XMAX}	Max. Transmit level		2		Vpp	Mic+/Mic- differential
f_{ch1}	High pass filter cut-off frequency		300		Hz	@WS=8kHz, MCLK=13.824MHz
f_{cl1}	Low pass filter cut-off frequency		3400		Hz	@WS=8kHz, MCLK=13.824MHz
f_{cl2}	Low pass filter cut-off frequency	4686	5037	5100	Hz	@ WS=44.1kHz – 48kHz, MCLK=20.48MHz
Δf_{MCLK}	Master clock frequency accuracy	-500	0	+500	ppm	
D_{MCLK}	Master Clock Duty Cycle	48	50	52	%	

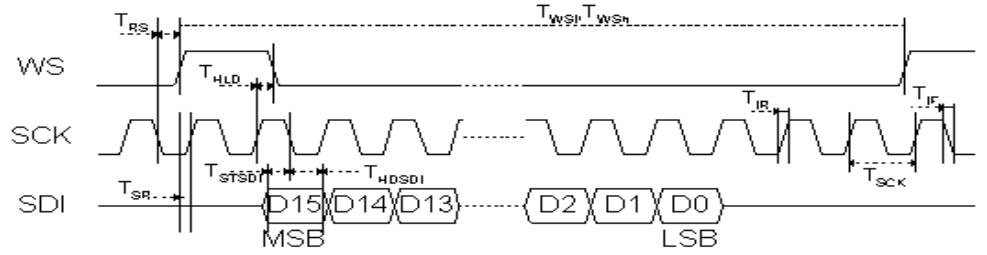
I^2S PARAMETERS (all values in nano seconds)

Parameter	Transmitter				Receiver				NOTES
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Bit Clock period T	325				325				
High time t_{HC}		114				114			
Low time t_{LC}		114				114			
Rise time t_{RC}			49						
Delay t_{dtr}				260					
Hold time t_{htr}	100								
Set-up time t_{sr}						65			
Hold time t_{hr}						0			

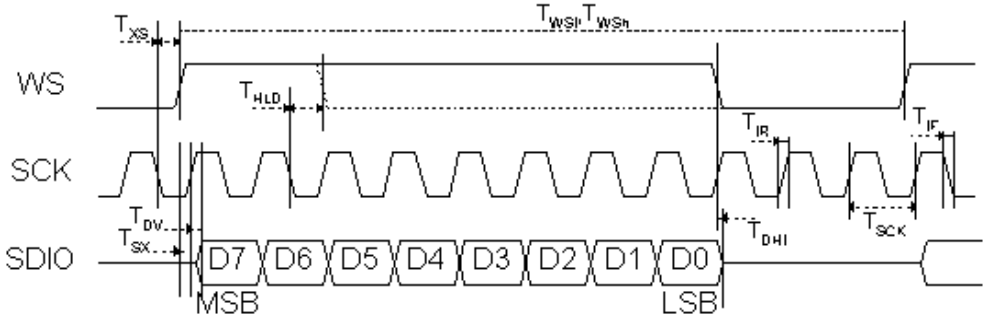

WS
SCK
SDIO
D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
MSB
LSB
SDI
Don't Care
D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
Don't Care
Long Frame Sync PCM Timing for 14 bits example
WS
SCK
SDIO
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
MSB
LSB
SDI
Don't Care
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
Don't Care
Short Frame Sync PCM Timing



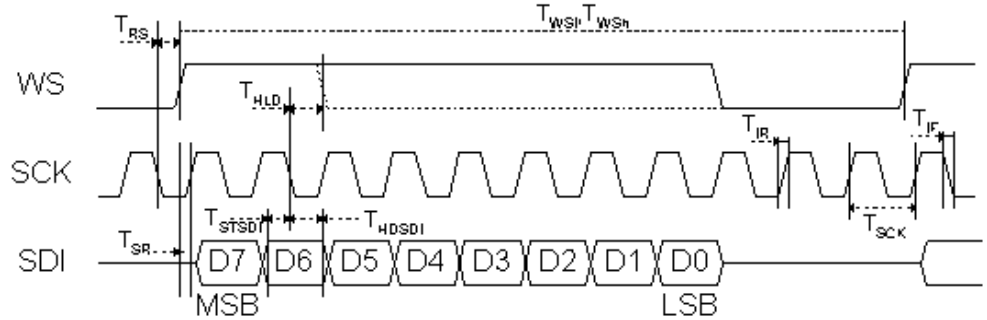
Short Frame Sync Transmit PCM Timing Parameters



Short Frame Sync Receive PCM Timing Parameters



Long Frame Sync Transmit PCM Timing Parameters



Long Frame Sync Receive PCM Timing Parameters

PCM PARAMETERS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bit Clock Frequency	$1/T_{SCK}$	SCK	64	---	3072	kHz
Bit Clock Duty Cycle	D_C	SCK	---	50	---	%
Word Sync. Frequency	$1/T_{WSl}$	WS @ low rate	---	8000	---	Hertz
Word Sync. Frequency	$1/T_{WSh}$	WS @ high rate	44.1	---	48	kHz
Rise Time	T_{IR}	SCK,SDI,SDIO,WS	---	---	50	nsec
Fall Time	T_{IF}	SCK,SDI,SDIO,WS	---	---	50	nsec
Hold Time for 2nd cycle of Bit clock	T_{HLD}	SCK low to WS low	50	---	---	nsec
Transmit Sync. Timing	T_{XS}	SCK to WS	20	---	---	nsec
	T_{SX}	WS to SCK	100	---	---	nsec
Receive Sync. Timing	T_{RS}	SCK to WS	20	---	---	nsec
	T_{SR}	WS to SCK	100	---	---	nsec
Setup Time for SDI valid	T_{STSDI}	---	20	---	---	nsec
Hold Time for SDI valid	T_{HDSDI}	---	50	---	---	nsec
Output Delay Time for SDIO valid	T_{DV}	SCK to SDIO	10	---	120	nsec
Output Delay Time for SDIO High Impedance	T_{DHI}	SCK to SDIO	10	---	120	nsec

9. ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS (Packaged Parts) [1]

Condition	Value
Junction temperature	150^0C
Storage temperature range	-65^0C to $+150^0$C
Voltage Applied to any pin	(V_{SS} - 0.3V) to (V_{CC} + 0.3V)
Voltage applied to any pin (Input current limited to +/-20 mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
Lead temperature (soldering – 10 seconds)	300^0C
V_{CC} - V_{SS}	-0.3V to +5.5V

[1] Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

OPERATING CONDITIONS (Packaged Parts)

Condition	Value
Commercial operating temperature range [1]	0^0C to $+70^0$C
Extended operating temperature [1]	-20^0C to $+70^0$C
Industrial operating temperature [1]	-40^0C to $+85^0$C
Supply voltage (V_{CC}) [2]	+2.7V to +3.3V
Ground voltage (V_{SS}) [3]	0V

[1] Case temperature *[2]* $V_{CC} = V_{CCA} = V_{CCD}$ *[3]* $V_{SS} = V_{SSA} = V_{SSD}$

10. ELECTRICAL CHARACTERISTICS

General Parameters

Symbol	Parameters	Min [2]	Typ [1]	Max [2]	Units	Conditions
V_{IL}	Input Low Voltage			V_{CC} x 0.2	V	
V_{IH}	Input High Voltage	V_{CC} x 0.8			V	
V_{OL}	SCL, SDA, SDIO Output Low Voltage			0.4	V	I_{OL} = 3 mA
V_{OL1}	RAC, $\overline{INT}$ Output Low Voltage			0.4	V	I_{OL} = 1 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OL} = -10 μA
I_{CC}	V_{CC} Current (Operating)					
	- Playback & A/D + D/A		30	50	mA	No Load [3]
	- Record & A/D + D/A		36	56	mA	No Load [3]
	- CODEC A/D + D/A		20	30	mA	No Load [3]
I_{SB}	V_{CC} Current (Standby)		1	10	μA	[3]
I_{IL}	Input Leakage Current			+/-1	μA	

[1] Typical values: T_A = 25°C and Vcc = 3.0 V.

[2] All min/max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} summed together.

TIMING PARAMETERS

Symbol	Parameters	Min [2]	Typ [1]	Max [2]	Units	Conditions
F_S	Sampling Frequency		8.0		kHz	[5]
			6.4		kHz	[5]
			5.3		kHz	[5]
			4.0		kHz	[5]
F_{CF}	Filter Knee					
	8.0 kHz (sample rate)		3.7		kHz	Knee Point [3][7]
	6.4 kHz (sample rate)		2.9		kHz	Knee Point [3][7]
	5.3 kHz (sample rate)		2.5		kHz	Knee Point [3][7]
	4.0 kHz (sample rate)		1.8		kHz	Knee Point [3][7]
T_{REC}	Record Duration					
	8.0 kHz (sample rate)		8.05		min	[6]
	6.4 kHz (sample rate)		10.06		min	[6]
	5.3 kHz (sample rate)		12.15		min	[6]
	4.0 kHz (sample rate)		16.1		min	[6]
T_{PLAY}	Playback Duration					
	8.0 kHz (sample rate)		8.05		min	[6]
	6.4 kHz (sample rate)		10.06		min	[6]
	5.3 kHz (sample rate)		12.15		min	[6]
	4.0 kHz (sample rate)		16.1		min	[6]
T_{PUD}	Power-Up Delay					
	8.0 kHz (sample rate)		1		msec	
	6.4 kHz (sample rate)		1		msec	
	5.3 kHz (sample rate)		1		msec	
	4.0 kHz (sample rate)		1		msec	
T_{STOP} OR $_{PAUSE}$	Stop or Pause					
	Record or Play					
	8.0 kHz (sample rate)		32		msec	
	6.4 kHz (sample rate)		40		msec	
	5.3 kHz (sample rate)		48		msec	
	4.0 kHz (sample rate)		64		msec	

Symbol	Parameters	Min [2]	Typ [1]	Max [2]	Units	Conditions
T_{RAC}	RAC Clock Period					
	8.0 kHz (sample rate)		256		msec	[9]
	6.4 kHz (sample rate)		320		msec	[9]
	5.3 kHz (sample rate)		386		msec	[9]
	4.0 kHz (sample rate)		512		msec	[9]
T_{RACLO}	RAC Clock Low Time					
	8.0 kHz (sample rate)		8		msec	
	6.4 kHz (sample rate)		10		msec	
	5.3 kHz (sample rate)		12.1		msec	
	4.0 kHz (sample rate)		16		msec	
T_{RACM}	RAC Clock Period in Message Cueing Mode					
	8.0 kHz (sample rate)		500		msec	
	6.4 kHz (sample rate)		625		msec	
	5.3 kHz (sample rate)		750		msec	
	4.0 kHz (sample rate)		1000		msec	
TRACML	RAC Clock Low Time in Message Cueing Mode					
	8.0 kHz (sample rate)		15.6		msec	
	6.4 kHz (sample rate)		19.5		msec	
	5.3 kHz (sample rate)		23.4		msec	
	4.0 kHz (sample rate)		31.2		msec	
THD	Total Harmonic Distortion					@1 KHz at 0TLP, sample rate = 5.3 KHz
	AUX IN to ARRAY,		1	2	%	
	ARRAY to SPKR		1	2	%	

ANALOG PARAMETERS

MICROPHONE INPUT [14]

Symbol	Parameters	Min (2)	Typ (1)(14)	Max (2)	Units	Conditions
$V_{MIC+/-}$	MIC +/- Input Voltage			300	mV	Peak-to-Peak [4][8]
$V_{MIC\ (0TLP)}$	MIC +/- input reference transmission level point (0TLP)		208		mV	Peak-to-Peak [4][10]
$A_{MIC\ (GT)}$	MIC +/- Gain Tracking		+/-0.1		dB	1 kHz, +3 to –40 dB 0TLP Input
R_{MIC}	Microphone input resistance		10		kΩ	MIC- and MIC+ pins
A_{AGC}	Microphone AGC Amplifier Range	6		40	dB	Over 3-300 mV Range
V_{MICBS}	Microphone Bias Voltage		2.2		V	I_{MICBS} = 0.0 mA
R_{MICBS}	MICBS Output Resistance		700		Ω	

AUX IN [14]

Symbol	Parameters	Min (2)	Typ (1)(14)	Max (2)	Units	Conditions
$V_{AUX\ IN}$	AUX IN Input Voltage			1.0	V	Peak-to-Peak (0 dB gain setting)
$V_{AUX\ IN\ (0TLP)}$	AUX IN (0TLP) Input Voltage		694.2		mV	Peak-to-Peak (0 dB gain setting)
$A_{AUX\ IN\ (GA)}$	AUX IN Gain Accuracy	-0.5		+0.5	dB	[11]
$A_{AUX\ IN\ (GT)}$	AUX IN Gain Tracking		+/-0.1		dB	1000 Hz, +3 to –45 dB 0TLP Input, 0 dB setting
$R_{AUX\ IN}$	AUX IN Input Resistance		10 to 100		kΩ	Depending on AUX IN Gain

SPEAKER OUTPUTS [14]

Symbol	Parameters	Min [2]	Typ [1][14]	Max [2]	Units	Conditions
V_{SPHG}	SP+/- Output Voltage (High Gain Setting)			3.6	V	Peak-to-Peak, differential load = 150Ω, OPA1, OPA0 = 01
R_{SPLG}	SP+/- Output Load Imp. (Low Gain)	8			Ω	OPA1, OPA0 = 10
R_{SPHG}	SP+/- Output Load Imp. (High Gain)	70	150		Ω	OPA1, OPA0 = 01
C_{SP}	SP+/- Output Load Cap.			100	pF	
V_{SPAG}	SP+/- Output Bias Voltage (Analog Ground)		1.2		VDC	
V_{SPDCO}	Speaker Output DC Offset			+/-100	mV DC	With CODEC D/A IN to Speaker.
PSRR	Power Supply Rejection Ratio		-55		dB	Measured with a 1 kHz, 100 ma_p sine wave input at V_{CC} and V_{CC} pins
F_R	Frequency Response (300-3400 Hz)	-0.25		+0.25	dB	With 0TLP input to AUX IN, 6 dB setting (12)
P_{OUTLG}	Power Output (Low Gain Setting)	23.5			mW RMS	Differential load at 8Ω

AUX OUT [14]

Symbol	Parameters	Min [2]	Typ [1][14]	Max [2]	Units	Conditions
$V_{AUX\ OUT}$	AUX OUT – Maximum Output Swing			1.0	V	5kΩ Load
R_L	Minimum Load Impedance	5			KΩ	
C_L	Maximum Load Capacitance			100	pF	
V_{BIAS}	AUX OUT		1.2		VDC	

VOLUME CONTROL [14]

Symbol	Parameters	Min [2]	Typ [1][14]	Max [2]	Units	Conditions
A_{OUT}	Output Gain		-28 to 0		dB	8 steps of 4 dB, referenced to output
	Absolute Gain	-0.5		+0.5	dB	AUX IN 1.0 kHz 0TLP, 6 dB gain setting measured differentially at SP+/-

[1] Typical values: T_A = 25°C and Vcc = 3.0V.

[2] All min/max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).

[4] Differential input mode. Nominal differential input is 208 mV p-p. (0TLP)

[5] Sampling frequency can vary as much as –6/+4 percent over the industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).

[6] Playback and Record Duration can vary as much as –6/+4 percent over the industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).

[7] Filter specification applies to the low pass filter.

[8] For optimal signal quality, this maximum limit is recommended.

[9] When a record command is sent, T_{RAC} = T_{RAC} + T_{RACLO} on the first page addressed.

[10] The maximum signal level at any input is defined as 3.17 dB higher than the reference transmission level point. (0TLP) This is the point where signal clipping may begin.

[11] Measured at 0TLP point for each gain setting. See AUX IN table.

[12] 0TLP is the reference test level through inputs and outputs. See AUX IN table.

[13] Referenced to 0TLP input at 1 kHz, measured over 300 to 3,400 Hz bandwidth.

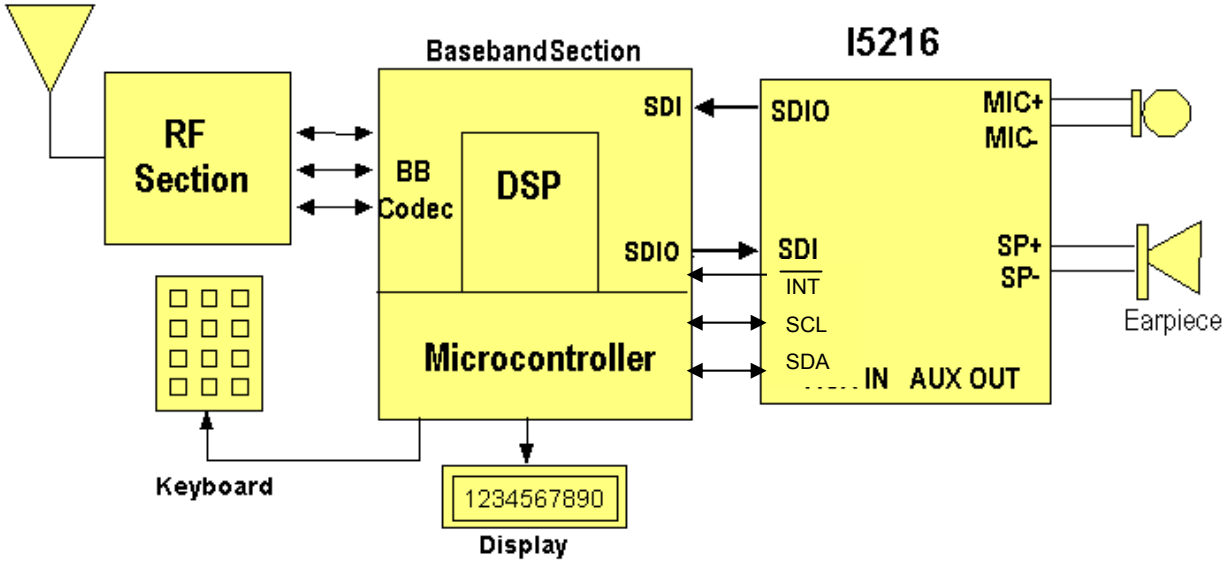
[14] For die, only typical values are applicable.

11. TYPICAL APPLICATION CIRCUIT

APPLICATIONS

The ISD5216 is a single chip solution for voice and analog storage that also includes the capability to store digital information in the memory array. The array may be divided between analog and digital storage, as the user chooses, when configuring the device.

Looking at the block diagram on the following page, one can see that the ISD5216 may be very easily designed into a cellular phone. Placing the device between the microphone and the existing baseband chip takes care of the transmit path. The SDI/SDIO of the baseband chip is connected to the SDIO/SDI of the ISD5216. Two pins are needed for the I^2C digital control and digital information for storage.



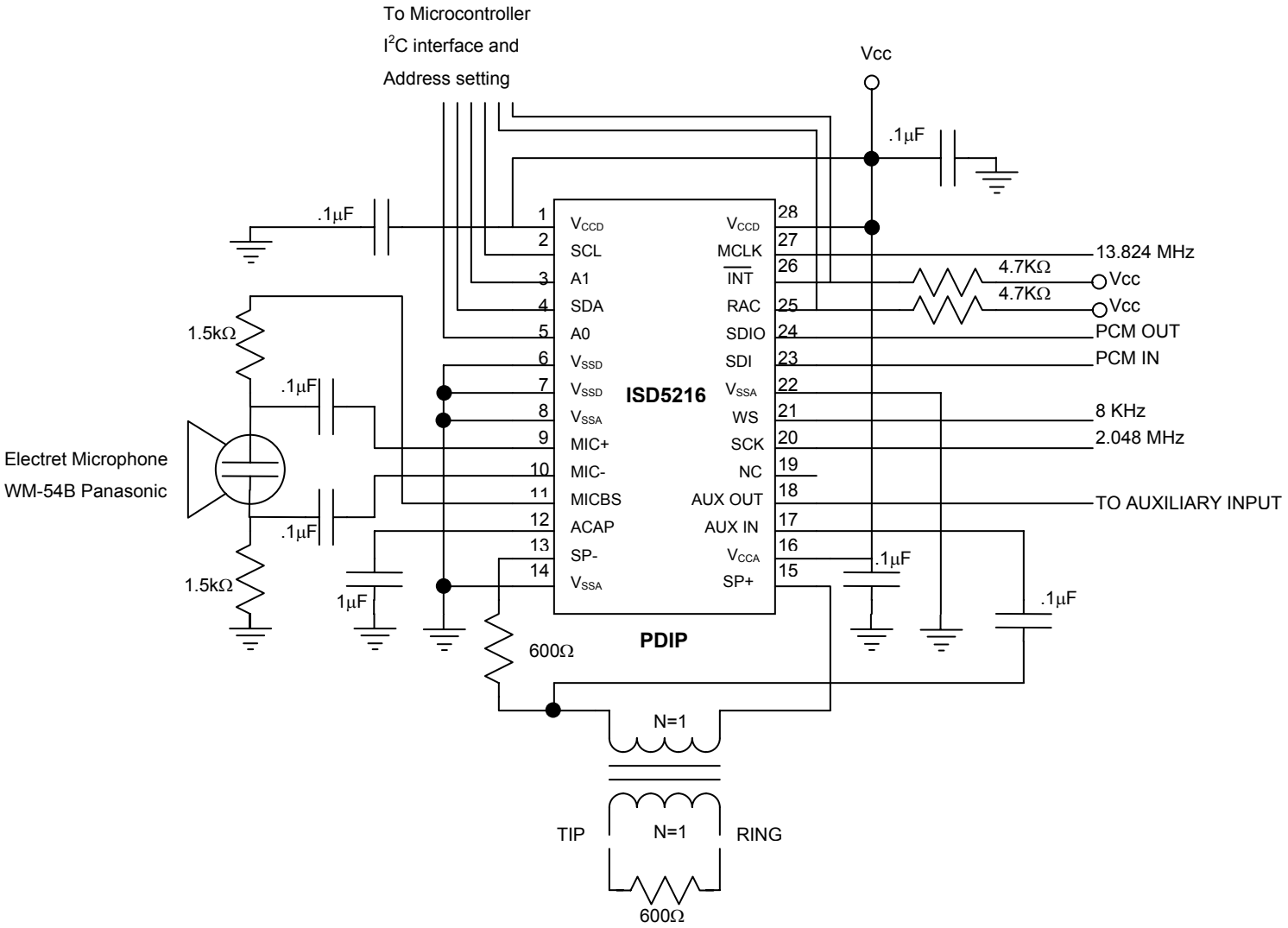
Starting at the MICROPHONE inputs, the input signal at the MICROPHONE inputs can be routed in the following ways:

- directly through the Voice band CODEC of the ISD5216 chip, then through the SDIO pin, to output the digital PCM signal.
- through the AGC amplifier, before it is routed to the voice band CODEC.
- through the AGC amplifier to the storage array
- through the AGC amplifier and mixed with an analog voice band CODEC signal coming from the digital SDI pin

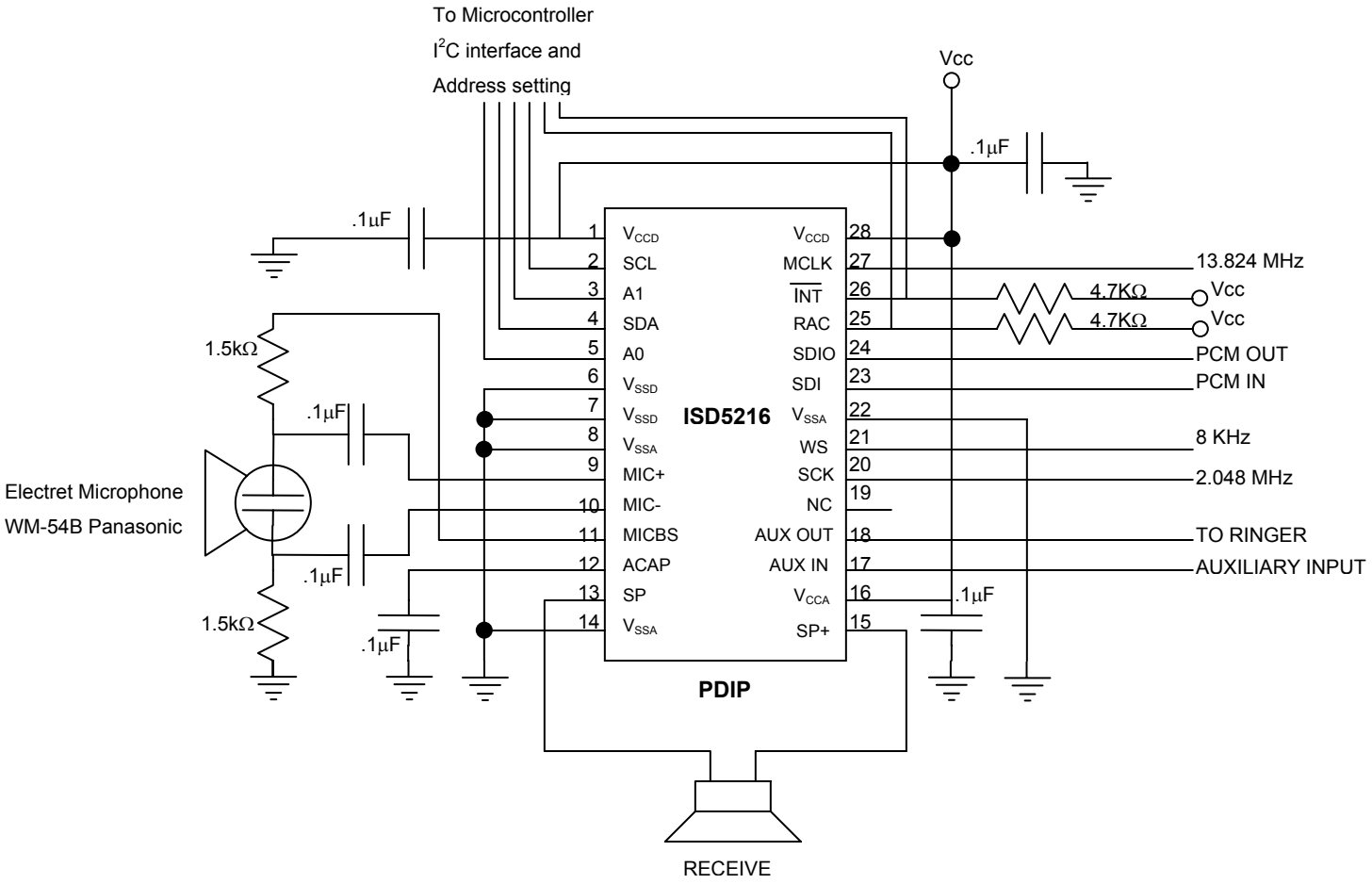
In addition, if the phone is inserted into a "hands-free" car kit, then the signal from the pickup microphone in the car can be passed through to the same places from the AUX IN pin and the phone's microphone is switched off. In this scenario, the other party's voice from the phone would be played into the PCM IN input and passed through to the AUX OUT pin that would drive the car kit's loudspeaker.

Depending upon whether one desires recording one side (simplex) or both sides (duplex) of a conversation, the various paths will also be switched through to the low pass filter (for antialiasing) and into the storage array. Later, the cell phone owner can play back the messages from the array. When this happens, the Array Output MUX is connected to the volume control, through the Output MUX, to the Speaker Amplifier. For applications other than a cell phone, the audio paths can be switched into many different and flexible configurations. Some examples follow.

TRANSFORMER APPLICATION

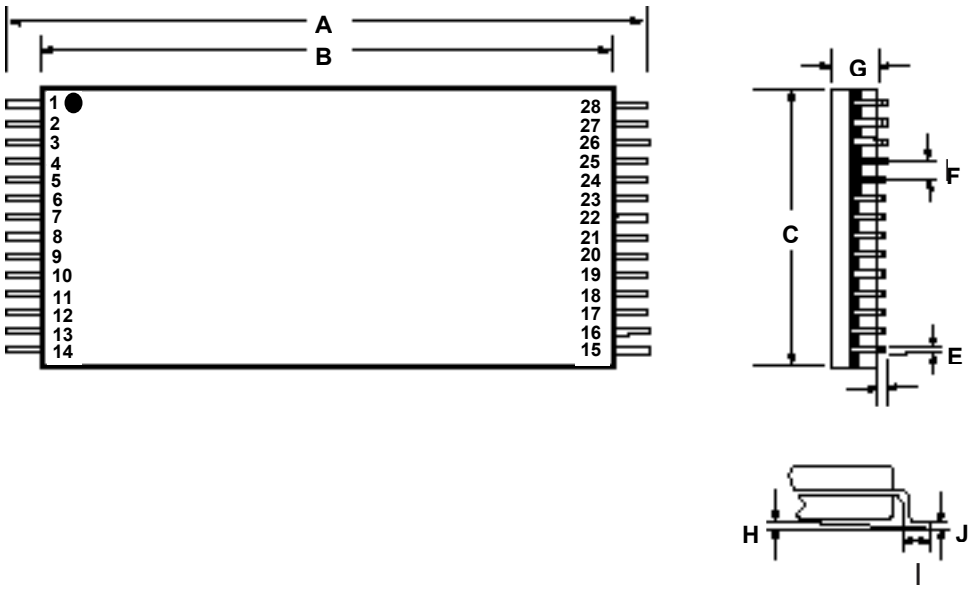


HANDSET APPLICATION



12. PACKAGE SPECIFICATIONG

12.1. PLASTIC THIN SMALL OUTLINE PACKAGE (TSOP) TYPE E DIMENSIONS

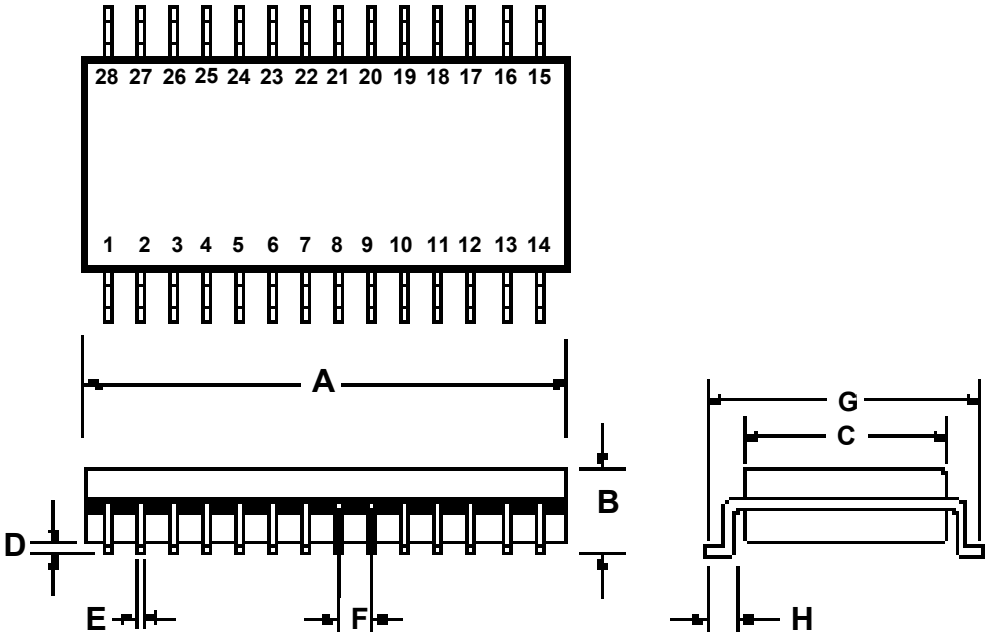


PLASTIC THIN SMALL OUTLINE PACKAGE (TSOP) TYPE E DIMENSIONS

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0^0	3^0	6^0	0^0	3^0	6^0
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

Note: *Lead coplanarity to be within 0.004 inches.*

12.2. PLASTIC SMALL OUTLINE INTEGRATED CIRCUIT (SOIC) DIMENSIONS

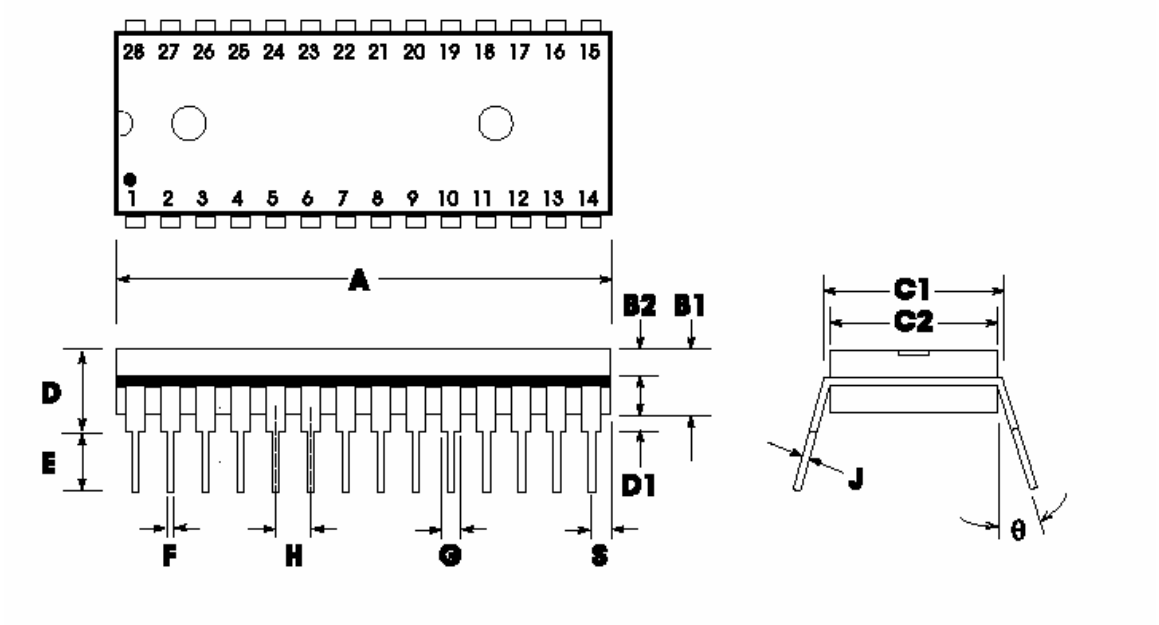


Plastic Small Outline Integrated Circuit (SOIC) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

Note: *Lead coplanarity to be within 0.004 inches.*

12.3. PLASTIC DUAL INLINE PACKAGE (PDIP) DIMENSIONS

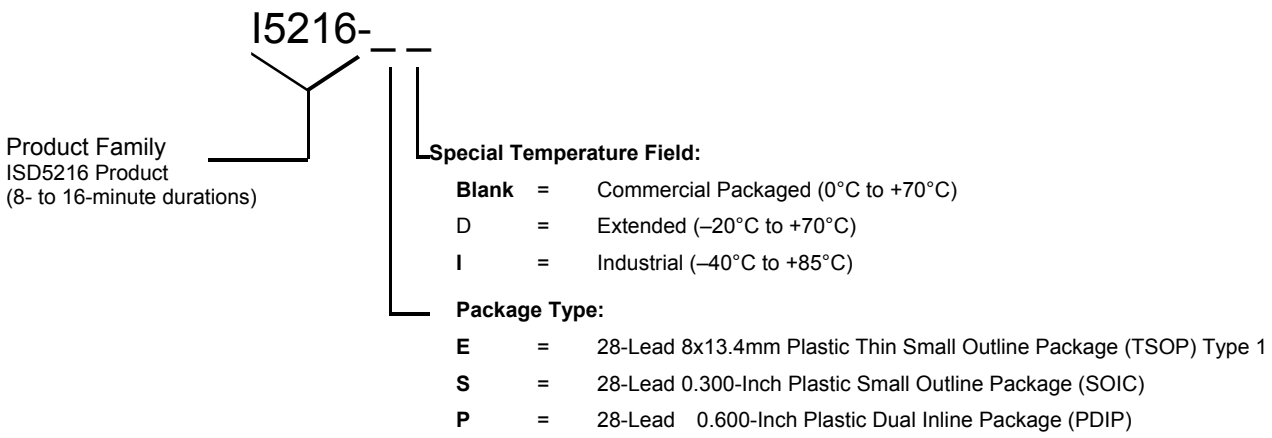


Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
0	0°		15°	0°		15°

13. ORDERING INFORMATION

Winbond Part Number Description



When ordering ISD5216 series devices, please refer to the following valid part numbers.

Part Number	Part Number
I5216E	I5216S
I5216ED	I5216P
I5216EI	I5216SI

Chip scale package is available upon customer's request. For the latest product information, access Winbond's worldwide website at http://www.winbond-usa.com

14. VERSION HISTORY

VERSION	DATE	DESCRIPTION
A1	Nov. 2001	Initial issue
B.1	Aug. 2002	Overall updates, not available in die form
B.2	Jun. 2003	Update cover page Replace all I5216 by ISD5216
B.3	Apr. 2005	Revise disclaim section

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Information contained in this ISD® ChipCorder® datasheet supersedes all data for the ISD ChipCorder products published by ISD® prior to August, 1998.

This datasheet and any future addendum to this datasheet is(are) the complete and controlling ISD® ChipCorder® product specifications. In the event any inconsistencies exist between the information in this and other product documentation, or in the event that other product documentation contains information in addition to the information in this, the information contained herein supersedes and governs such other information in its entirety. This datasheet is subject to change without notice.

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