



# 21150 PCI-to-PCI Bridge

## Brief Datasheet

### Product Features

Intel's 21150 is a PCI-to-PCI bridge that is fully compliant with *PCI Local Bus Specification*, Revision 2.1, and the *Advanced Configuration Power Interface (ACPI) Specification*. The 21150 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions.

- Complies fully with Revision 2.1 of the *PCI Local Bus Specification*
- Complies fully with the *PCI Bus Power Management Specification*
- Complies fully with the *Advanced Configuration Power Interface (ACPI) Specification*
- Allows 72 bytes of read data buffering in each direction
- Includes live insertion support
- Provides ten secondary clock outputs:
  - Low skew, permitting direct drive of option slots
  - Individual clock disables, capable of automatic configuration during reset
- Supports both 5-V and 3.3-V signaling environments
- Allows 88 bytes of buffering (data and address) for posted memory write commands in each direction—up to 5 posted write transactions simultaneously in each direction
- Provides enhanced address decoding:
  - A 32-bit I/O address range
  - A 32-bit memory-mapped I/O address range
  - A 64-bit prefetchable memory address range
  - ISA-aware mode for legacy support in the first 64 KB of I/O address range
- Provides VGA addressing and VGA palette snooping support
- Provides concurrent primary and secondary bus operation to isolate traffic
- Provides a 4-pin general-purpose I/O interface, accessible through device-specific configuration space
- Available in both 33 MHz and 66 MHz versions
- Includes downstream lock support
- Provides arbitration support for nine secondary bus devices:
  - A programmable 2-level arbiter
  - Hardware disable control, permitting use of an external arbiter
- Provides an IEEE standard 1149.1 JTAG interface
- Implements delayed transactions for all PCI configuration, I/O, and memory read commands—up to three transactions simultaneously in each direction
- Supports PCI transaction forwarding for the following commands:
  - All I/O and memory commands
  - Type 1 to Type 1 configuration commands
  - Type 1 to Type 0 configuration commands (downstream only)
  - All Type 1 to special cycle configuration commands



## Description

The 21150 has separate posted write, read data, and delayed transaction queues with significant buffering capability. In addition, the 21150 supports buffering of simultaneous, multiple, posted write and delayed transactions in both directions.

Among the features of the 21150 are:

- A programmable 2-level secondary bus arbiter
- An IEEE standard 1149.1 JTAG interface
- Live insertion support
- A 4-pin general-purpose I/O interface
- Individual secondary clock disables
- Enhanced address decoding

The 21150 has sufficient clock and arbitration pins to support nine PCI bus master devices directly on its secondary interface.

The 21150 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications such as multimedia.

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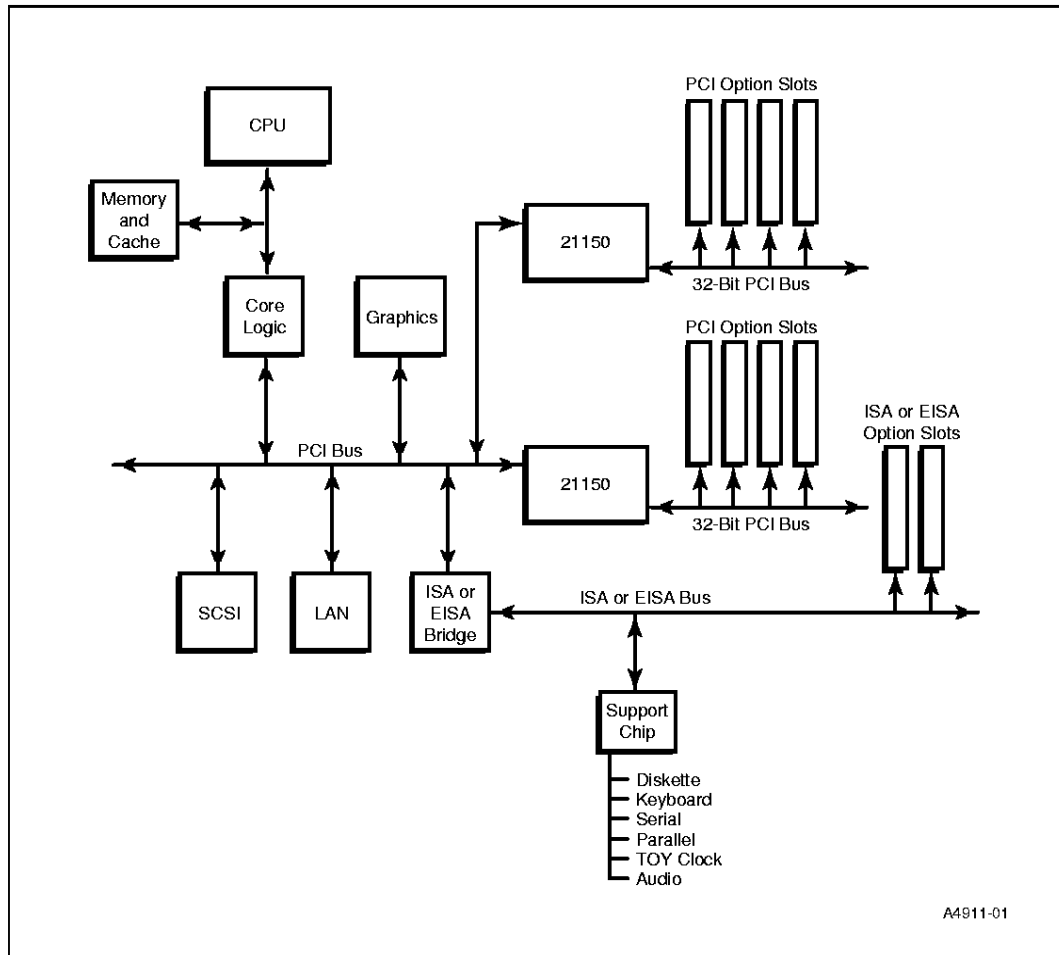
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## Applications

The 21150 makes it possible to extend a system's load capability limit beyond that of a single PCI bus by allowing motherboard designers to add more PCI devices, or more PCI option card slots, than a single PCI bus can support. Figure 1, the system card block diagram illustrates the use of two PCI-to-PCI bridges on a system board. Each 21150 added to the board creates a new PCI bus that provides support for the additional PCI slots or devices.

Figure 1. System Card Block Diagram

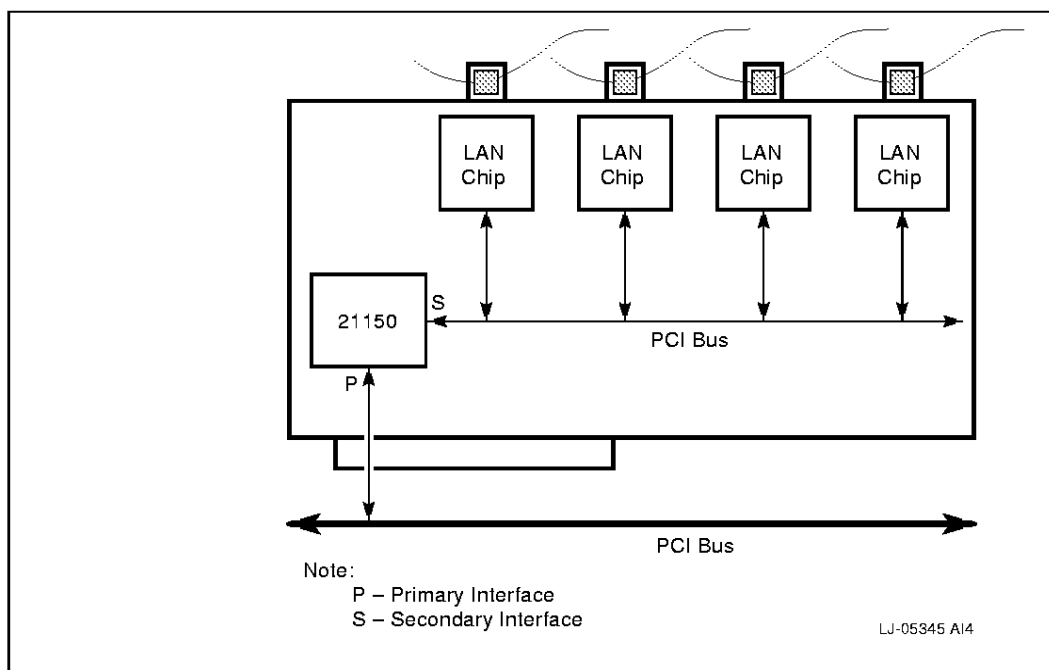


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## Multidevice PCI Option Cards

Option card designers can use the 21150 to implement multiple-device PCI option cards. Without a PCI-to-PCI bridge, PCI loading rules would limit option cards to one device. The *PCI Local Bus Specification* loading rules limit PCI option cards to a single connection per PCI signal in the option card connector. However, the 21150 overcomes this restriction by providing, on the option card, an independent PCI bus to which up to nine devices can be attached. Figure 2, the 21150 with option cards diagram illustrates how the 21150 enables the design of a multicomponent option card.

Figure 2. 21150 with Option Cards



Characteristics	Specifications
Power supply	Vdd 3.3 V Vdd_clamp=5 V or 3.3 V
Operating temperature	T <sub>J</sub> maximum = 125°C
Storage temperature range	-55°C to +125°C (-67°F to 257°F)
Power dissipation (typical)	1.2 W @ Vdd=3.3 V with 33-MHz PCI Clock
Package	208-pin PQFP



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