
HN62428 Series

524,288-word x 16-bit / 1,048,576-word x 8-bit CMOS
Programmable Mask ROM

HITACHI

The HN62428 Series is a 8-Mbit CMOS Programmable Mask ROM organized either as 524,288 words by 16 bits or as 1,048,576 words by 8 bits. It can be operated with a battery because of low power consumption.

Features

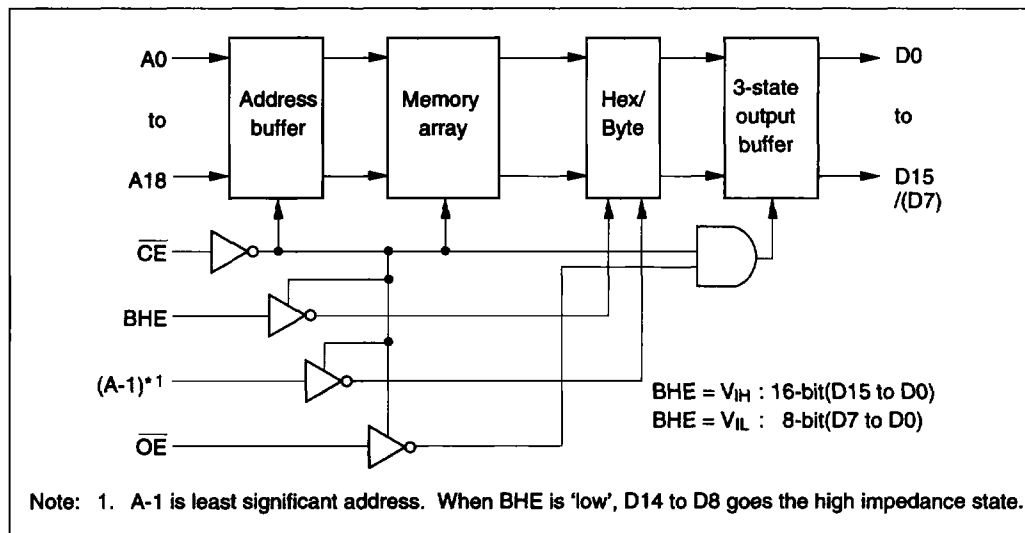
- Single 5 V
- Wired OR is permitted for the output in three states.
- TTL compatible
- Address access time: 150/200 ns (max)
- Low power consumption: 100 mW (typ) active
5 μ W (typ) standby
- Byte-wide or word-wide data organization (switched by BHE terminal)

Ordering Information

Type No.	Access time	Package
HN62428P-15/-20	150/200 ns	600 mil 42-pin plastic DIP (DP-42)
HN62428TT-15/-20	150/200 ns	44-pin plastic TSOP-II (TTP-44D)
HN62428FB-15/-20	150/200 ns	44-pin plastic SOP (FP-44D)

HN62428 Series

Block Diagram



Pin Arrangement

HN62428P

A18	1	42	NC
A17	2	41	A8
A7	3	40	A9
A6	4	39	A10
A5	5	38	A11
A4	6	37	A12
A3	7	36	A13
A2	8	35	A14
A1	9	34	A15
A0	10	33	A16
$\overline{CE}$	11	32	BHE
V _{SS}	12	31	V _{SS}
OE	13	30	D15/A-1
D0	14	29	D7
D8	15	28	D14
D1	16	27	D6
D9	17	26	D13
D2	18	25	D5
D10	19	24	D12
D3	20	23	D4
D11	21	22	V _{CC}

(Top View)

HN62428TT

NC	1	44	NC
A18	2	43	NC
A17	3	42	A8
A7	4	41	A9
A6	5	40	A10
A5	6	39	A11
A4	7	38	A12
A3	8	37	A13
A2	9	36	A14
A1	10	35	A15
A0	11	34	A16
$\overline{CE}$	12	33	BHE
V _{SS}	13	32	V _{SS}
OE	14	31	D15/A-1
D0	15	30	D7
D8	16	29	D14
D1	17	28	D6
D9	18	27	D13
D2	19	26	D5
D10	20	25	D12
D3	21	24	D4
D11	22	23	V _{CC}

(Top View)

HN62428FB

NC	1	44	NC
A18	2	43	NC
A17	3	42	A8
A7	4	41	A9
A6	5	40	A10
A5	6	39	A11
A4	7	38	A12
A3	8	37	A13
A2	9	36	A14
A1	10	35	A15
A0	11	34	A16
$\overline{CE}$	12	33	BHE
V _{SS}	13	32	V _{SS}
OE	14	31	D15/A-1
D0	15	30	D7
D8	16	29	D14
D1	17	28	D6
D9	18	27	D13
D2	19	26	D5
D10	20	25	D12
D3	21	24	D4
D11	22	23	V _{CC}

(Top View)

HN62428 Series

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Terminal voltage	V_{in} , V_{out}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Bias temperature	T_{bias}	-20 to +85	°C

Note: With respect to V_{SS} .

Recommended DC Operating Conditions ($V_{SS} = 0$ V, $T_a = 0$ to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
	V_{IL}	-0.3	—	0.8	V

DC Characteristics ($V_{CC} = 5$ V $\pm$ 10%, $V_{SS} = 0$ V, $T_a = 0$ to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Power supply current	Active	I_{CC}	—	50	mA	$V_{CC} = 5.5$ V, $I_{DOUT} = 0$ mA, $t_{RC} = \min$
	Standby	I_{SB}	—	30	μ A	$V_{CC} = 5.5$ V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leak current		$ I_{LI} $	—	10	μ A	$V_{in} = 0$ to V_{CC}
Output leak current		$ I_{LO} $	—	10	μ A	$\overline{CE} = 2.2$ V, $V_{out} = 0$ to V_{CC}
Output voltage		V_{OH}	2.4	—	V	$I_{OH} = -205$ μ A
		V_{OL}	—	0.4	V	$I_{OL} = 1.6$ mA

Capacitance ($V_{CC} = 5$ V $\pm$ 10%, $V_{SS} = 0$ V, $T_a = 25^\circ\text{C}$, $V_{IN} = 0$ V, $f = 1$ MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	C_{in}	—	15	pF
Output capacitance	C_{out}	—	15	pF

Note: This parameter is sampled and not 100% tested.

AC Operating Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }+70^\circ\text{C}$)

Test Conditions

- Input pulse level: 0.8 to 2.4 V
- I/O timing reference level: 1.5 V
- Input rise/fall time: 10 ns
- Output load: 1 TTL gate + $C_L = 100\text{ pF}$ (including jig capacitance)

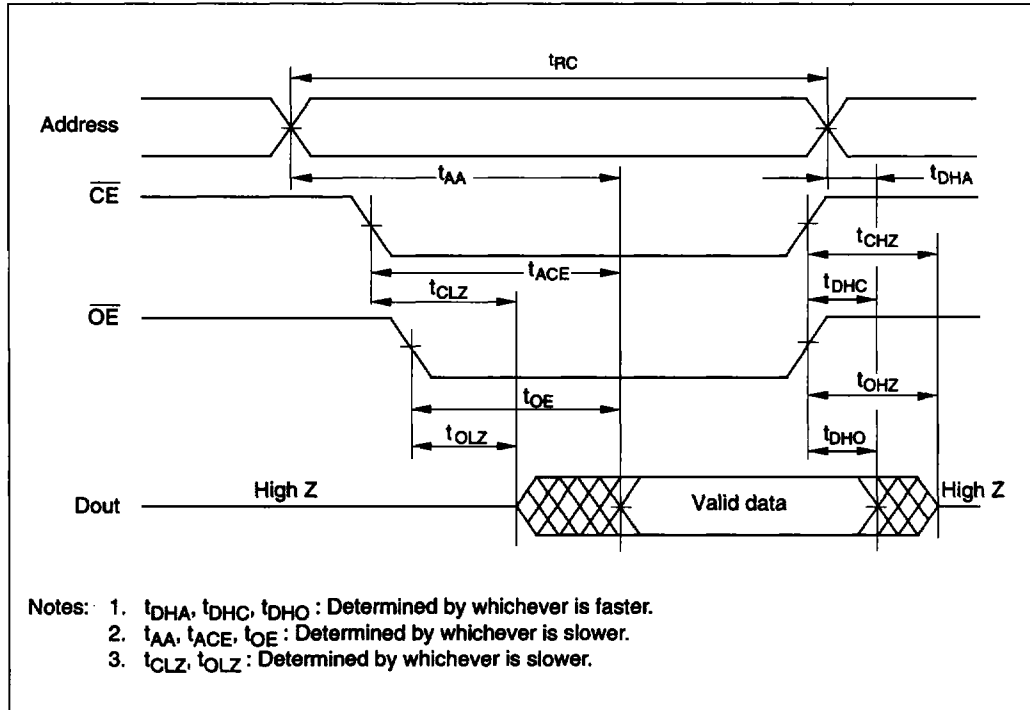
Item	Symbol	HN62428-15		HN62428-20		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
BHE access time	t_{BHE}	—	150	—	200	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to output in high-Z	t_{CHZ}^{*1}	—	70	—	70	ns
$\overline{OE}$ to output in high-Z	t_{OHZ}^{*1}	—	70	—	70	ns
BHE to output in high-Z	t_{BHZ}^{*1}	—	70	—	70	ns
$\overline{CE}$ to output in low-Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to output in low-Z	t_{OLZ}	10	—	10	—	ns
BHE to output in low-Z	t_{BLZ}	10	—	10	—	ns

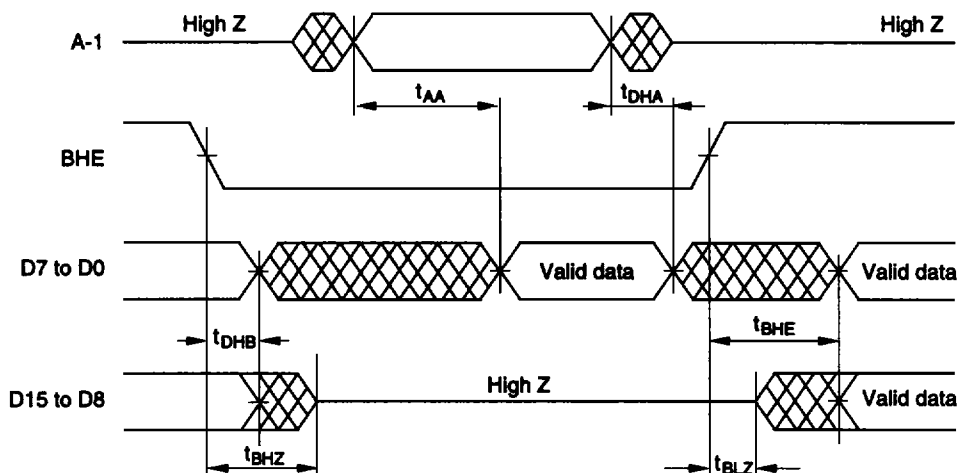
Note: ^{*1} t_{CHZ} , t_{OHZ} and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

HN62428 Series

Timing Waveform

Word Mode (BHE = "V_{IH}") or Byte Mode (BHE = "V_{IL}")

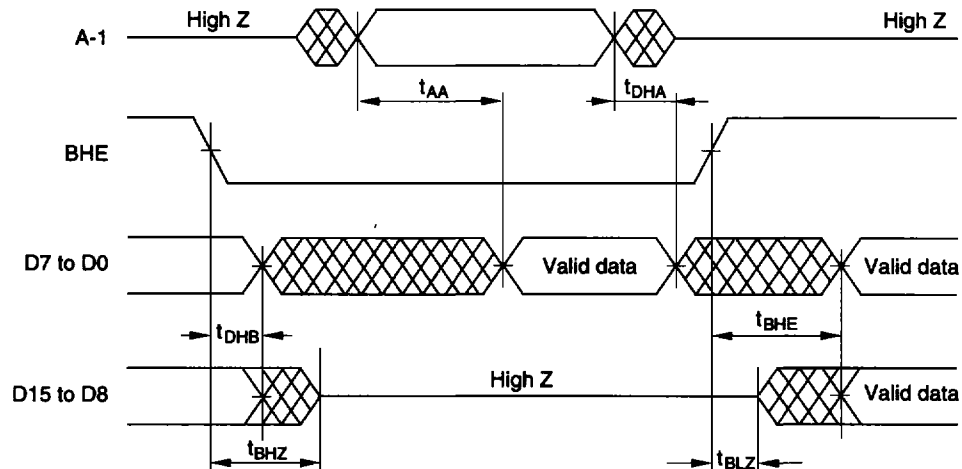


Switching between Word Mode and Byte Mode


- Notes:
1. $\overline{CE}$, $\overline{OE}$ are of selected status. A18 – A0 are fixed.
 2. D15/A-1 terminal is of output state when BHE = V_{IH} . $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

HN62428 Series

Switching between Word Mode and Byte Mode

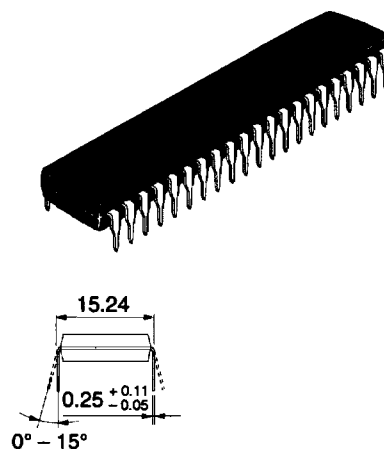
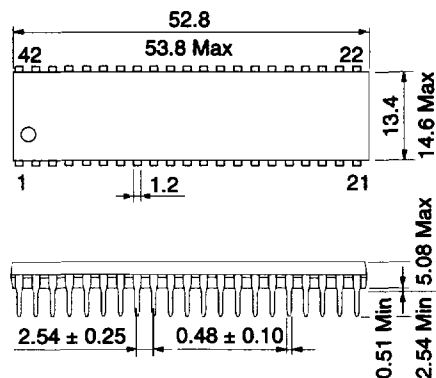


- Notes:
1. $\overline{CE}$, $\overline{OE}$ are of selected status. A18 – A0 are fixed.
 2. D15/A-1 terminal is of output state when $BHE = V_{IH}$. $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

Package Dimensions

HN62428P Series (DP-42)

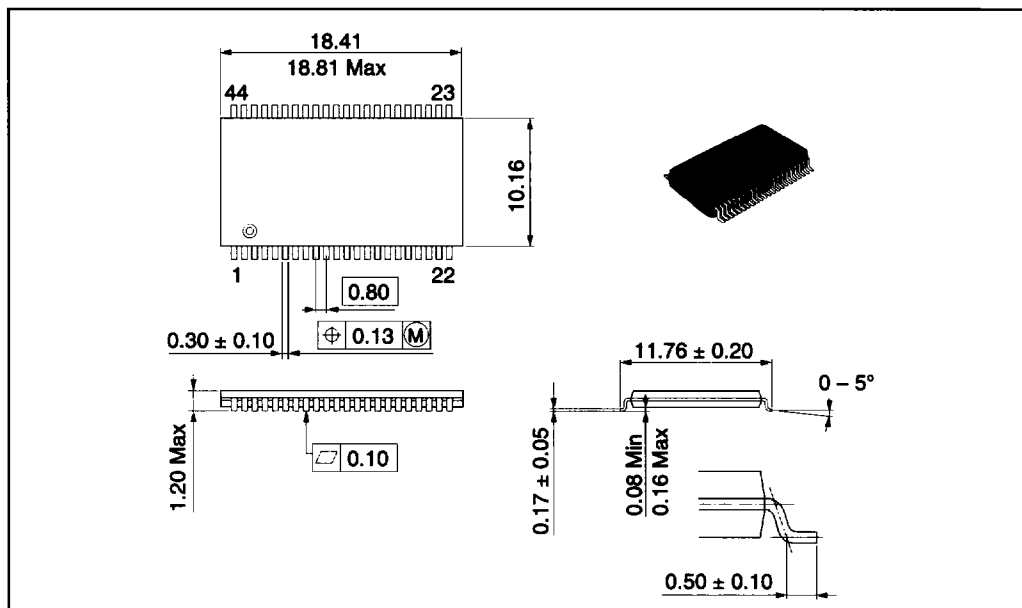
Unit : mm



Package Dimensions (cont)

HN62428TT Series (TTP-44D)

Unit : mm



HN62428FB Series (FP-44D)

Unit : mm

