

Low Power T1/E1 Integrated Short Haul Transceiver with Transmit Jitter Attenuation

Description

The 29C305A is a fully integrated transceiver for both North American 1.544 MHz (T1), and European 2.048 MHz (CEPT/E1) applications. Transmit pulse shapes (T1 or E1) are selectable for various line lengths and cable types.

The 29C305A provides transmit jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface. It is especially well suited for applications involving T1 and higher rates such as M13 mux, SONET, etc. This demultiplexing results in a "gapped" clock which the 305A smooths out.

The 29C305A is an advanced double-poly, double-metal CMOS device, requires only a single 5-volt power supply.

The MHS 29C305A finds applications in widely diverse areas of telecommunication, including :

- SONET Equipment
- M13 Multiplexers
- PCM / Voice Channel Banks
- Digital microwave Radio
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals.

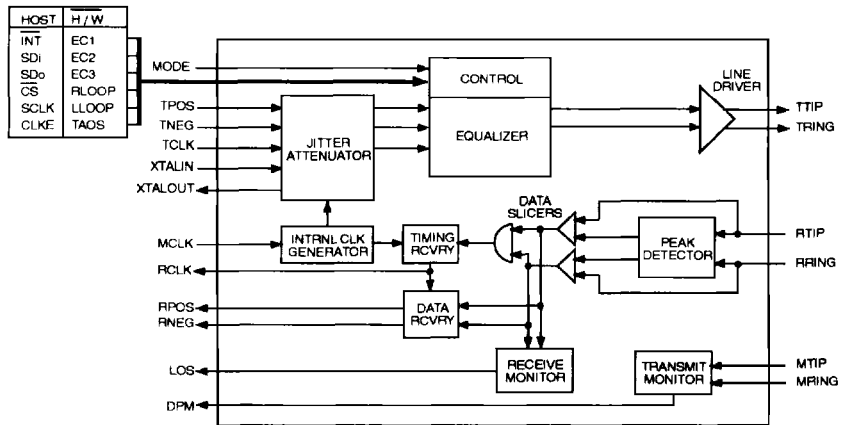
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Features

- Low power consumption (400 mW maximum) 40 % less than the 29C305
- Constant low output impedance transmitter, regardless of data pattern
- Compatible with most popular PCM framers including MHS 29C96
- Line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV
- Selectable slicer levels (T1/E1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 Ft
- Local and remote loopback functions
- Transmit driver performance monitor (DPM) output
- Receive monitor with loss of signal (LOS) output
- Receive jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Transmit jitter attenuation starting at 3 Hz
- Microprocessor controllable
- Available in 28 pin DIP and PLCC

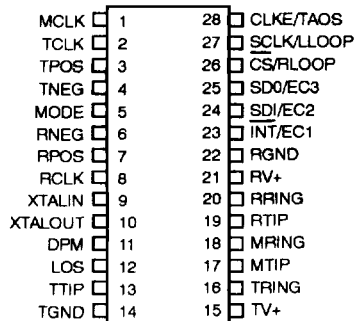
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Figure 1. 29C305A Block Diagram.

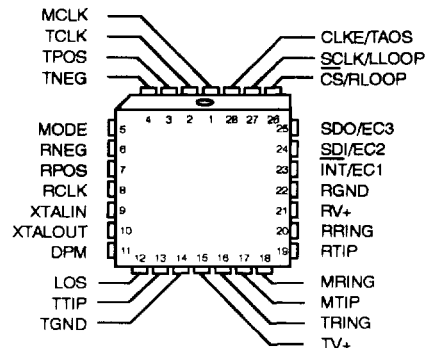


Interface

Pin Configuration



28 PIN DIP



28 PIN PLCC

Pin description

Symbol	Pin #	I/O	Name	Description
MCLK	1	I	Master Clock	A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
TCLK	2	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
TPOS	3	I	Transmit Positive Data	Input for positive pulse to be transmitted on the twisted-pair line.
TNEG	4	I	Transmit Negative Data	Input for negative pulse to be transmitted on the twisted-pair line.
MODE	5	I	Mode Select	Setting MODE to logic 1 puts the 29C305A in the Host mode. In the Host mode, the serial interface is used to control the 29C305 and determine its status. Setting MODE to logic 0 puts the 29C305A in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
RNEG	6	O	Receive Negative Data	Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge of RCLK.
RPOS	7	O	Receive Positive Data	
RCLK	8	O	Recovered Clock	This is the clock recovered from the signal received at RTIP and RRING.
XTALIN	9	I	Crystal Input	An external crystal operating at four times the bit rate (6.176 MHz for T1, 8.192 MHz for E1 applications) with an 18.7 pF load is required to enable the jitter attenuation function of the 29C305A. These pins may also used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
XTALOUT	10	O	Crystal Output	
DPM	11	O	Driver Performance Monitor	DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ± 2 clock periods. DPM remains at logic 1 until a signal is detected.
LOS	12	O	Loss Of Signal	LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when the receive signal input reaches 12.5 % marks density (4 marks in 32 bit periods) with no more than 15 consecutive zeros.
TTIP	13	O	Transmit Tip	Differential Driver Outputs. These low impedance outputs achieve maximum power savings through a 1:1.15 transformer (T1) or a 1:1 (75 Ω) or 1:1.26 (120 Ω) transformer (E1) without additional components. To provide higher return loss, resistors may be used in series with a transformer as specified in Tables 7, 8 and 9.
TRING	16	O	Transmit Ring	
TGND	14	-	Transmit Ground	Ground return for the transmit drivers power supply TV+.
	15	I	Transmit Power Supply	+5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ± 0.3 V.
MTIP	17	I	Monitor Tip	These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another 29C305A on the board. <i>Host mode only</i> : To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100 kHz to the TCLK frequency.
MRING	18	I	Monitor Ring	

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Pin description (continued)

Symbol	Pin #	I/O	Name	Description
RTIP	19	I	Receive Tip	The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
RRING	20	I	Receive Ring	
RV+	21	I	Receive Power Supply	+ 5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
RGND	22	-	Receive Ground	Ground return for power supply RV+.
INT	23	O	Interrupt (Host Mode)	This 29C305A Host mode output goes low to flag the host processor when LOS or DPM go active. INT is an open-drain output and should be tied to power supply RV+ through a resistor. INT is reset by clearing the respective register bit (LOS and/or DPM.)
EC1		I	Equalizer Control 1 (H/W Mode)	The signal applied at this pin in the 29C305A. Hardware mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
SDI	24	I	Serial Data In (Host Mode)	The serial data input stream is applied to this pin when the 29C305A operates in the Host mode. SDI is sampled on the rising edge of SCLK.
EC2		I	Equalizer Control 2 (H/W Mode)	The signal applied at this pin in the 29C305A. Hardware mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
SDO	25	O	Serial Data Out (Host Mode)	The serial data from the on-chip register is output on this pin in the 29C305A Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when CS is high.
EC3		I	Equalizer Control 3 (H/W Mode)	The signal applied at this pin in the 29C305A. Hardware mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
CS	26	I	Chip Select (Host Mode)	This input is used to access the serial interface in 29C305A Host mode. For each read or write operation, CS must transition from high to low, and remain low.
RLOOP		I	Remote Loopback (H/W Mode)	This input controls loopback functions in the 29C305A Hardware mode. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset.
SCLK	27	I	Serial Clock (Host Mode)	This clock is used in the 29C305A Host mode to write data to or read data from the serial interface registers.
LLOOP		I	Local Loopback (H/W Mode)	This input controls loopback functions in the 29C305A Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
CLKE	28	I	Clock Edge (Host Mode)	Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
TAOS		I	Transmit All Ones (H/W Mode)	When set to a logic 1, TAOS causes the 29C305A (Hardware mode) to transmit a continuous stream of marks at the TCLK frequency.

Functional Description

The 29C305A is a fully integrated PCM transceiver for both 1.544 MHz (T1) and 2.048 MHz (E1) applications which allows full-duplex transmission of digital data over existing twisted-pair installations.

Figure 1 is a simplified block diagram of the 29C305A. The 29C305A transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Transmitter

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 1. Refer to Table 2 and Figure 2 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The 29C305A also matches FCC and ECSA specifications for CSU applications. 2.048 MHz pulses can drive either coaxial or shielded twisted-pair lines using appropriate resistors in line with the output transformer.

Jitter Attenuation

Jitter attenuation of the 29C305A transmit outputs is provided by a Jitter Attenuation Loop (JAL) and an

Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 3 for crystal specifications. The ES is a 32 × 2-bit register. Transmit data is clocked into the ES with the transmit clock (TCLK) signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the transmit path.

Driver Performance Monitor

The transceiver incorporates a Driver Performance Monitor (DPM) connected in parallel with TTIP and TRING at the output transformer. The DPM output level goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

Line Code

The 29C305A transmits data as a 50 % AMI line code as shown in Figure 3. The output driver maintains a constant low output impedance of 3 Ω (typical) regardless of whether it is driving marks or spaces. This well controlled output impedance provides excellent return loss (> 20 dB) when used with external 9.4 Ω precision resistors (± 1 % accuracy) in series with a transmit transformer with a turns ratio of 1:2.3 (± 2 % accuracy). Series resistors also provide increased surge protection and reduced short circuit current flow.

Table 1: Equalizer Control Inputs.

EC3	EC2	EC1	Line Length ¹	Cable Loss ²	Application	Frequency
0	1	1	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB		
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		CEPT	2.048 MHz
0	1	0	FCC Part 68, Option A		CSU	1.544 MHz
0	1	1	ECSA TIC1.2			
Notes: 1. Line length from transceiver to DSX-1 cross-connect point. 2. Maximum cable loss at 772 kHz.						

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Table 2 : 29C305A Master Clock and Transmit Timing Characteristics (See Figure 2).

Symbol	Parameter		Min	Typ ¹	Max	Units
MCLK	Master clock frequency	T1	-	1.544	-	MHz
MCLK		E1	-	2.048	-	MHz
MCLKt	Master clock tolerance		-	± 100	-	ppm
MCLKd	Master clock duty cycle		40	-	60	%
fc	Crystal frequency	T1	-	6.176	-	MHz
fc		E1	-	8.192	-	MHz
TCLK	Transmit clock frequency	T1	-	1.544	-	MHz
TCLK		E1	-	2.048	-	MHz
TCLKt	Transmit clock tolerance		-	-	± 50	ppm
TCLKd	Transmit clock duty cycle		10	-	90	%
t _{SUT}	TPOS/TNEG to TCLK setup time		25	-	-	ns
t _{HT}	TCLK to TPOS/TNEG Hold time		25	-	-	ns

Note : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.

Figure 2. 29C305A Transmit Clock Timing Diagram.

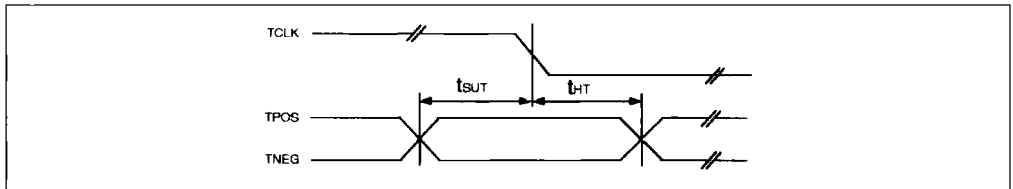
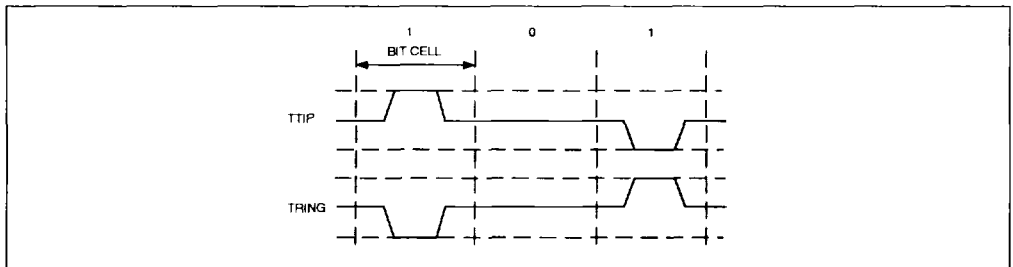


Figure 3. 50 % AMI Coding Diagram.



Receiver

The signal is received from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RPOS and RNEG, and the recovered is output at RCLK. Refer to Table 4 and Figure 4 for 29C305A receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For T1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000 or 001) the threshold is set to 70 % of the peak value. This threshold is maintained above 65 % for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000 or 001) the threshold is set to 50 %.

The receiver is capable of accurately recovering signals with up to -13.6 dB attenuation (from 2.4 V), corresponding to a received signal level of

approximately 500 mV. Maximum cable length is 1500 feet of ABAM cable (approximately 6 dB). Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and the receive monitor. The data and clock recovery circuits are highly tolerant, with an input jitter tolerance significantly better than required by Pub 62411, as shown in Figure 5. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and the RCLK output is replaced with the MCLK. Received marks are output regardless of the LOS status, but the LOS pin will not reset until the ones density reaches 12.5 %. This level is based on receipt of at least 4 ones in any 32 bit periods with no more than 15 consecutive zeros.

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Table 3 : 29C305A Crystal Specifications (External).

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	± 20 ppm @ 25 °C ± 25 ppm from - 40 °C to 85 °C (Ref 25 °C reading)	± 20 ppm @ 25 °C ± 25 ppm from - 40 °C to 85 °C (Ref 25 °C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C ₀ = 7 pF maximum C _M = 17 fF typical	HC49 (R3W), C ₀ = 7 pF maximum C _M = 17 fF typical

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Table 4 : 29C305A Receive Timing Characteristics (See Figure 4).

Symbol	Parameter		Min	Typ ¹	Max	Units
RCLKd	Receive clock duty cycle ²	T1	40	50	60	%
RCLKd		E1	40	50	60	%
tpw	Receive clock pulse width ²	T1	594	648	702	ns
tpw		E1	447	488	529	ns
tpWH	Receive clock pulse width high	T1	-	324	-	ns
tpWH		E1	-	244	-	ns
tpWL	Receive clock pulse width low	T1	270	324	378	ns
tpWL		E1	203	244	285	ns
tsUR	RPOS / RNEG to RCLK rising setup time	T1	50	270	-	ns
tsUR		E1	50	203	-	ns
thR	RCLK rising to RPOS / RNEG hold time	T1	50	270	-	ns
thR		E1	50	203	-	ns

Notes :

1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz, 0.2 UI clock displacement for 2.048 MHz.)

Figure 4. 29C305A Receive Clock Timing Diagram.

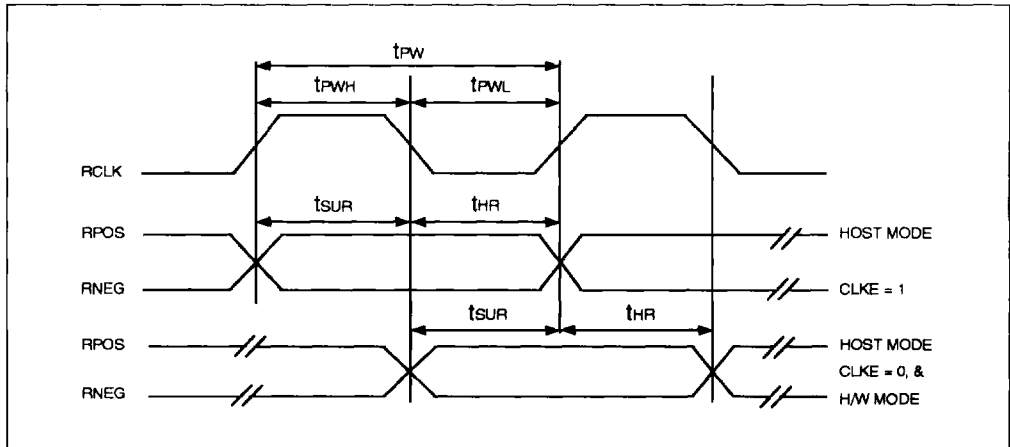
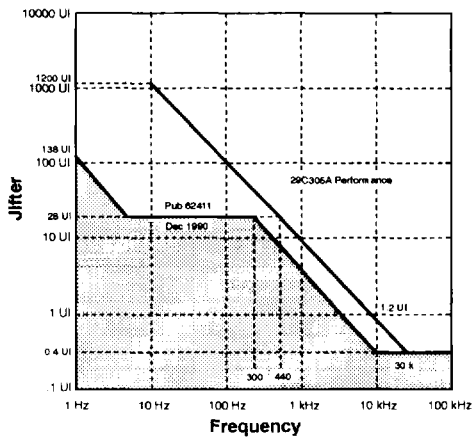


Figure 5. 29C305A Receive Jitter Tolerance.



Operating Modes

The 29C305A transceiver can be controlled by a microprocessor through the serial interface (Host mode), or through hard-wired pins (Hardware mode).

The mode of operation is set by the MODE pin logic level. The transceivers can also be commanded to operate in one of several diagnostic modes.

Host Mode Operation

To allow a host microprocessor to access and control the 29C305A through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/ Address byte and an 8-bit Data byte.

The Host mode provides a latched Interrupt output ($\overline{\text{INT}}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are

valid, relative to the Serial Clock (SCLK) or RCLK as follows :

CLKE	OUTPUT	CLOCK	VALID EDGE
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The 29C305A serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The 29C305A contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select ($\overline{\text{CS}}$) input to transition from high to low. Bit 1 of the Serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 5 lists serial data output bit combinations for each status. Serial data structure is shown in Figure 6 and I/O timing characteristics are shown in Table 6, and Figures 7 and 8.

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Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{\text{INT}}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK.

To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon

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crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. MCLK provides the receiver reference. The crystal oscillator provides the transmitter reference. If the 29C305A crystal oscillator is grounded, MCLK is used as the transmitter reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and centers the oscillator, then calibration begins.

Table 5 : 29C305A Serial Data Outputs Bits (See Figure 6).

Bit D5	Bit D6	Bit D7	STATUS
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

Figure 6. 29C305A Serial Interface data Structure.

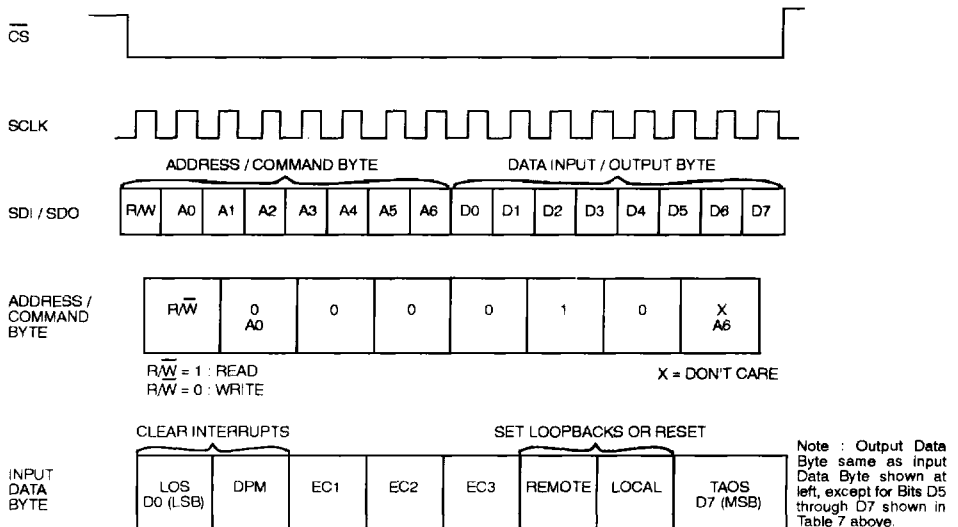


Table 6 : 29C305A Serial I/O Timing Characteristics (See Figures 7 and 8).

Symbol	Parameter	Test Conditions	Min	Typ ¹	Max	Units
t_{RF}	Rise/Fall time – any digital output	Load 1.6 mA, 50 pF	–	–	100	ns
t_{DC}	SDI to SCLK setup time		50	–	–	ns
t_{CDH}	SCLK to SDI hold time		50	–	–	ns
t_{CL}	SCLK low time		240	–	–	ns
t_{CH}	SCLK high time		240	–	–	ns
t_r, t_f	SCLK rise and fall time		–	–	50	ns
t_{CC}	CS to SCLK setup time		50	–	–	ns
t_{CCH}	SCLK to CS hold time		50	–	–	ns
t_{CWH}	CS inactive time		250	–	–	ns
t_{CDV}	SCLK to SDO valid		–	–	200	ns
t_{CDZ}	SCLK falling edge or CS rising edge to SDO high Z		–	100	–	ns

Note : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.

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Figure 7. 29C305A Serial Data Input Timing Diagram.

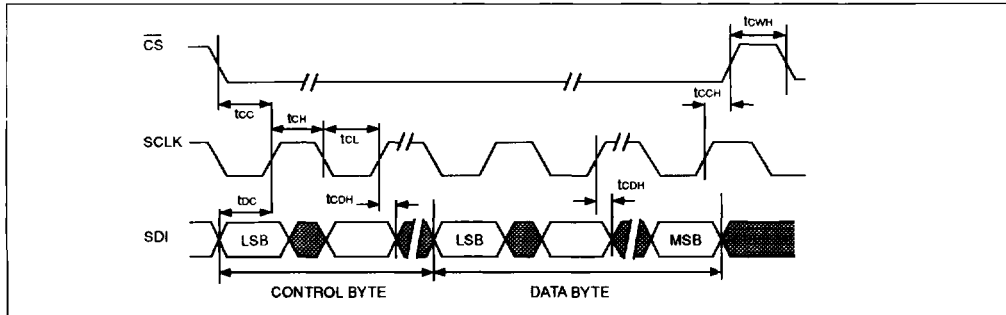
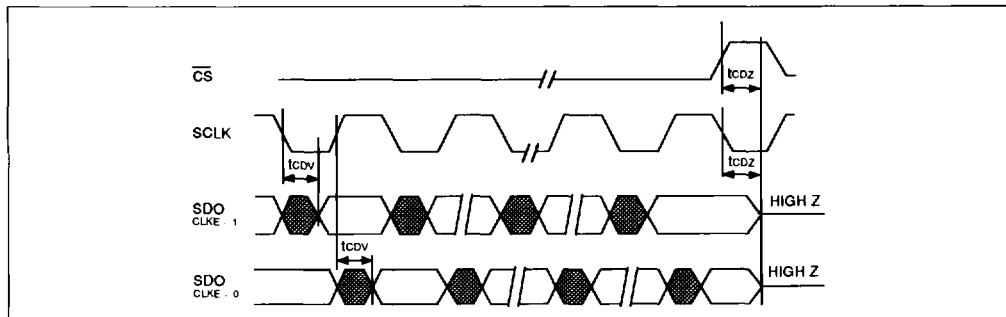


Figure 8. 29C305A Serial Data Output Timing Diagram.



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Diagnostic Mode Operation

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback. During TAOS, the transmitter is locked to MCLK. If MCLK is not supplied, the transmitter powers down.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmits circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS,

RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs will be transmitted normally. (A stream of 1's will be transmitted if the TAOS command is active.) During local Loopback if TCLK is not supplied, the transmitter powers down.

Power Requirements

The 29C305A is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± 3 V of each other, and decoupled to their respective grounds separately, as shown in Figure 9. Isolation between the transmit and receive circuits is provided internally. The transmitter powers down to conserve power when the required clock input is not supplied. The 29C305A enters the power down mode during normal operation and local loopback if TCLK is not supplied, and during TAOS if MCLK is not supplied.

Applications

1.544 MHz DSX-1 Interface Applications

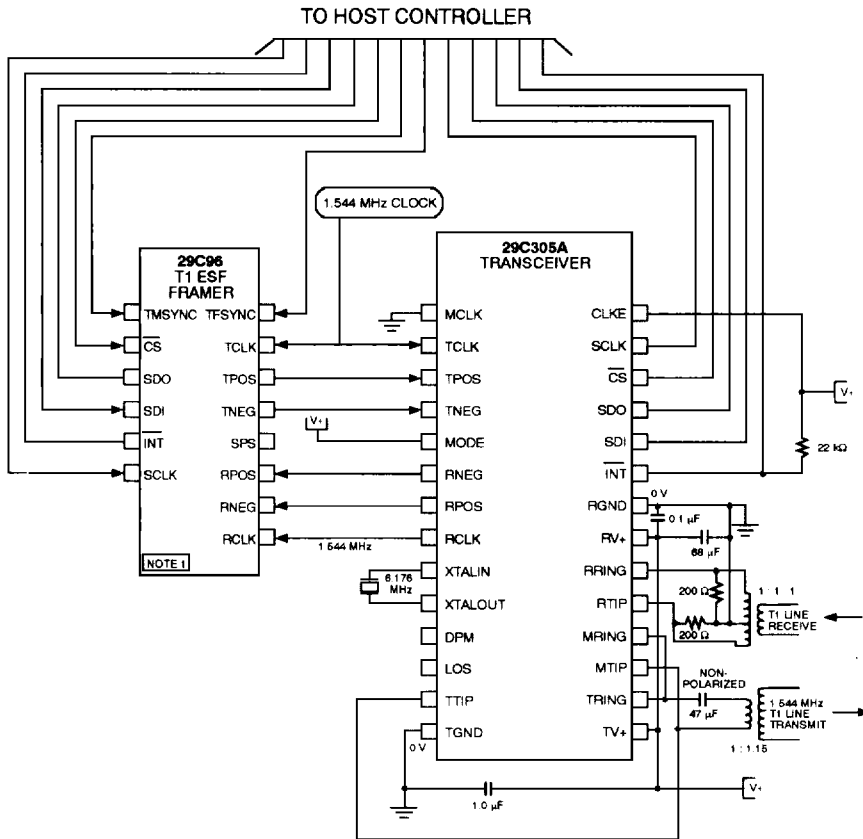
Figure 9 is a typical 1.544 MHz T1 interface application using a 1:1.15 transmit transformer without in-line resistors for maximum power savings. The 29C305A is shown in Host mode with the 29C96 T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface.

Table 7: T1/DSX-1 Output Combinations (100 Ω).

EC	Xfmr Ratio ¹	Rt Value ²	Rtn Loss ³
011 - 111	1 : 1.15	Rt = 0 Ω	0.5 dB
011 - 111	1 : 2	Rt = 9.4 Ω	20 dB
011 - 111	1 : 2.3	Rt = 9.4 Ω	28 dB

- Notes :
1. Transformer turns ration accuracy is ± 2 %
 2. Rt value are ± 1 %
 3. Typical return loss, 102 kHz - 2.048 MHz band.

Figure 9. Typical 29C305A 1.544 MHz T1 Application (Host Mode).



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Notes : 1. In addition to the 29C96, the 29C305A is compatible with a wide variety of digital framing and signaling devices.

The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68 µF and 0.1 µF on the receive side.)

For DSX-1 applications, series resistors can be used in line with the transmit transformer to provide higher return loss. Table 7 lists transformer ratios, Rt values and typical return loss values for 1.544 MHz EC codes.

2.048 MHz E1 Interface Applications

Figure 10 is a typical 2.048 MHz E1 application. The 29C305A is shown in Hardware mode with the 29C96 E1/CRC4 Framer. As in the DSX-1 application Figure 9, this configuration is illustrated with a crystal in place to enable the 29C305A Jitter Attenuation Loop, and a single power supply bus. The hard-wired

control lines for TAOS, LOOP and RLOOP are individually controllable, and the LOOP and RLOOP lines are also tied to a single control for the Reset function. EC3 and EC2 are hardwired to ground, but the EC1 pin is switchable high or low selecting codes 000 and 001. With the 1 : 1 transformer ratio and code 000 selected on the EC inputs, the 29C305A outputs the CCITT specified 2.37 V pulse onto 75 Ω coaxial cable. Simple changing the EC code to 001 allows the 29C305A to match the 3.0V pulse specification for 120 Ω shielded twisted-pair cable. No transformer change is required. For situations where a 1:1.26 transformer is desired, EC code 000 selects the correct output for 120 Ω twisted-pair cable.

To achieve higher return loss, increased surge protection and lower output short circuit current,

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series resistors can be used in line with the transmit transformer. Tables 8 and 9 list transformer ratios, series resistor (Rt) and typical return loss values with

associated 2.048 MHz EC codes for 75 Ω coax and 120 Ω TWP, respectively.

Table 8 : E1/CEPT Output Combinations (75 Ω).

EC	Xfmr Ratio ¹	Rt Value ²	Rtn Loss ³
001	1 : 1	Rt = 10 Ω	5 dB
001	1 : 2	Rt = 14.3 Ω	12 dB
000	1 : 1	Rt = 0 Ω	0.5 dB
000	1 : 2	Rt = 9.4 Ω	24 dB

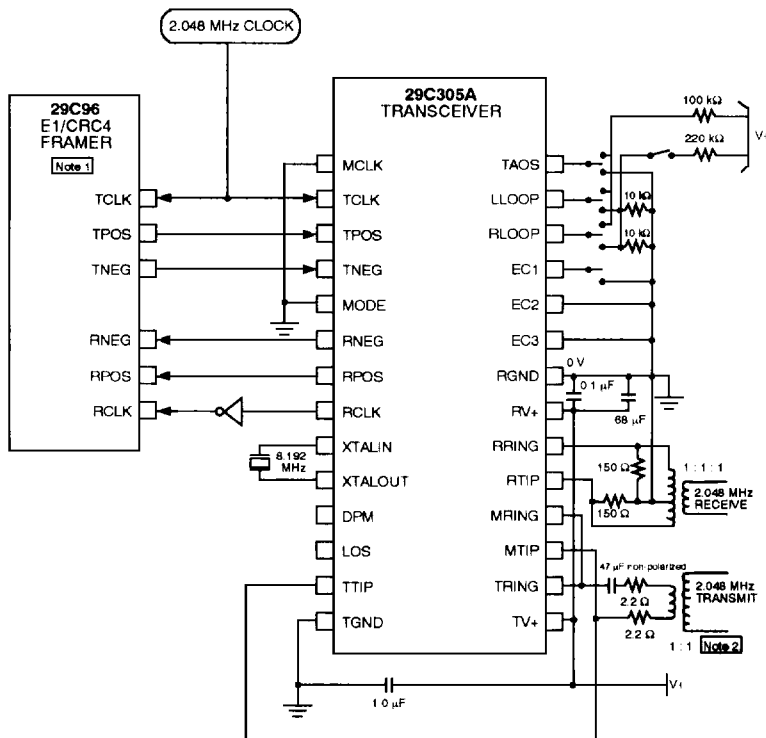
Notes : 1. Transformer turns ration accuracy is ±2 %
 2. Rt value are ± 1 %
 3. Typical return loss, 102 kHz – 2.048 MHz band.

Table 9 : E1/CEPT Output Combinations (120 Ω).

EC	Xfmr Ratio ¹	Rt Value ²	Rtn Loss ³
001	1 : 1	Rt = 0 Ω	0.5 dB
001	1 : 2	Rt = 15 Ω	30 dB
000	1 : 1.26	Rt = 0 Ω	0.5 dB
000	1 : 2	Rt = 8.7 Ω	12 dB

Notes : 1. Transformer turns ration accuracy is ±2 %
 2. Rt value are ± 1 %
 3. Typical return loss, 102 kHz – 2.048 MHz band.

Figure 10. Typical 29C305A 2.048 MHz Application (Hardware Mode).



Notes : 1. In addition to the 29C96, the 29C305 is compatible with a wide variety of framing and signaling devices.
 2. For 75 Ω coaxial cable, use a 1:1 transformer ratio and EC code 000.
 For 120 Ω twisted pair cable use either a 1:1 transformer with EC code 001, or a 1:1.26 transformer with code 000.

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
RV+, TV+	DC supply (referenced to GND)	-	6.0	V
V _{IN}	Input voltage, any pin ¹	RGND - 0.3	RV+ + 0.3	V
I _{IN}	Input current, any pin ²	- 10	10	mA
T _A	Ambient operating temperature	- 40	85	°C
T _{STG}	Storage temperature	- 65	150	°C

WARNING : Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed at these extremes.

- Notes :**
1. Excluding RTIP and RRING which must stay within -6 V to RV + 0.3 V.
 2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

2

Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
RV+, TV+	DC supply ³		4.75	5.0	5.25	V
T _A	Ambient operating temperature		- 40	25	85	°C
P _D	Total Power Dissipation	100 % ones density & maximum line length @ 5.25 V	-	400	-	mW

- Notes :**
3. TV+ must not exceed RV+ by more than 0.3 V.
 4. Power dissipation while driving 75 Ω load over operating range. Includes device and load. Digital input levels are within 10 % of the supply rails and digital outputs are driving a 50 pF capacitive load.

Digital Characteristics (T_A = -40° to 85° C, V+ = 5.0 V ± 5 %, GND = 0 V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V _{IH}	High level input voltage ^{5, 6} (pins 1-5, 10, 23-28)		2.0	-	-	V
V _{IL}	Low level input voltage ^{5, 6} (pins 1-5, 10, 23-28)		-	-	0.8	V
V _{OH}	High level output voltage ^{5, 6} (pins 6-8, 11, 12, 23, 25)	I _{OUT} = - 400 μA	2.4	-	-	V
V _{OL}	Low level output voltage ^{5, 6} (pins 6-8, 11, 12, 23, 25)	I _{OUT} = 1.6 mA	-	-	0.4	V
I _{LL}	Input leakage current ⁷		- 10	-	+ 10	μA
I _{3L}	Three-state leakage current ⁵ (pin 25)		- 10	-	+ 10	μA

- Notes :**
5. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
 6. Output drivers will output CMOS logic levels into CMOS loads.
 7. Except MTIP and MRING I_{LL} = ± 50 μA.

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Analog Specifications ($T_A = -40^\circ$ to 85°C , $V_+ = 5.0\text{ V} \pm 5\%$, $\text{GND} = 0\text{ V}$)

Parameter		Test Conditions	Min	Typ	Max	Units	
AMI Output Pulse Amplitudes	T1	measured at the DSX	2.4	3.0	3.6	V	
	E1	measured at line side	2.7	3.0	3.3	V	
Recommended Output Load at TTIP and TRING			-	75	-	Ω	
Jitter added by the transmitter ⁸	10 Hz - 8 kHz		-	-	0.01	UI	
	8 kHz - 40 kHz		-	-	0.025	UI	
	10 Hz - 40 kHz		-	-	0.025	UI	
	Broad Band		-	-	0.05	UI	
Sensitivity below DSX (0dB = 2.4 V)			13.6	-	-	dB	
			500	-	-	mV	
Loss of Signal threshold			-	0.3	-	V	
Data decision threshold	T1		-	65	-	% peak	
	E1		-	50	-	% peak	
Allowable consecutive zeros before LOS			160	175	190	-	
Input jitter tolerance 10 kHz - 100 kHz			0.4	-	-	UI	
Jitter attenuation curve corner frequency ⁹			-	3	-	hz	
Minimum return Loss ^{10, 11}		Transmit		Receive			
			Min	Typ	Min	Type	
		51 kHz - 102 kHz	20	28	20	30	dB
		102 kHz - 2.048 MHz	20	28	20	30	dB
	2.048 MHz - 3.072 MHz	20	24	20	25	dB	

- Notes : 8. Input signal to TCLC is jitter-free.
 9. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
 10. In accordance with CCITT G.703/RC6367A return loss specifications (CEPT), when wired as shown in Figure 9.
 11. Guaranteed by design.

Ordering Information

I	S	29C30X	A
Temperature Range blank : Commercial I : Industrial	Package S = PLCC P = PDIL	Part Number 29C300 29C301 29C304 29C305 29C310 29C318	A = Low Power

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