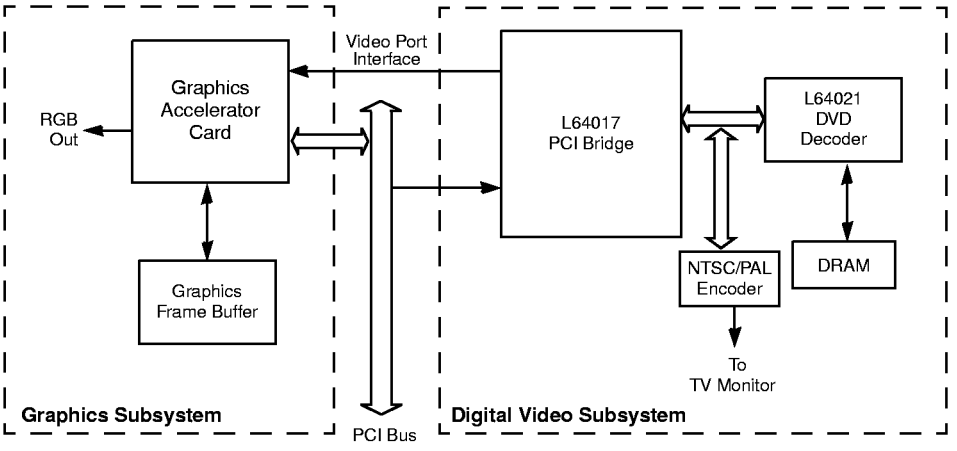
L64017 PCI Bridge Chip

Advance Datasheet

The L64017 PCI Bridge is a companion chip of LSI Logic's L64021 Digital Video Decoder (DVD). The L64017 provides a fully integrated, low-cost video interface between a PCI bus and the L64021. This interface includes video color control. The bridge chip is ideally suited for multimedia DVD/MPEG-2 playback applications on PCI systems.

Figure 1 illustrates the L64017 in a typical system.

Figure 1 Typical System Block Diagram



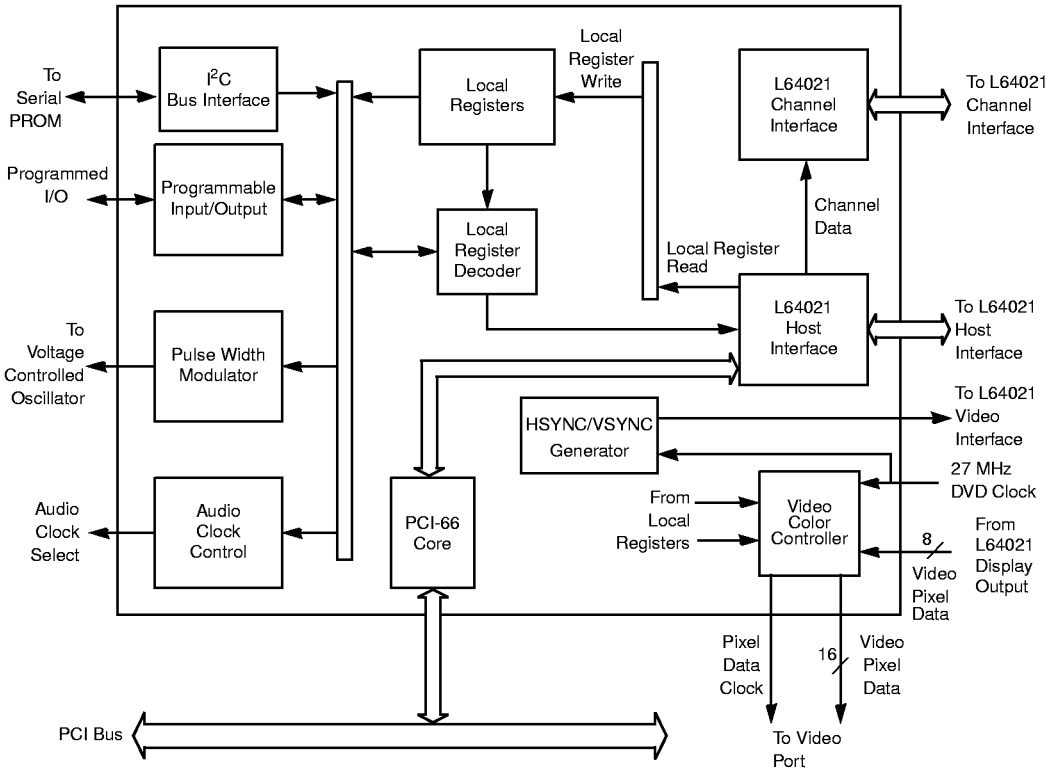
Features and Benefits

- Programmable Built-in Video Color Control
- Full PCI bus interface support (PCI 2.1 specification)
- Glueless Video Port Interface to LPB, VMI 1.4, AMC 2.0, VIP 1.1, and ZV (Zoomed Video)
- PC98 Compliant
- 0.35-µ G10® technology with 3.3 V operation
- 208-pin Plastic Quad Flat Pack (PQFP) package
- Supports various displays with gamma correction of CRTs
- Provides seamless video data transfer between graphics subsystem and digital video solution without sacrificing PC bus bandwidth
- Supports popular 8-bit and 16-bit video port interfaces
- Supports the latest technologies
- Provides high performance and low-power consumption
- Available in cost-effective package

Functional Description

The L64017 provides complete control of the L64021 DVD Decoder from the PCI bus. Figure 2 provides a block diagram of the L64017. Short descriptions of the functional blocks are given following the figure. Refer to the *L64017 PCI Bridge Technical Manual* for detailed information.

Figure 2 L64017 Functional Block Diagram



PCI Interface

The L64017 PCI Interface complies with the PCI 2.1 specification. The L64017 implements the Master-Slave PCI core. This PCI target interface uses a type 0 configuration space header to perform the PCI configuration process.

L64021 Host Interface

The L64021 Host Interface provides a seamless interface to the L64021 registers.

L64021 Channel Interface

The L64021 Channel Interface uses the L64017's PCI master capabilities to control the delivery of channel data from the PCI bus to the L64021.

HSYNC/VSYNC Generator

The HSYNC/VSYNC generator provides the horizontal and vertical synchronization pulses to the L64021 video interface.

Video Color Controller

The Video Color Controller (VCC) detects chroma values from the incoming video stream, processes the values according to the programmed settings of the L64017's internal registers, and reinserts the new chroma values in the outgoing video data stream.

Local Registers and Decoder

The local registers reside in the L64017 and provide control over a variety of hardware functions.

Programmable I/O Interface

The programmable input/output interface provides seven programmable I/O control hardware functions.

Pulse Width Modulator

The system uses an external voltage-controlled (VCX) oscillator to generate a nominal 27-MHz video clock. To eliminate variance and drift, the Pulse Width Modulator (PWM) outputs a variable voltage signal to control the VCX oscillator.

Audio Clock Control

The L64017 can control an external programmable clock generator to select the appropriate audio clock frequency.

I^2C Bus Interface

The L64017 uses the I^2C two-wire interface to read four bytes of data from a Serial PROM.

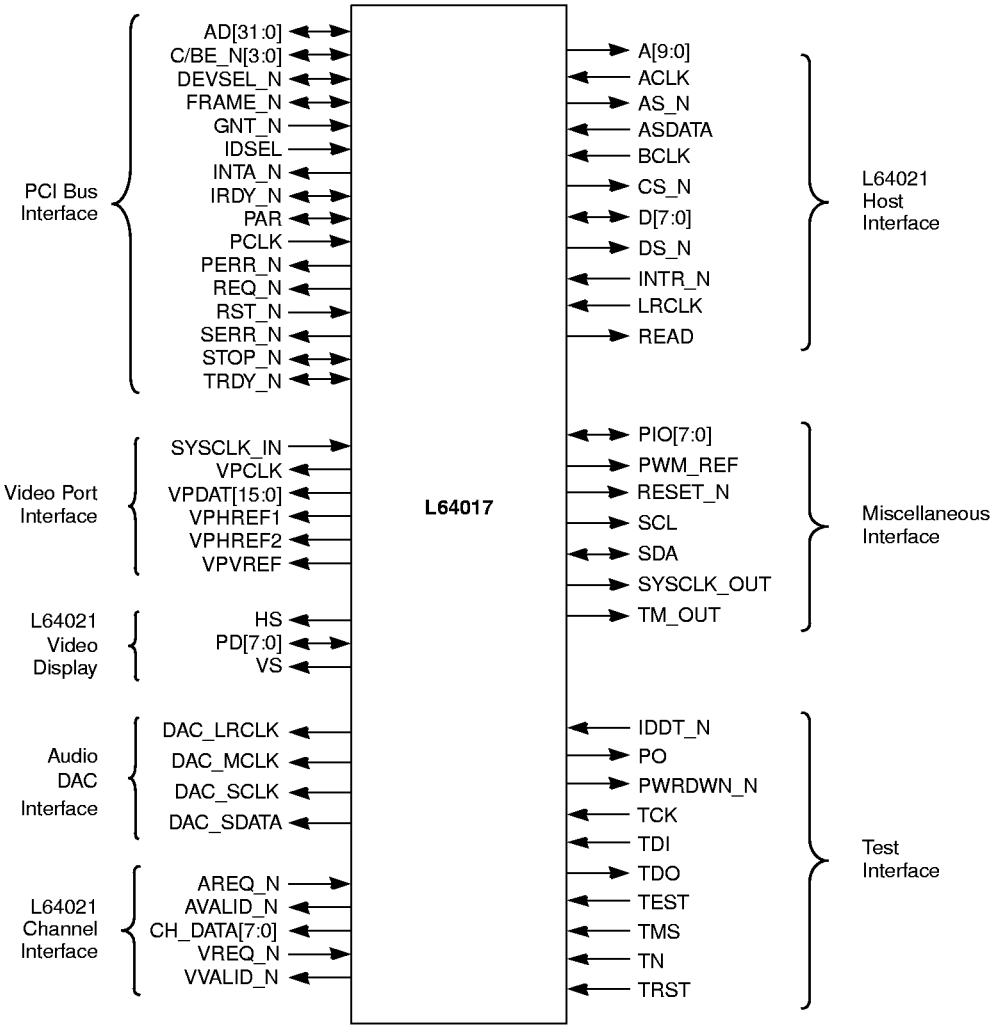
Video Port Interface

The L64017 interfaces to video ports that are supported by the most popular VGA chips: S3 LPB bus, ATI AMC 2.0 bus, VMI 1.4 bus (video port only), and VIP 1.1 bus (video port only).

Signal Descriptions

This section describes the external signals of the L64017. The descriptions are categorized according to the interface. Active-LOW signals have "_N" appended to the end of their names.

Figure 3 L64017 Logic Symbol



PCI Bus Interface

AD[31:0] **Multiplexed Address and Data Bus** **3-state I/O**

The PCI 32-bit address and 32-bit data are multiplexed on AD[31:0]. The address phase is the clock cycle in which FRAME_N is asserted. During the address phase, AD[31:0] contains a physical memory address.

The least-significant byte (LSB) of the 32-bit data word is transferred on AD[7:0], and the most significant byte (MSB) is transferred on AD[31:24]. Write data is stable when IRDY_N is asserted, and read data is stable when TRDY_N is asserted.

C/BE_N[3:0] **Bus Command and Byte Enables** **3-state I/O**

The PCI Bus commands and data byte enables are multiplexed on C/BE_N[3:0]. During the address phase (FRAME_N is asserted), C/BE_N[3:0] contains the bus command.

During the data phase, C/BE_N[3:0] contains the byte enables. C/BE_N0 enables data writes on AD[7:0], which is the LSB. C/BE_N3 enables data writes on AD[31:24], which is the MSB.

DEVSEL_N **PCI Device Select** **3-state I/O**

The target, whose address was specified in the address phase of the current transfer, asserts DEVSEL_N.

FRAME_N **PCI Cycle Frame** **3-state I/O**

The current master asserts FRAME_N to indicate the beginning and duration of an access. FRAME_N is asserted to indicate the start of a bus transaction. Bus transfers continue while FRAME_N is asserted, and they terminate when FRAME_N is deasserted.

GNT_N **PCI Bus Grant** **3-state I**

This input is asserted in response to the L64017 asserting REQ_N to indicate the L64017 has permission to use the PCI bus.

IDSEL **PCI Initialization Device Select** **I**

IDSEL is a chip select that is input to the L64017 chip during configuration read and configuration write cycles.

INTA_N **PCI Interrupt A** **Open Drain O**
Assertion of this output indicates a PCI interrupt occurred.

IRDY_N **PCI Initiator Ready** **3-state I/O**
The initiator, which is the current bus master, asserts IRDY_N to indicate when there is valid data on AD[31:0] during a write cycle, or that it is ready to accept data from AD[31:0] during a read cycle. A data phase (transfer) is completed on any clock cycle where both IRDY_N and TRDY_N are asserted. Wait cycles are inserted until both IRDY_N and TRDY_N are asserted.

PAR **Parity** **3-state I/O**
PAR is set or reset to create even parity for the 36 bits comprised of AD[31:0] and C/BE_N[3:0]. Even parity means that the total number of ones (bits set to a high state) on PC_AD[31:0], C/BE_N[3:0], and PAR is even.

PCLK **PCI Bus Clock** **I**
PCLK is the 33-MHz clock that provides timing for all transactions on the PCI bus. All PCI input signals, except RST_N, are sampled on the rising edge of the PCLK.

PERR_N **Parity Error** **O**
Assertion of PERR_N indicates one or more data parity errors have occurred.

REQ_N **PCI Bus Request** **3-state O**
The L64017 asserts REQ_N to request a master transfer on the bus.

RST_N **PCI Bus Reset** **I**
RST_N is an asynchronous signal that resets PCI-specific registers, state machines, and signals to an initial state. All PCI Interface signals are held 3-stated when RST_N is asserted.

SERR_N **System Error** **O**
The L64017 asserts SERR_N when a parity error is detected on AD[31:0] and C/BE_N[3:0] during the address phase of a transfer.

STOP_N **PCI Stop** **3-state I/O**
The target asserts STOP_N to stop the current data transfer. As a master, the L64017 terminates the data transfer when STOP_N is asserted.

TRDY_N **PCI Target Ready** **3-state I/O**
The target, which is the current bus slave, asserts TRDY_N to indicate when there is valid data on AD[31:0] during a read cycle, or when it is ready to accept data from AD[31:0] during a write cycle. The data phase of a transfer completes on any clock cycle when both IRDY_N and TRDY_N are asserted.

L64021 Channel Interface

AREQ_N **Audio Transfer Request** **I**
The L64021 asserts this signal LOW to indicate that the L64021 is ready to receive a new byte of coded audio data. The maximum transfer rate over this interface is 40 Mbits/s.

AVALID_N **Audio Data Valid** **O**
On the rising edge of AVALID_N, the next byte of audio data or program stream data that is present on the CH_DATA[7:0] pins is written to the L64021. The L64017 relays the data to the L64021 by immediately asserting the AVALID_N signal LOW.

CH_DATA[7:0] **Channel Data Bus** **O**
CH_DATA[7:0] is an output bus that serves as a parallel output path for channel data.

VREQ_N **Video Transfer Request** **I**
The L64021 asserts VREQ_N LOW when it is ready to receive a new byte of coded video data. The maximum transfer rate over this interface is 20 Mbits/s.

Note: In a DVD system, VREQ_N and VVALID_N are not used.

VVALID_N **Video Data Valid** **O**
On the rising edge of VVALID_N, the next byte of video data that is present on the CH_DATA[7:0] data bus is written to the L64021. VVALID_N is not used in the system or program stream modes.

L64021 Host Interface

A[9:0] **Address Bus** **O**
This 10-bit address line provides access to the L64021's internal registers. In the L64021, the address value on these lines is latched on the falling edge of AS_N (Motorola).

ACLK **Audio Master Clock** **I**
ACLK is an audio clock from the L64021 DVD Decoder.

AS_N **Address Strobe** **O**
This signal latches (in the L64021) the address currently on the A[8:0] bus. The address latches on the falling edge of the AS_N signal. A LOW on both CS_N and AS_N indicates the start of a bus transaction. The actual transaction type (either read or write) is determined by the READ polarity. The end of a bus cycle is determined by the rising edge of AS_N.

ASDATA **Decoder Audio Serial Data** **I**
ASDATA receives serial, digital audio data from the L64021's audio decoder.

BCLK **Decoder Audio Bit Serial Clock** **I**
The L64017 uses this input to clock in the serial audio data from the L64021 DVD Decoder.

CS_N **Chip Select** **O**
Assertion of this active-LOW signal indicates an attempt by an external host CPU to access the L64021 either for a read or a write bus cycle. A LOW on both CS_N and AS_N indicates the start of a bus transaction. The actual transaction type (either read or write) is determined by the READ polarity. The end of a bus cycle is determined by the rising edge of AS_N. CS_N may stay active LOW for more than one bus transaction cycle.

D[7:0] **Host Data Bus** **I/O**
D[7:0] is an eight-bit bidirectional data bus used for data communication between the host CPU and the L64021. During a read bus cycle, D[7:0] carries valid information from an internal L64021 register. The L64021's DTACK signal determines when the data on the host data bus is valid. The rising edge of DS_N (Motorola mode) indicates to the L64021 when to strobe the data into the chip.

DS_N	**Data Strobe** Assertion of DS_N indicates when the CPU strobes the data in or out of the L64021. During a read bus cycle, the start of a read transaction is triggered when DS_N, CS_N, and AS_N are all LOW. During a write bus cycle, the rising edge of DS_N indicates when the L64021 latches the data present on D[7:0].	**O**
INTR_N	**Interrupt** The L64021's host interface drives this signal LOW to send an interrupt to the Host CPU.	**I**
LRCLK	**Decoder Audio Left/Right Clock** Using the default setting, LRCLK is driven HIGH when the ASDATA pin has a right channel sample, and LRCLK is driven LOW when the ASDATA pin has a left channel sample.	**I**
READ	**Read/Write Strobe** READ indicates whether the current bus cycle is a read or write. When READ is HIGH, a read bus cycle is in progress. When READ is LOW, a write bus cycle is in progress. CS_N must be LOW for the CPU to access the L64021.	**O**

L64021 Video Display Interface

HS	**Horizontal Sync** HS is the horizontal sync output. The horizontal sync signal is synchronous to SYSCLK. Its pulse is controlled by registers 0x284 to 0x287.	**O**
PD[7:0]	**Pixel Data Output Bus** The data on the PD[7:0] bus is the pixel data of the reconstructed picture from the L64021. The pixel data is formatted in CCIR601 (Y, Cb, Cr) chromaticity.	**I**
VS	**Vertical Sync / Odd-Even Field** VS is a conventional Vertical Sync output. VS changes state at the beginning of each field. The parity of the field is controlled by the timing of VS relative to HS. Its pulse is controlled by registers 0x288 to 0x28B.	**O**

Audio DAC Interface

DAC_LRCLK **Audio DAC Left/Right Clock** **O**
This output enables the left or right serial data output.

DAC_LRCLK	Description
0	Left Channel Enabled
1	Right Channel Enabled

DAC_MCLK **Audio DAC Master Clock** **O**
DAC_MCLK is the digital audio master clock. Its frequency is programmable.

DAC_SCLK **Audio DAC Serial Clock** **O**
DAC_SCLK is the serial audio digital PCM clock. Its frequency is programmable.

DAC_SDATA **Audio DAC Serial Data** **O**
This signal is the digital PCM signal that carries audio information. DAC_SDATA uses the I^2S format.

Video Port Interface

SYSCLK_IN **System Clock In** **I**
SYSCLK_IN is the 27-MHz system clock.

VPCLK **Video Port Clock** **O**
VPCLK is the 27-MHz video port clock.

VPDAT[15:0] **Video Data** **O**
VPDAT[15:0] is a 16-bit pixel data bus used for transferring ITU R-656 YCbCr video data from the L64017's video controller to the Video Port.

VPHREF1 **Video Port Horizontal Reference Signal 1** **O**
VPHREF1 is a horizontal reference signal for the video port.

VPHREF2 **Video Port Horizontal Reference Signal 2** **O**
VPHREF2 is a horizontal reference signal for the video port.

VPVREF **Video Port Vertical Reference Signal** **O**
VPVREF is a vertical reference signal for the video port.

Test Interface

IDDT_N	**Test Pin** This signal is an LSI Logic test pin. Leave it unconnected for normal operation.	**I**
PO	**Test Pin** This signal is an LSI Logic test pin. Leave it unconnected for normal operation.	**O**
PWRDWN_N	**Power Down** This output is used to turn off the oscillator.	**O**
TCK	**Test Clock** TCK shifts the contents of the boundary scan register.	**I**
TDI	**Test Data Input** TDI contains test data. It is sampled on the rising edge of TCK.	**I**
TDO	**Test Data Output** TDO outputs the boundary scan register's data.	**O**
TEST	**Test Enable** Assertion of TEST enables test mode.	**I**
TMS	**Test Mode Signal** TMS is the shift enable to the boundary scan register.	**I**
TN	**Test Pin** This signal is an LSI Logic test pin. Leave it unconnected for normal operation.	**I**
TRST	**Test Reset** When asserted, TRST resets the Boundary Scan Test Access Port controller.	**I**

Miscellaneous Interface

PIO[7:0]	**Programmable Input/Output** These user-defined signals are available for control or status functions for the L64017 hardware.	**I/O**
PWM_REF	**Pulse Width Modulation Reference** This signal provides a reference signal for tuning the VCX oscillator.	**O**

RESET_N	**Reset** This active-LOW reset signal resets the L64021.	**O**
SCL	**I²C Controller Clock** This signal clocks all data on SDA into and out of a Serial PROM.	**O**
SDA	**Serial Data** This bidirectional pin transfers data into and out of a Serial PROM.	**I/O**
SYSCLK_OUT	**System Clock Out** This clock is the 27-MHz system output clock.	**O**
TM_OUT	**L64021 Power Management Signal** This pin connects to the TM0 and TM1 pins of the L64021. During normal operation, this pin is LOW. In power-saving mode, this pin is HIGH.	**O**

Electrical Requirements

This section specifies the electrical requirements for the L64017. Four tables list electrical data in the following categories:

- Absolute Maximum Ratings (Table 1)
- Recommended Operating Conditions (Table 2)
- Capacitance (Table 3)
- DC Characteristics (Table 4)

Table 1 Absolute Maximum Ratings

Symbol	Parameter	Limits[1]	Unit
V_{DD}	DC Supply	-0.3 to +3.9	V
V_{IN}	5 V Compatible Input Voltage	-1.0 to 6.5	V
I_{IN}	DC Input Current	±10	µA
T_{STG}	Storage Temperature Range, Plastic	-40 to +125	°C

1. Referenced to V_{SS}.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
V_{DD}	DC Supply, Commercial	+3.0 to +3.6	V
T_A	Operating Ambient Temperature	0 to +70	°C
T_J	Junction Temperature	≤150	°C

Table 3 Capacitance

Symbol	Parameter[1]	Min	Typ	Max	Unit
C_{IN}	Input Capacitance (5 V compatible)	–	3.0	–	pF
C_{OUT}	Output Capacitance	–	3.0	–	pF
C_{IO}	I/O Bus Capacitance	–	3.0	–	pF

1. Measurement conditions are V_{IN} = 3.3 V, T_A = 25 ˚C, and clock frequency = 1 MHz.

Table 4 DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IL}	Voltage Input Low		V_{SS} – 0.5	–	0.8	V
V_{IH}	Voltage Input High	5 V compatible	2.0	–	5.5	V
V_T	Switching Threshold		–	1.4	2.0	V
V_{OH}	Voltage Output High	I_{OH} = -4.0 mA	2.4	–	V_{DD}	V
V_{OL}	Voltage Output Low	I_{OL} = 4.0 mA I_{OL} = 6.0 mA	–	0.2	0.4	V
I_{IN}	Input Current	V_{IN} = V_{DD} or V_{SS}	–10	±1	10	µA
I_{OZ}	Current 3-State Output Leakage	V_{OUT} = V_{SS} or V_{DD}	–10	±1	10	µA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}	TBD	TBD	TBD	µA
I_{CC}	Dynamic Supply Current	V_{DD} = Max, f = 27 MHz	–	TBD	–	mA

1. Junction temperature range: 0 to 115 °C, ±5% power supply.

Pinout, Package, and Ordering Information

The L64017 is available in a 208-pin PQFP package. Table 5 provides ordering information for the L64017. Table 6 provides an alphabetical pin list for the PQFP package. Figure 4 shows the pinout. Figure 5 provides the 208-pin PQFP mechanical drawing.

Table 5 L64013 Ordering Information

Part Number	Order Number	Clock Frequency	Package Type	Operating Range
L64017	TBD	27 MHz	208-pin PQFP	Commercial

Table 6 Alphabetical Pin List for the 208-pin PQFP Package

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A0	155	AD17	69	CH_DATA4	177	PAR	82
A1	158	AD18	65	CH_DATA5	176	PCLK	39
A2	159	AD19	64	CH_DATA6	175	PD0	197
A3	160	AD20	63	CH_DATA7	174	PD1	196
A4	161	AD21	62	CS_N	137	PD2	195
A5	163	AD22	61	D0	145	PD3	194
A6	164	AD23	60	D1	146	PD4	193
A7	165	AD24	54	D2	147	PD5	192
A8	167	AD25	51	D3	148	PD6	191
A9	168	AD26	50	D4	151	PD7	190
ACLK	123	AD27	49	D5	152	PERR_N	80
AD0	108	AD28	48	D6	153	PIO0	112
AD1	107	AD29	47	D7	154	PIO1	113
AD2	106	AD30	46	DAC_LRCLK	132	PIO2	114
AD3	103	AD31	45	DAC_MCLK	130	PIO3	115
AD4	102	ADATA	122	DAC_SCLK	131	PIO4	118
AD5	98	AREQ_N	170	DAC_SDATA	129	PIO5	119
AD6	97	AS_N	144	DEVSEL_N	75	PIO6	120
AD7	96	AVALID_N	172	DS_N	138	PIO7	121
AD8	94	BCLK	124	FRAME_N	72	PO	33
AD9	93	C/BE0_N	95	GNT_N	40	PWM_REF	136
AD10	92	C/BE1_N	83	HS	202	PWRDWN_N	27
AD11	91	C/BE2_N	71	IDDT_N	198	READ	139
AD12	87	C/BE3_N	58	IDSEL	59	REQ_N	41
AD13	86	CH_DATA0	186	INTA_N	37	RESET_N	26
AD14	85	CH_DATA1	185	INTR_N	140	RST_N	38
AD15	84	CH_DATA2	184	IRDY_N	73	SCL	111
AD16	70	CH_DATA3	183	LRCLK	125	SDA	110

(Sheet 1 of 2)

Table 6 Alphabetical Pin List for the 208-pin PQFP Package (Cont.)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
SERR_N	81	VDD	78	VPDAT3	19	VSS	52
STOP_N	76	VDD	79	VPDAT4	17	VSS	53
SYSCLK_IN	127	VDD	89	VPDAT5	16	VSS	55
SYSCLK_OUT	142	VDD	90	VPDAT6	15	VSS	66
TCK	29	VDD	100	VPDAT7	14	VSS	77
TDI	30	VDD	101	VPDAT8	11	VSS	88
TDO	35	VDD	109	VPDAT9	10	VSS	99
TEST	25	VDD	116	VPDAT10	9	VSS	104
TM_OUT	133	VDD	126	VPDAT11	8	VSS	105
TMS	31	VDD	134	VPDAT12	5	VSS	117
TN	28	VDD	143	VPDAT13	4	VSS	128
TRDY_N	74	VDD	149	VPDAT14	3	VSS	135
TRST	34	VDD	156	VPDAT15	2	VSS	141
VDD	1	VDD	166	VPHREF1	204	VSS	150
VDD	7	VDD	179	VPHREF2	205	VSS	157
VDD	13	VDD	180	VPVREF	206	VSS	162
VDD	24	VDD	187	VREQ_N	171	VSS	169
VDD	36	VDD	199	VS	203	VSS	178
VDD	43	VDD	207	VSS	6	VSS	181
VDD	44	VDD	208	VSS	12	VSS	182
VDD	56	VPCLK	188	VSS	18	VSS	189
VDD	57	VPDAT0	22	VSS	23	VSS	200
VDD	67	VPDAT1	21	VSS	32	VSS	201
VDD	68	VPDAT2	20	VSS	42	VVALID_N	173

(Sheet 2 of 2)

Figure 4 208-pin PQFP Pinout

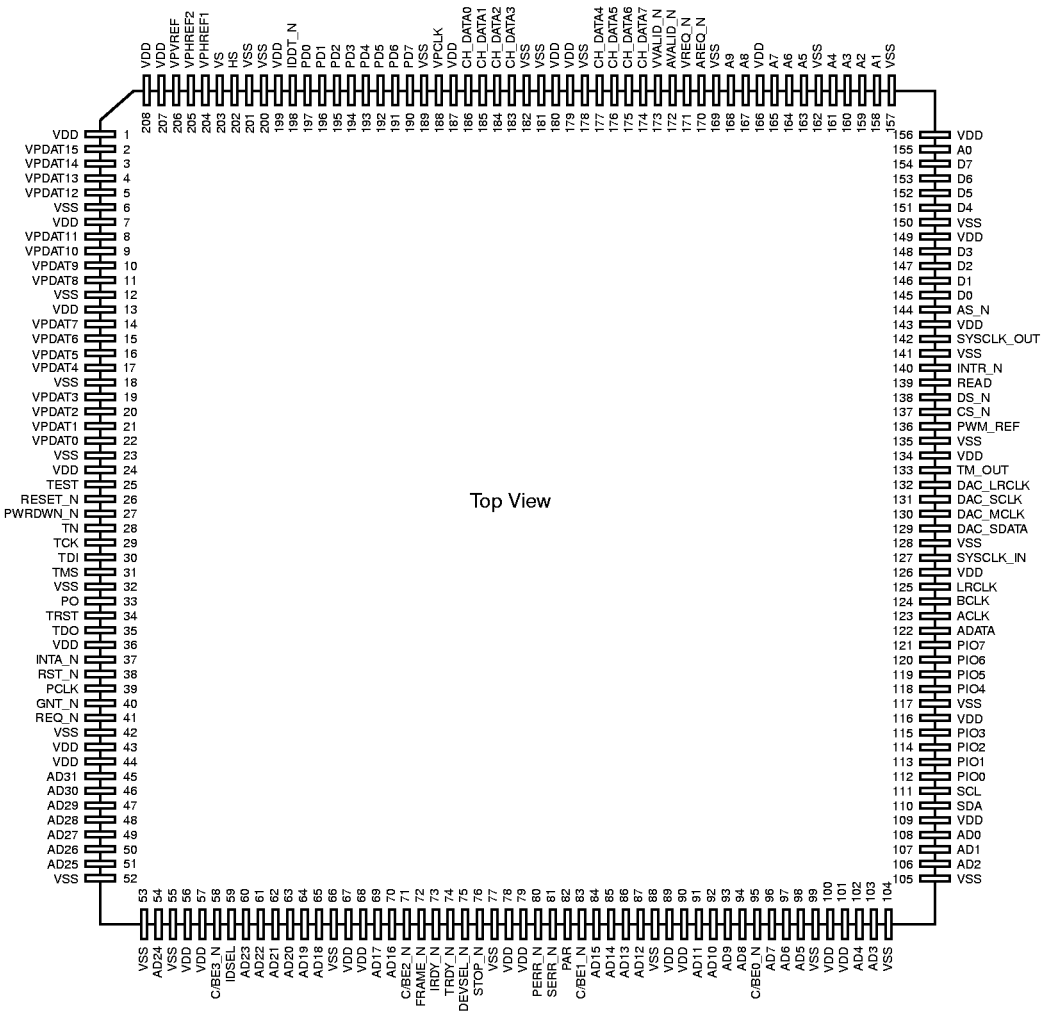
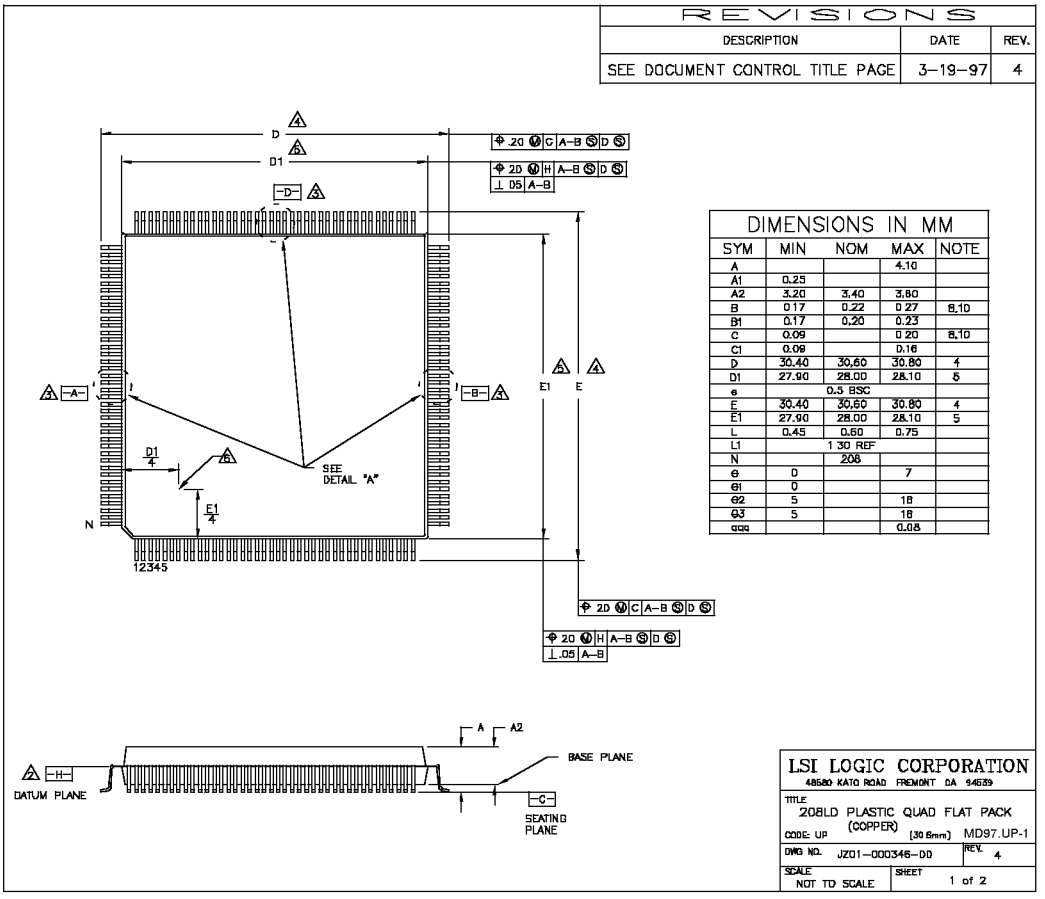
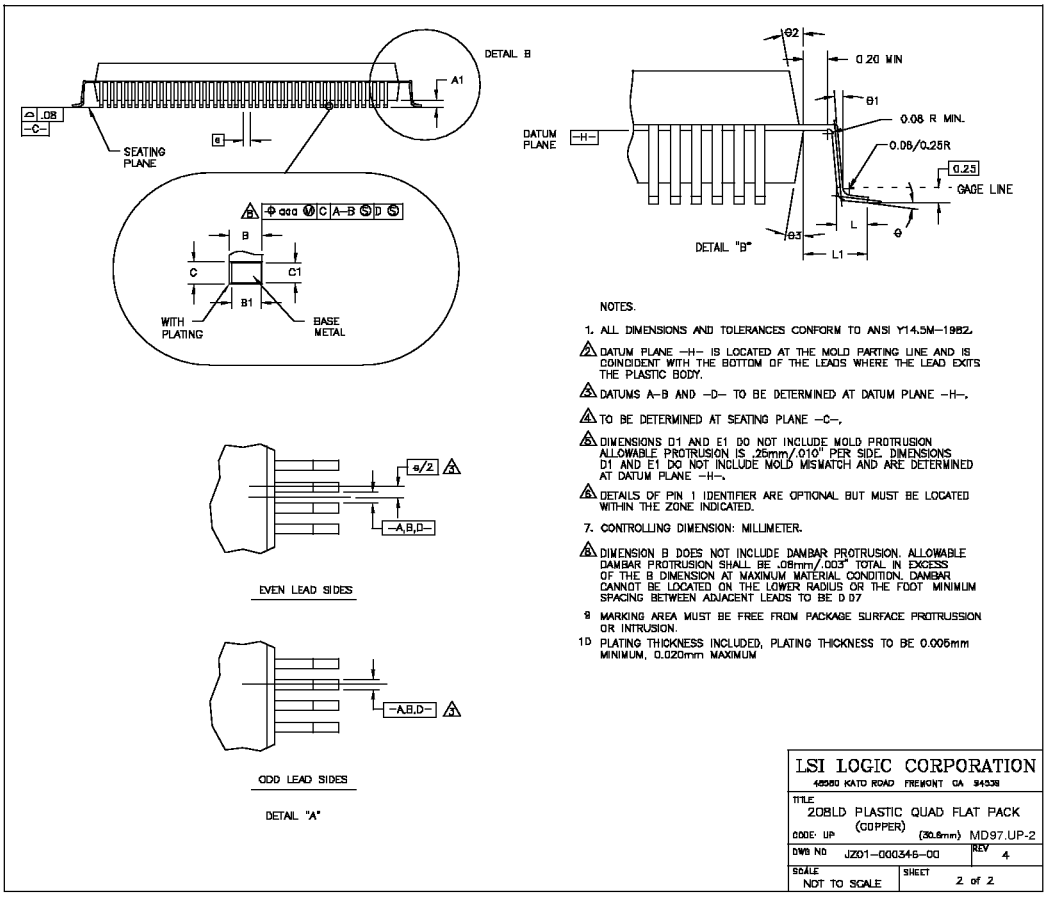


Figure 5 208 PQFP (UP) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UP.**

Figure 5 208 PQFP (UP) Mechanical Drawing (Cont.)



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