



# M2118 FAMILY

## 16,384 x 1 BIT DYNAMIC RAM

### MILITARY

	M2118-4	M2118-7
Maximum Access Time (ns)	120	150
Read, Write Cycle (ns)	270	320
Read-Modify Cycle (ns)	320	410

- Single +5V Supply, ±10% Tolerance
- HMOS Technology
- Low Power: 150 mW Max. Operating  
11 mW Max. Standby
- Low  $V_{DD}$  Current Transients
- All Inputs, Including Clocks, TTL Compatible
- $\overline{CAS}$  Controlled Output is Three-State, TTL Compatible
- $\overline{RAS}$  Only Refresh
- 128 Refresh Cycles Required Every 2ms
- Allows Negative Overshoot  $V_{IL\ min} = -2V$
- Military Temperature Range  $-55^\circ$  to  $+85^\circ C (T_C)$
- Not Recommended for New Designs

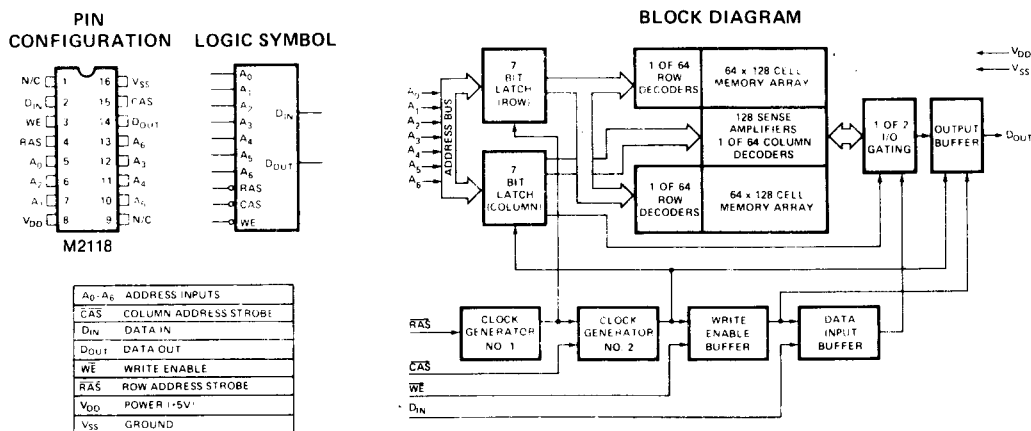
The Intel® M2118 is a 16,384 word by 1-bit Dynamic MOS RAM designed to operate from a single +5V power supply. The M2118 is fabricated using HMOS—a production proven process for high performance, high reliability, and high storage density.

The M2118 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients contribute to the high noise immunity of the M2118 in a system environment.

Multiplexing the 14 address bits into the 7 address input pins allows the M2118 to be packaged in the industry standard 16-pin DIP. The two 7-bit address words are latched into the M2118 by the two TTL clocks, Row Address Strobe ( $\overline{RAS}$ ) and Column Address Strobe ( $\overline{CAS}$ ). Non-critical timing requirements for  $\overline{RAS}$  and  $\overline{CAS}$  allow use of the address multiplexing technique while maintaining high performance.

The M2118 three-state output is controlled by  $\overline{CAS}$ , independent of  $\overline{RAS}$ . After a valid read or read-modify-write cycle, data is latched on the output by holding  $\overline{CAS}$  low. The data out pin is returned to the high impedance state by returning  $\overline{CAS}$  to a high state.

The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing  $\overline{RAS}$ -only refresh cycles, or normal read or write cycles on the 128 address combinations of  $A_0$  through  $A_6$  during a 2ms period. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.



**ABSOLUTE MAXIMUM RATINGS\***

Case Temperature Under Bias .....	-65°C to +95°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin Relative to $V_{SS}$ .....	7.5V
Data Out Current .....	50mA
Power Dissipation .....	1.0W

**\*COMMENT:**

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. AND OPERATING CHARACTERISTICS<sup>[1]</sup>**

$T_C^4 = -55^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ , unless otherwise noted.

Symbol	Parameter	Limits			Unit	Test Conditions	Notes
		Min	Typ <sup>[2]</sup>	Max			
$ I_{LI} $	Input Load Current (any input)		0.1	10	$\mu\text{A}$	$V_{IN}=V_{SS}$ to $V_{DD}$	
$ I_{LO} $	Output Leakage Current for High Impedance State		0.1	10	$\mu\text{A}$	Chip Deselected: $\overline{\text{CAS}}$ at $V_{IH}$ , $V_{OUT} = 0$ to $5.5V$	
$I_{DD1}$	$V_{DD}$ Supply Current, Standby		1.2	2	mA	$\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ at $V_{IH}$	
$I_{DD2}$	$V_{DD}$ Supply Current, Operating		21	25	mA	M2118-4, $t_{RC} = t_{RCMIN}$	3
			19	23	mA	M2118-7, $t_{RC} = t_{RCMIN}$	3
$I_{DD3}$	$V_{DD}$ Supply Current, $\overline{\text{RAS}}$ -Only Cycle		14	16	mA	M2118-4, $t_{RC} = t_{RCMIN}$	3
			12	14	mA	M2118-7, $t_{RC} = t_{RCMIN}$	3
$I_{DD5}$	$V_{DD}$ Supply Current, Standby, Output Enabled		2	4	mA	$\overline{\text{CAS}}$ at $V_{IL}$ , $\overline{\text{RAS}}$ at $V_{IH}$	3
$V_{IL}$	Input Low Voltage (all inputs)	-2.0		0.8	V		
$V_{IH}$	Input High Voltage (all inputs)	2.4		7.0	V		
$V_{OL}$	Output Low Voltage			0.4	V	$I_{OL} = 4.2\text{mA}$	
$V_{OH}$	Output High Voltage	2.4			V	$I_{OH} = -5\text{mA}$	

**NOTES:**

- All voltages referenced to  $V_{SS}$ .
- Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltages.
- $I_{DD}$  is dependent on output loading when the device output is selected. Specified  $I_{DDMAX}$  is measured with the output open.
- Case temperatures are "instant on."

**CAPACITANCE<sup>[1]</sup>**

$T_C^2 = 25^\circ\text{C}$ ,  $V_{DD} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ , unless otherwise noted.

Symbol	Parameter	Typ	Max	Unit
$C_{I1}$	Address, Data In	3	5	pF
$C_{I2}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , Data Out	4	7	pF

**NOTES:**

- Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I\Delta t}{\Delta V} \text{ with } \Delta V \text{ equal to 3 volts and power supplies at nominal levels.}$$

- Case temperatures are "instant on."

**A.C. CHARACTERISTICS** [1,2,3]

 $T_C^{10} = -55^{\circ}\text{C to } +85^{\circ}\text{C}$ ,  $V_{DD} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ , unless otherwise noted. 1.

**READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES**

Symbol	Parameter	M2118-4		M2118-7		Unit	Notes
		Min.	Max.	Min.	Max.		
t <sub>RAC</sub>	Access Time From $\overline{\text{RAS}}$	120		150		ns	4,5
t <sub>ICAS</sub>	Access Time From $\overline{\text{CAS}}$	65		80		ns	4,5,6
t <sub>REF</sub>	Time Between Refresh	2		2		ms	
t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	120		135		ns	
t <sub>CPN</sub>	$\overline{\text{CAS}}$ Precharge Time (non-page cycles) <sup>1</sup>	55		70		ns	
t <sub>CRP</sub>	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	0		0		ns	
t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	25	55	25	70	ns	7
t <sub>RSH</sub>	$\overline{\text{RAS}}$ Hold Time	85		105		ns	
t <sub>CSH</sub>	$\overline{\text{CAS}}$ Hold Time	120		165		ns	
t <sub>ASR</sub>	Row Address Set-Up Time	0		0		ns	
t <sub>RAH</sub>	Row Address Hold Time	15		15		ns	
t <sub>ASC</sub>	Column Address Set-Up Time	0		0		ns	
t <sub>CAH</sub>	Column Address Hold Time	15		20		ns	
t <sub>AR</sub>	Column Address Hold Time, to $\overline{\text{RAS}}$	70		90		ns	
t <sub>T</sub>	Transition Time (Rise and Fall) <sup>1</sup>	3	50	3	50	ns	8
t <sub>OFF</sub>	Output Buffer Turn Off Delay	0		50		ns	

**READ AND REFRESH CYCLES**

t <sub>RC</sub>	Random Read Cycle Time	270		320		ns	
t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	140	10000	175	10000	ns	
t <sub>CAS</sub>	$\overline{\text{CAS}}$ Pulse Width	65	10000	95	10000	ns	
t <sub>RCS</sub>	Read Command Set-Up Time	0		0		ns	
t <sub>RCH</sub>	Read Command Hold Time	0		0		ns	

**WRITE CYCLE**

t <sub>RC</sub>	Random Write Cycle Time	270		320		ns	
t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	140	10000	175	10000	ns	
t <sub>CAS</sub>	$\overline{\text{CAS}}$ Pulse Width	65	10000	95	10000	ns	
t <sub>WCS</sub>	Write Command Set-Up Time	0		0		ns	9
t <sub>WCH</sub>	Write Command Hold Time	30		45		ns	
t <sub>WCR</sub>	Write Command Hold Time, to $\overline{\text{RAS}}$	85		115		ns	
t <sub>WP</sub>	Write Command Pulse Width	30		50		ns	
t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time	65		110		ns	
t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time	50		100		ns	
t <sub>DS</sub>	Data-In Set-Up Time	0		0		ns	
t <sub>DH</sub>	Data-In Hold Time	30		45		ns	
t <sub>DHR</sub>	Data-In Hold Time, to $\overline{\text{RAS}}$	85		115		ns	

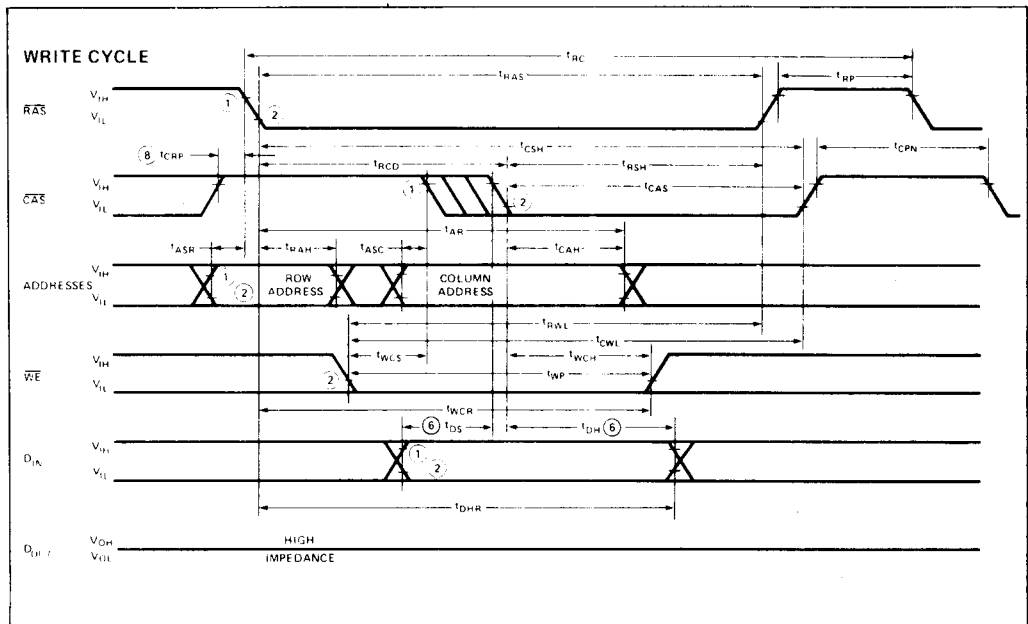
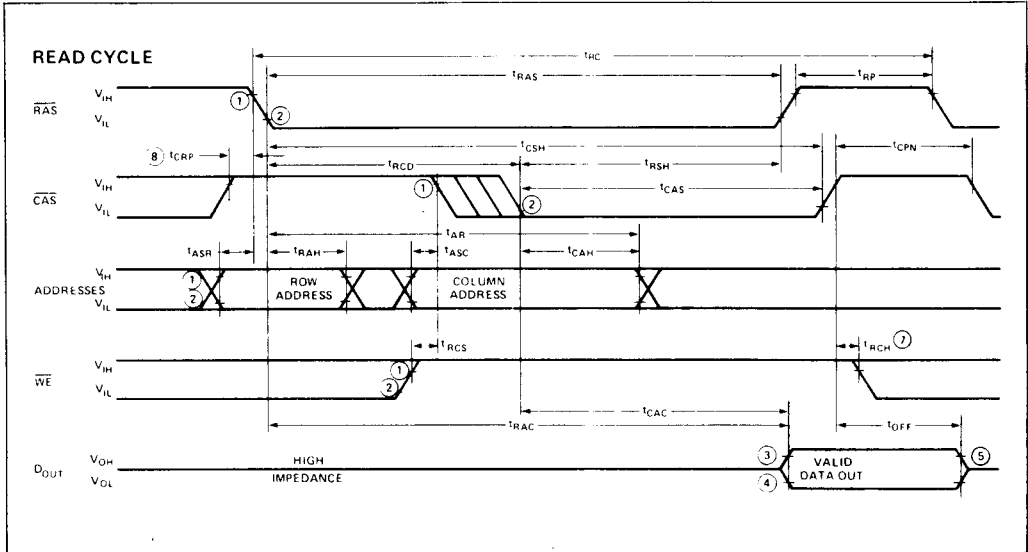
**READ-MODIFY-WRITE CYCLE**

t <sub>RWC</sub>	Read-Modify-Write Cycle Time	320		410		ns	
t <sub>RRW</sub>	RMW Cycle $\overline{\text{RAS}}$ Pulse Width	190	10000	265	10000	ns	
t <sub>CRW</sub>	RMW Cycle $\overline{\text{CAS}}$ Pulse Width	120	10000	185	10000	ns	
t <sub>RWD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay	120		150		ns	9
t <sub>CWD</sub>	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	65		80		ns	9

**NOTES:**

- All voltages referenced to  $V_{SS}$ .
- Eight cycles are required after power up or prolonged periods (greater than 2ms) of  $\overline{\text{RAS}}$  inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- A.C. Characteristics assume  $t_r = 5\text{ns}$ .
- Assume that  $t_{RCD} \approx t_{RCD}(\text{max.})$ . If  $t_{RCD}$  is greater than  $t_{RCD}(\text{max.})$  then  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds  $t_{RCD}(\text{max.})$ .
- Load = 2 TTL loads and 100pF.
- Assumes  $t_{RCD} \geq t_{RCD}(\text{max.})$ .
- $t_{RCD}(\text{max.})$  is specified as a reference point only. If  $t_{RCD}$  is less than  $t_{RCD}(\text{max.})$  access time is  $t_{RAC}$ . If  $t_{RCD}$  is greater than  $t_{RCD}(\text{max.})$  access time is  $t_{RCD} + t_{CAC}$ .
- $t_r$  is measured between  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$ .
- $t_{WCS}$ ,  $t_{CWD}$  and  $t_{RWD}$  are specified as reference points only. If  $t_{WCS} \approx t_{WCS}(\text{min.})$  the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If  $t_{CWD} \approx t_{CWD}(\text{min.})$  and  $t_{RWD} \approx t_{RWD}(\text{min.})$  the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
- Case temperatures are "instant on."

WAVEFORMS



- NOTES
- $V_{IH}$  MIN AND  $V_{IL}$  MAX ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS
  - $V_{OH}$  MIN AND  $V_{OL}$  MAX ARE REFERENCE LEVELS FOR MEASURING TIMING OF  $D_{OUT}$
  - $t_{OFF}$  IS MEASURED TO  $I_{OUT} < I_{IO}$
  - $t_{DS}$  AND  $t_{DH}$  ARE REFERENCED TO  $\overline{CAS}$  OR  $\overline{WE}$ , WHICHEVER OCCURS LAST
  - $t_{RCH}$  IS REFERENCED TO THE TRAILING EDGE OF  $\overline{CAS}$  OR  $\overline{RAS}$ , WHICHEVER OCCURS FIRST
  - $t_{CRP}$  REQUIREMENT IS ONLY APPLICABLE FOR  $\overline{RAS}$ ,  $\overline{CAS}$  CYCLES PRECEDED BY A  $\overline{CAS}$  ONLY CYCLE (i.e. FOR SYSTEMS WHERE  $\overline{CAS}$  HAS NOT BEEN DECODED WITH  $\overline{RAS}$ )

