One Chip Frontend 1 (OCF1) SAA7110/SAA7110A

SHORT DESCRIPTION

The one chip frontend SAA7110(A) is a digital multistandard colour decoder (OCF1) on the basis of the digital TV-2 system with 2 integrated A/D converters, a clock generation circuit (CGC) and BCS- (Brightness, Contrast, Saturation) control.

FEATURES

- Six analog inputs (six times CVBS or three times Y/C or combinations)
- Three analog processing channels
- Three built in analog anti alias filters
- Analog signal adding of two channels
- Two Video CMOS 8-bit A/D- converters
- Full programmable static gain for the main channels or automatic gain control for the selected CVBS/Y channel
- Selectable signal (white) peak control
- Luminance and chrominance signal processing for standards PAL-B/G, NTSC-M, SECAM
- Full range HUE control
- Automatic detection of 50/60Hz field frequency->automatic switching between standards PAL and NTSC, SECAM forceable
- Horizontal and vertical sync detection for all standards
- Cross-colour reduction by chrominance comb filtering for NTSC or special cross-colour cancellation for SECAM
- UV signal delay lines for PAL to correct chrominance phase errors
- The YUV bus supports a data rate of:
  (780 x f_h) for 60 Hz 12.2727MHz (NTSC)
  (944 x f_h) for 50 Hz 14.75MHz (PAL/SECAM)
- Square pixel-format with 768/640 active samples per line on the YUV bus
- CCIR 601 level compatible
- 4:2:2 and 4:1:1 YUV output formats in 8-bit resolution
- User programmable luminance peaking for aperture correction
- Compatible with memory-based features (line-locked clock, square pixel)
- Requires only one crystal (26.8MHz) for all standards
- Real-time status information output (RTCO)
- Brightness Contrast Saturation control for the YUV-bus
- Negation of picture possible
- One user programmable general purpose switch on an output pin
- Switchable between on-chip Clock Generation Circuit (CGC) and external CGC (SAA7197)
- Power On Control
- I^2C-bus controlled

APPLICATIONS

- Desktop Video
- Multimedia
- Digital Television
- Image Processing
- Video Phone
- Video Picture Grabbing

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	digital supply voltage range	4.5	5.5	V
V_{DDA}	analog supply voltage range	4.75	5.25	V
T_{amb}	ambient temperature range	0	70	°C

ORDERING AND PACKAGE INFORMATION

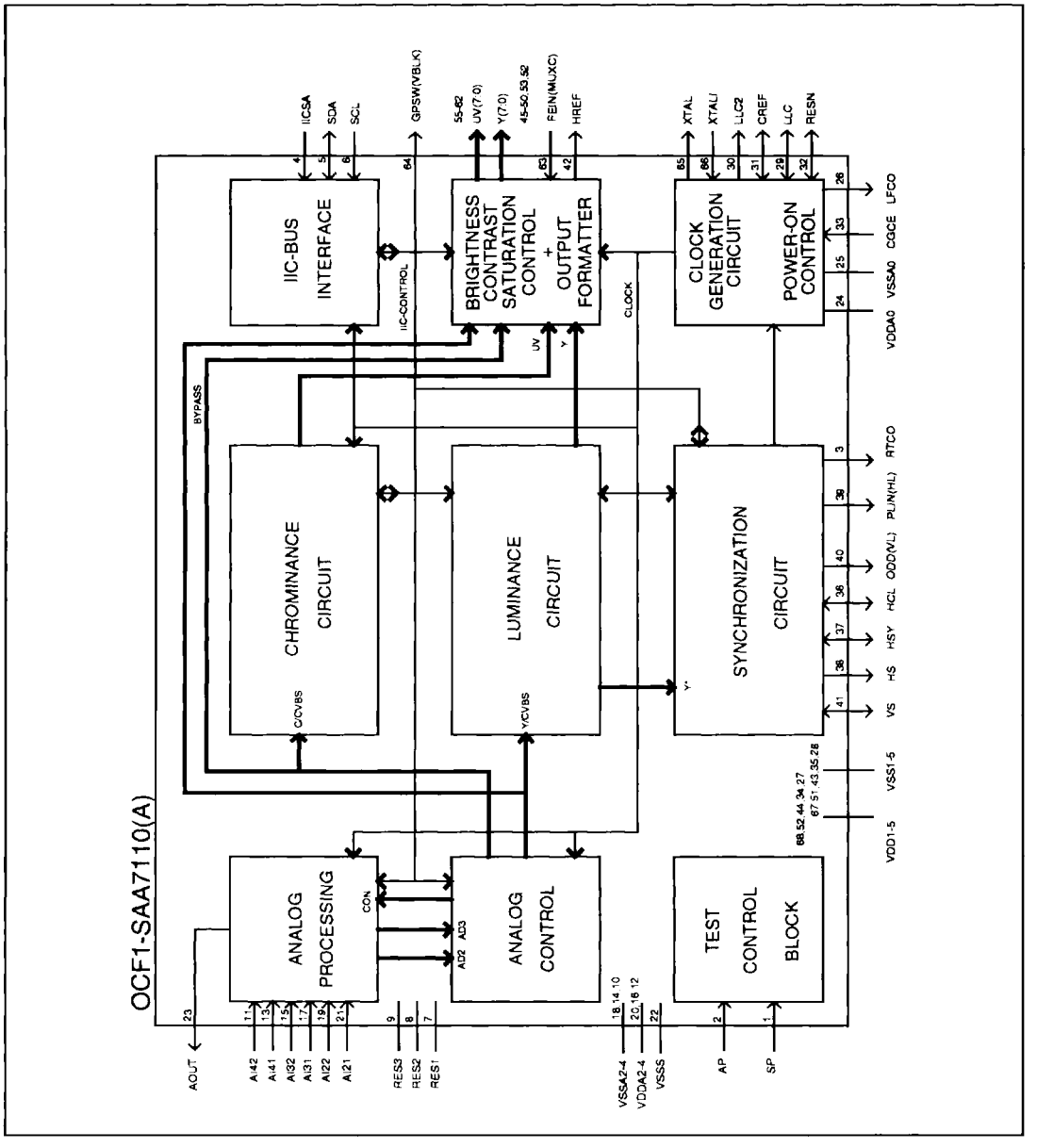
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7110(A)	68	PLCC	Plastic	SOT188

GENERAL DESCRIPTION

The CMOS circuit SAA7110(A), analog frontend and digital video decoder, is a highly integrated circuit for Desk Top Video applications. The decoder is based on the principle of line-locked clock decoding. It runs square-pixel frequencies to achieve correct aspect ratio. Monitor controls are provided to ensure best display. The circuit is I^2C-bus-controlled.

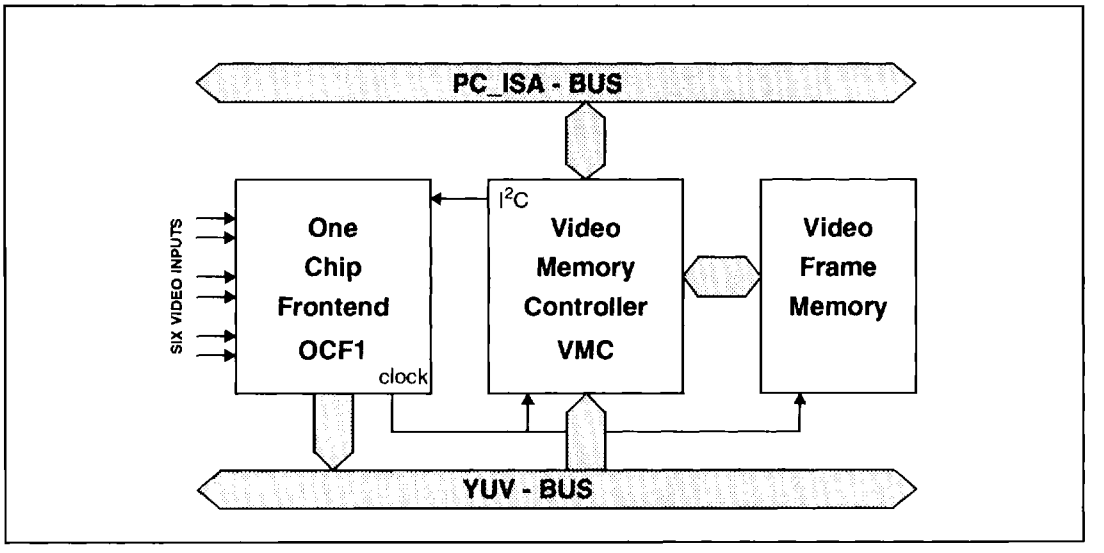
1. BLOCK DIAGRAM

FIGURE 1. BLOCK DIAGRAM



2. SYSTEM VIEW

FIGURE 2. SYSTEM VIEW



3. PINNING

PIN NO.	SYMBOL	I/O/P	DESCRIPTION
1	SP	I	SHIFT PIN for testing; connect to ground in normal operation
2	AP	I	ACTION PIN for testing; connect to ground in normal operation
3	RTCO	O	Real Time Control Output. This pin is used to fit out serially the increments of the HPLL and FSC-PLL and an information of the PAL- or SECAM-sequence
4	IICSA	I	IIC Slave Address select (0=9Ch(for write), 9Dh for read; 1=9Eh (for write), 9Fh for read)
5	SDA	I/O	I²C-bus SERIAL DATA input/output
6	SCL	I	I²C-bus SERIAL CLOCK input
7	RES1	-	Reserved pin 1 (do not connect))
8	RES2	-	Reserved pin 2 (do not connect))
9	RES3	-	Reserved pin 3 (do not connect))
10	V_{SSA4}	P	ground for analog input 4
11	AI42	I	analog input 42
12	V_{DDA4}	P	positive supply voltage (+5 V) for analog input 4
13	AI41	I	analog input 41
14	V_{SSA3}	P	ground for analog input 3
15	AI32	I	analog input 32
16	V_{DDA3}	P	positive supply voltage (+5 V) for analog input 3
17	AI31	I	analog input 31

TABLE 1. PINNING

PIN NO.	SYMBOL	I/O/P	DESCRIPTION
18	V_{SSA2}	P	ground for analog input 2
19	AI22	I	analog input 22
20	V_{DDA2}	P	positive supply voltage (+5 V) for analog input 2
21	AI21	I	analog input 21
22	V_{SSS}	P	SUBSTRATE ground connection
23	AOUT	O	Analog test OUTput (do not connect).
24	V_{DDA0}	P	positive supply voltage (+5 V) for internal CGC (Clock Generation Circuit)
25	V_{SSA0}	P	ground for internal CGC
26	LFCO	O	LINE FREQUENCY CONTROL output signal; this is the analog clock control signal driving the external CGC. The frequency is a multiple of the actual line frequency (nominally 7.375/6.13636 MHz). The signal has triangular form with a 4-bit accuracy.
27	V_{DD5}	P	positive supply voltage (+5 V)
28	V_{SS5}	P	ground
29	LLC	I/O	LINE LOCKED CLOCK I/O (CGCE=1 -> output; CGCE=0 -> input); this is the system clock, its frequency is $1888*f_h$ for 50 Hz/625 lines per field systems and $1560*f_h$ for 60 Hz/525 lines per field systems; or variable input clock up to 32MHz in input mode.
30	LLC2	O	Line Locked Clock output; $f_{LLC2}=0.5xf_{LLC}$; (CGCE=1 -> output; CGCE=0 -> High impedance)
31	CREF	I/O	CLOCK REFERENCE I/O (CGCE=1 -> output; CGCE=0 -> input). This is a clock qualifier signal distributed by the internal or an external clock generator circuit (CGC). Using CREF all interfaces on the YUV bus are able to generate a bus timing with identical phase.
32	RESN	I/O	RESET active LOW I/O (CGCE=1 -> output; CGCE=0 -> input); sets the device into a defined state. All data outputs are in high impedance state. The I^2C-bus is reset (waiting for start condition). Using the external CGC, the LOW period must be maintained for at least 30 LLC clock cycles.
33	CGCE	I	CGC Enable input signal, active HIGH; (CGCE=1 -> On chip CGC active; CGCE=0 -> External CGC mode: use SAA7197)
34	V_{DD4}	P	positive supply voltage (+5V)
35	V_{SS4}	P	ground
36	HCL	I/O	HORIZONTAL CLAMPING pulse I/O (programmable via IIC-bit PULIO, PULIO=1 -> output, PULIO=0 -> input); this signal is used to indicate the black level clamping period for the analog input interface. The beginning and end of its HIGH period (only in the output mode) can be programmed via the I^2C-bus register 03h, 04h in 50 Hz mode and registers 16h, 17h in 60 Hz mode, active HIGH.
37	HSY	I/O	HORIZONTAL SYNC indicator signal I/O (programmable via IIC-bit PULIO, PULIO=1 -> output, PULIO=0 -> input); is used to indicate the sync tip part of the CVBS input signal for gain control purposes. This signal is fed to the analog interface. The beginning and end of its HIGH period (only in the output mode) can be programmed via the I^2C-bus register 01h, 02h in 50 Hz mode and registers 14h, 15h in 60 Hz mode, active HIGH.

TABLE 1. PINNING

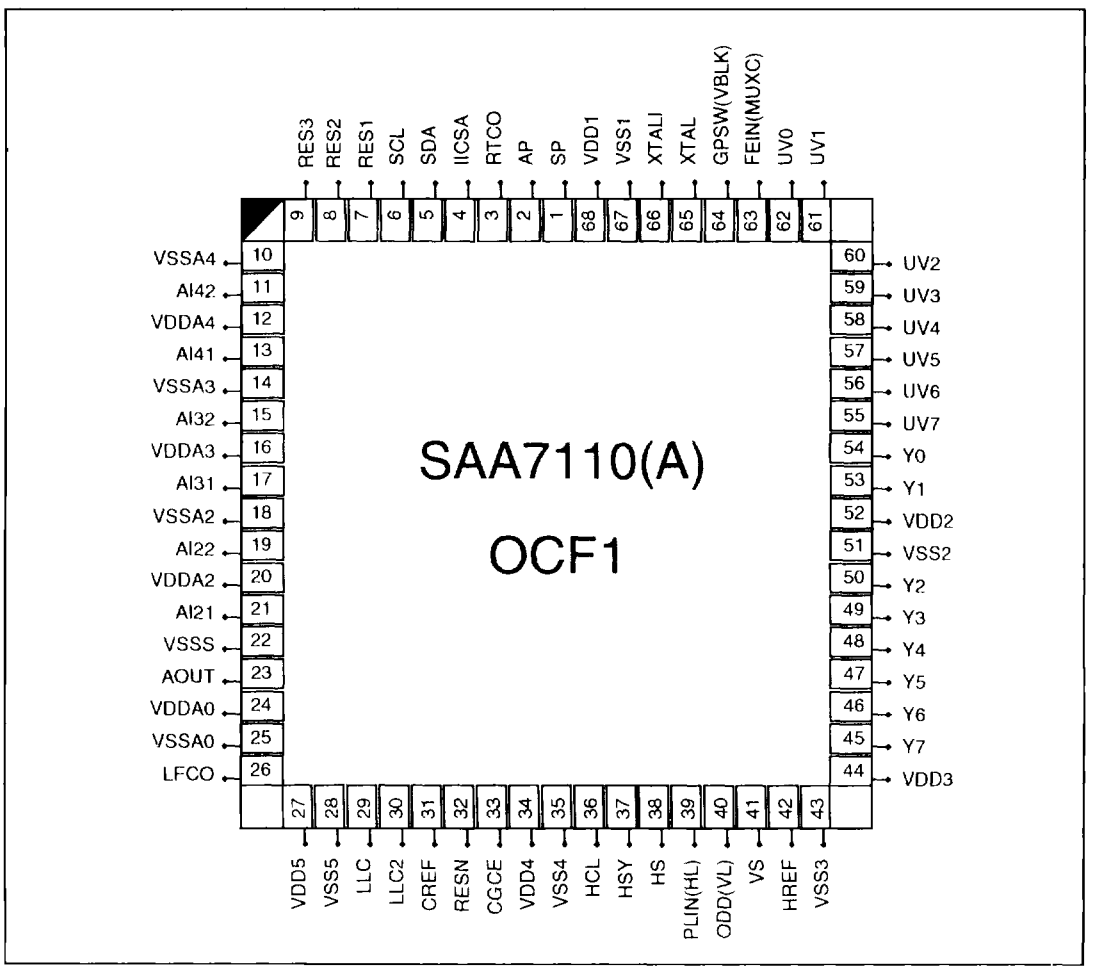
PIN NO.	SYMBOL	I/O/P	DESCRIPTION
38	HS	O	HORIZONTAL SYNC output signal (programmable; the high period is 128 LLC clock cycles. The position of the positive slope is programmable in 8 LLC increments over a complete line (=64 us) via I^2C-bus register 05h (50 Hz mode) or 18h (60 Hz mode).
39	PLIN (HL)	O	PAL IDENTIFIER NOT output signal; marks for demodulated PAL signals the inverted line (PLIN=LOW) and a non inverted line (PLIN=HIGH) and for demodulated SECAM signals the DR line (PLIN=LOW) and the DB line (PLIN=HIGH). Select PLIN function via IIC-bit RTSE=0. (H-PLL LOCKED output signal; a HIGH state indicates that the internal PLL has locked; select HL function via I^2C-bit RTSE=1).
40	ODD (VL)	O	ODD/EVEN field identification (output); a HIGH state indicates the odd field. Select ODD function via IIC-bit RTSE=0. (VERTICAL LOCKED output signal; a HIGH state indicates that the internal VNL is in a locked state; select VL function via I^2C-bit RTSE=1).
41	VS	I/O	VERTICAL SYNC signal I/O (programmable via IIC-bit OEHV, OEHV=1 -> output, OEHV=0 -> input); this signal indicates the vertical sync with respect to the YUV output. The high period of this signal is approximate six lines if the vertical noise limiter (VNL) function is active. The positive slope contains the phase information for a deflection controller, e.g. TDA9150. In input mode, this signal is used to synchronize the vertical gain- and clamp-blanking stage, active HIGH.
42	HREF	O	HORIZONTAL REFERENCE output signal; this signal is used to indicate data on the digital YUV bus. The positive slope marks the beginning of a new active line. The HIGH period of HREF is either 768 Y samples or 640 Y samples long depending on the detected field frequency (50/60 Hz-mode). HREF is used to synchronize data multiplexer / demultiplexers. HREF is also present during the vertical blanking interval.
43	V_{SS3}	P	ground
44	V_{DD3}	P	positive supply voltage (+5 V)
45-50	Y (7-2)	O	Digital Y (luminance) output signal; higher 6 bits of the 8-bit luminance output signal as part of the digital YUV bus (data rate LLC/2), or A/D2(3) output (data rate LLC/2) selectable via IIC-bit SQPB=1.
51	V_{SS2}	P	ground
52	V_{DD2}	P	positive supply voltage (+5 V)
53-54	Y (1-0)	O	Digital Y (luminance) output signal; lower 2 bits of the 8-bit luminance output signal as part of the digital YUV bus (data rate LLC/2), or A/D2(3) output (data rate LLC/2) selectable via IIC-bit SQPB=1
55-62	UV (7-0)	O	Digital UV (color difference) output signal; multiplexed color difference signal for U and V component of demodulated CVBS or Chroma signal. The format and multiplexing scheme can be selected via I^2C-bus control. These signals are part of the digital YUV bus (data rate LLC/4), or A/D3(2) output (data rate LLC/2) selectable via IIC-bit SQPB=1
63	FEIN (MUXC)	I	FAST ENABLE INPUT signal (active LOW); this signal is used to control fast switching on the digital YUV bus. A HIGH at this input forces the IC to set its Y and UV outputs to the high impedance state.(Set IIC-bits MS24 and MS34 and MUYC to LOW to use the FEIN function). (MULTIPLEX COMPONENTS (input signal); control signal for the analog multiplexers for fast switching between locked Y/C signals or locked CVBS signals. FEIN automatically fixed to LOW (Digital YUV bus enabled), if one of the three MUXC functions are selected (MS24 or MS34 or MUYC = HIGH)

TABLE 1. PINNING

PIN NO.	SYMBOL	I/O/P	DESCRIPTION
64	GPSW (VBLK)	O	GENERAL PURPOSE SWITCH (output signal); the state of this signal is programmable via I^2C-bus register 0Dh, bit 1; select GPSW function via IIC-bit VBLKA =0. (Vertical BLanK test output; select VBLK function via IIC-bit VBLKA =1)
65	XTAL	O	26.8 MHz crystal oscillator output; not connected if TTL clock signal is used
66	XTALI	I	Input terminal for 26.8 MHz crystal oscillator or connection of external oscillator with TTL compatible square wave clock signal.
67	V_{SS1}	P	ground
68	V_{DD1}	P	positive supply voltage (+5 V)

TABLE 1. PINNING

FIGURE 3. PINNING OCF1-SAA7110(A)



4. FUNCTIONAL DESCRIPTION

ANALOG INPUT PROCESSING

The OCF1 offers six analog signal inputs, two analog main channels with clamp circuit, analog amplifier, anti alias filter, and video CMOS ADC. A third analog channel also with clamp circuit, analog amplifier, anti alias filter can be added or switched to both main channels directly before the ADCs.

ANALOG CONTROL CIRCUITS

The clamp control circuit controls the proper clamping of the analog input signals. The coupling capacitor is also used to storage and filter the clamping voltage. The normal digital clamping level for luminance or CVBS signals is 64 and for chrominance signals 128.

The gain control circuits generate via I^2C the static gain levels for the three analog amplifiers or controls one of these amplifiers automatically via a build in Automatic Gain Control AGC. The AGC is only used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range.

The anti alias filters are adapted to the clock frequency.

The vertical blanking control circuit generates a I^2C programmable vertical blanking pulse. During the vertical blanking time gain and clamping control were frozen.

The fast switch control circuit is used for special applications.

CHROMINANCE PROCESSING

The 8-bit chrominance signal passes the input interface, the chrominance bandpass filter to eliminate DC components, and is finally fed to the multiplication inputs of a quadrature demodulator, where two subcarrier signals from the local oscillator (DTO1) with 90 degree phase shift are applied. The frequency is dependent on the present colour standard.

The multiplier operates as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down mixer for SECAM signals.

The two multiplier output signals are converted to a serial UV data stream and applied to two lowpass filter stages, then to a gain controlled amplifier. A final multiplexed lowpass filter achieves, together with the preceding stages, the required bandwidth performance.

The from PAL and NTSC originated signal are applied to a comb filter.

The signal, originated from SECAM is fed through a cloche-filter (0 Hz center frequency), a phase demodulator and a differentiator to obtain frequency- demodulated colour-difference signals. The SECAM signal is fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are fed to the BCS control and finally to the output formatter stage and to the output interface.

LUMINANCE PROCESSING

The 8-bit luminance signal, a digital CVBS format or a luminance format (S-VHS, HI8), is fed through a switchable prefilter. High frequency components are emphasized to compensate for loss. The following chrominance trap filter (f_0 = 4.43 MHz or f_0 = 3.58 MHz center frequency selectable) eliminates most of the colour carrier signal, therefore, it must be by-passed for S-Video (S-VHS, HI8) signals.

The high frequency components of the luminance signal can be "peaked" (control for sharpness improvement via I^2C bus) in two bandpass filters with selectable transfer characteristic.

A coring circuit with selectable characteristic improves the signal once more, this signal is then added to the original ('unpeaked') signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes.

The improved luminance signal is fed via the variable delay compensation to the BCS-control and the output interface.

YUV-BUS, DIGITAL OUTPUTS

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or a field memory, a digital colour space converter (SAA 7192 DCSC) or a Video enhancement and D/A processor (SAA7165 VEDA2). The outputs are controlled via the I^2C bus in normal selections, or they are controlled by an output enable chain (FEIN on pin 63).

The YUV data rate equals LLC2. Timing is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference).

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the multiplexed colour difference signals (B-Y) and (R-Y). The frame in the format tables is the time, required to transfer a full set of samples. In case of 4:2:2 format two luminance samples are transmitted in comparison to one U and one V sample within the frame. The time frames are controlled by the HREF signal.

Fast enable is achieved by setting input FEIN to LOW. The signal is used to control fast switching on the digital YUV-bus. High on this pin forces the Y and UV outputs to a high-impedance state.

SYNCHRONIZATION

The prefiltered luminance signal is fed to the synchronization stage. It's bandwidth is reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency.

The resulting output signal is applied to the loop filter to accumulate all phase deviations. Adjustable output signals (e. g. HCL and HSY) are generated according to analog frontend requirements. The output signals HS, VS, and PLIN are locked to the timing reference guaranteed between the input signal and the HREF signal as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications, which ask for absolute timing accuracy to the input signals. The loop filter signal drives an oscillator to generate the line frequency control output signal LFCO.

CLOCK GENERATION CIRCUIT

The internal CGC generates all clock signals required in the one chip frontend. The output signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency:

7.38 MHz = 472 x f_H in 50 Hz systems
6.14 MHz = 360 x f_H in 60 Hz systems
Internally the LFCO signal is multiplied by factors 2 or 4 in the PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to get the LLC and LLC2 output clock signals. The rectangular output clocks have a 50% duty factor.
It's also possible to operate the OCF1 with an external CGC (SAA7197) providing the signals LLC and CREF for the OCF1. The selection of the intern/external CGC will be controlled by the CGCE input signal.

POWER-ON RESET
Power-on reset is activated at power-on (only using internal CGC), when the supply voltage decreases below 3.5 V. The indicator output RESN is LOW for a time. The RESN signal can be applied to reset other circuits of the digital TV system.

RTCO OUTPUT
This real time control and status output signal contains serial information about actual system clock, subcarrier frequency and PAL/SECAM sequence. The signal can be used for various applications in external circuits, e. g. in a digital encoder to achieve "clean" encoding.

FIGURE 4. BLOCK PICTURE Analog Input and Analog Control Part

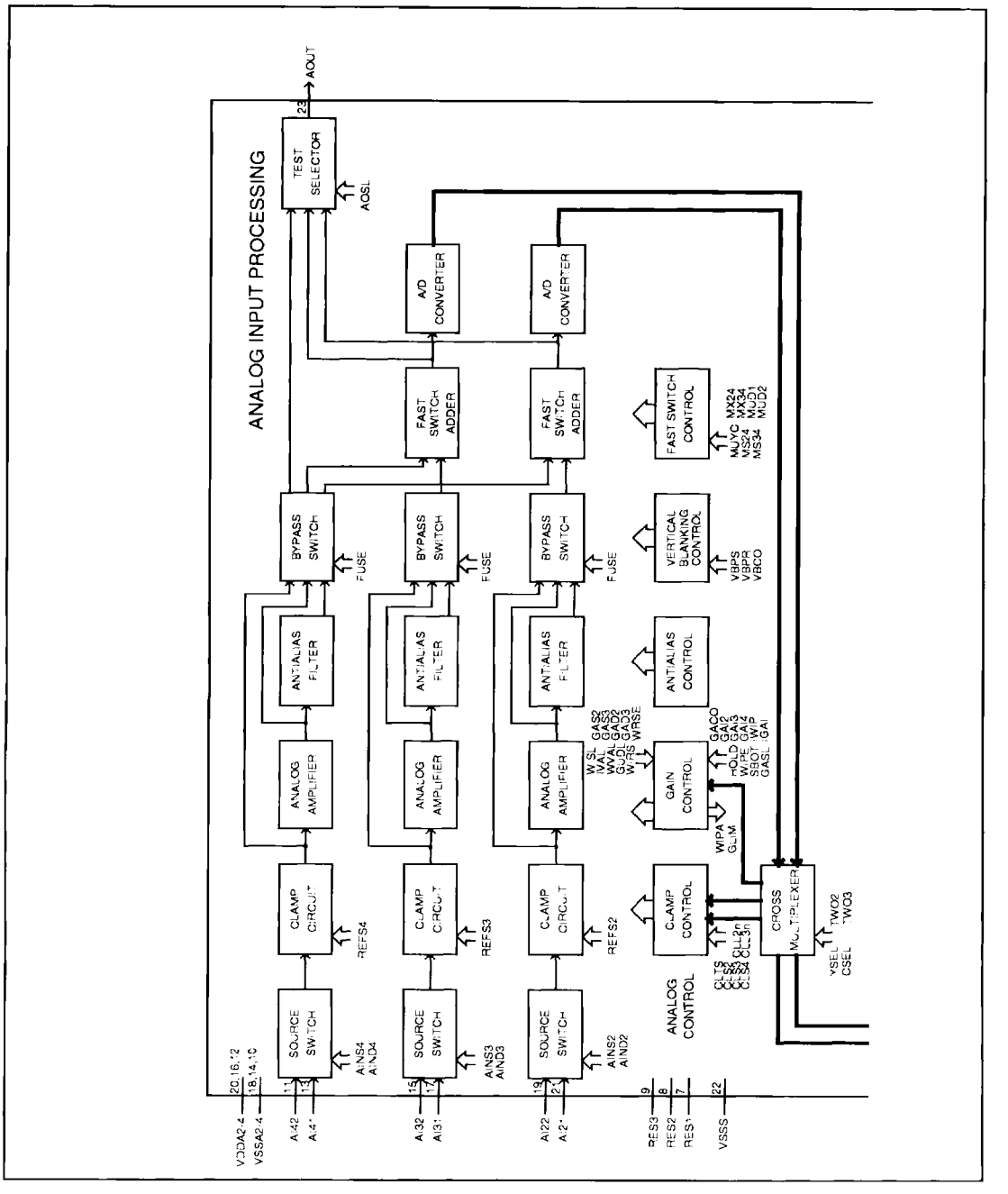


FIGURE 5. BLOCK PICTURE Multi-Standard Decoder Part

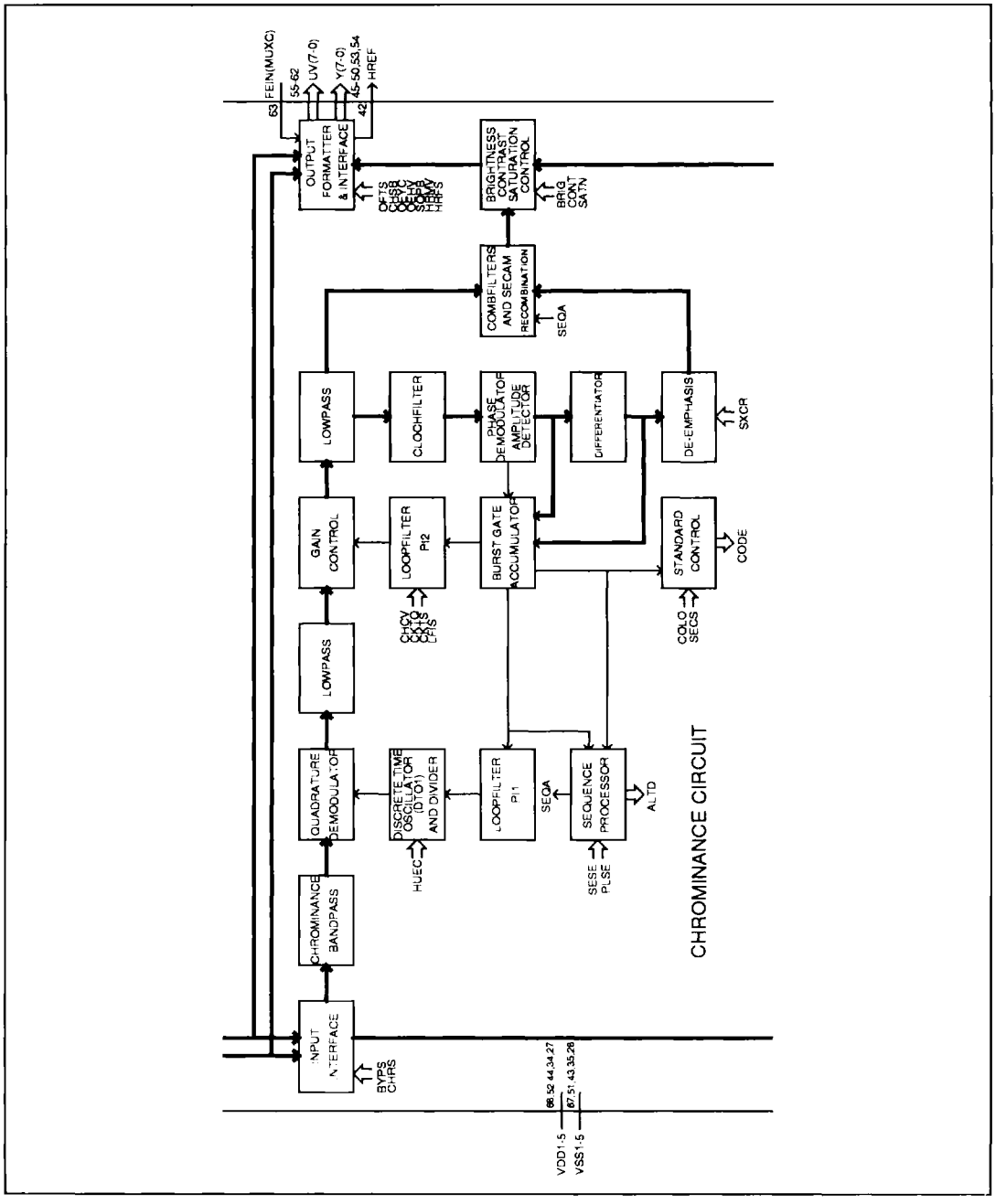
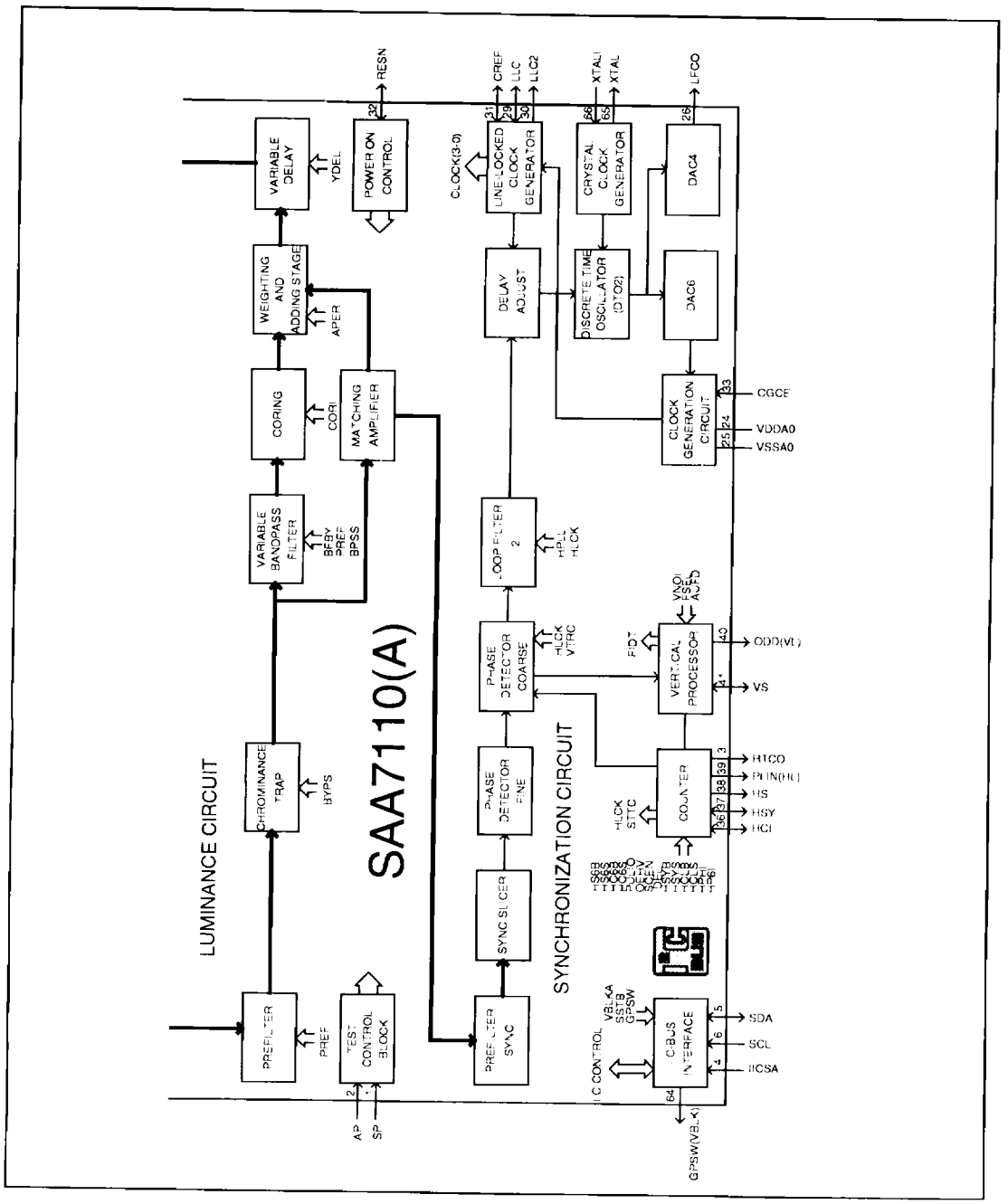


FIGURE 6. BLOCK PICTURE Luminance and Synchronization Part



5. CLAMP AND GAIN DESCRIPTION

CLAMPING

The coupling capacitance is used as clamp capacitance for each input. An internal digital clamp comparator generates the information about clamp-up or clamp-down. The clamping levels for the two A/D channels are adjustable over the 8-bit range (1 to 254). Clamping time in normal use is set with the HCL pulse at the back porch of the video signal. The clamping pulse HCL is user adjustable.

GAIN CONTROL

The luminance AGC can be used for every channel were luminance or CVBS is coming in. AGC active time is the sync tip of the video signal. The sync tip pulse HSY is user adjustable. The AGC can be switched off and the gain for the three main input channels can be adjusted independently. Signal (white) peak control limits the gain at signal overshoots. The flow charts on this page and on the next page show more details of the AGC. The influence of supply voltage variation within the specified range is automatically eliminated by clamp and automatic gain control.

FIGURE 7. AUTOMATIC GAIN CONTROL RANGE

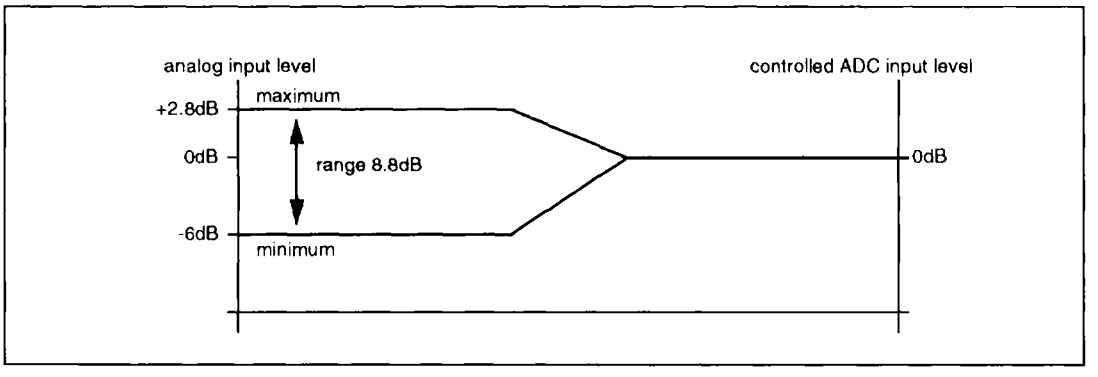


FIGURE 8. CLAMP AND GAIN FLOWCHART

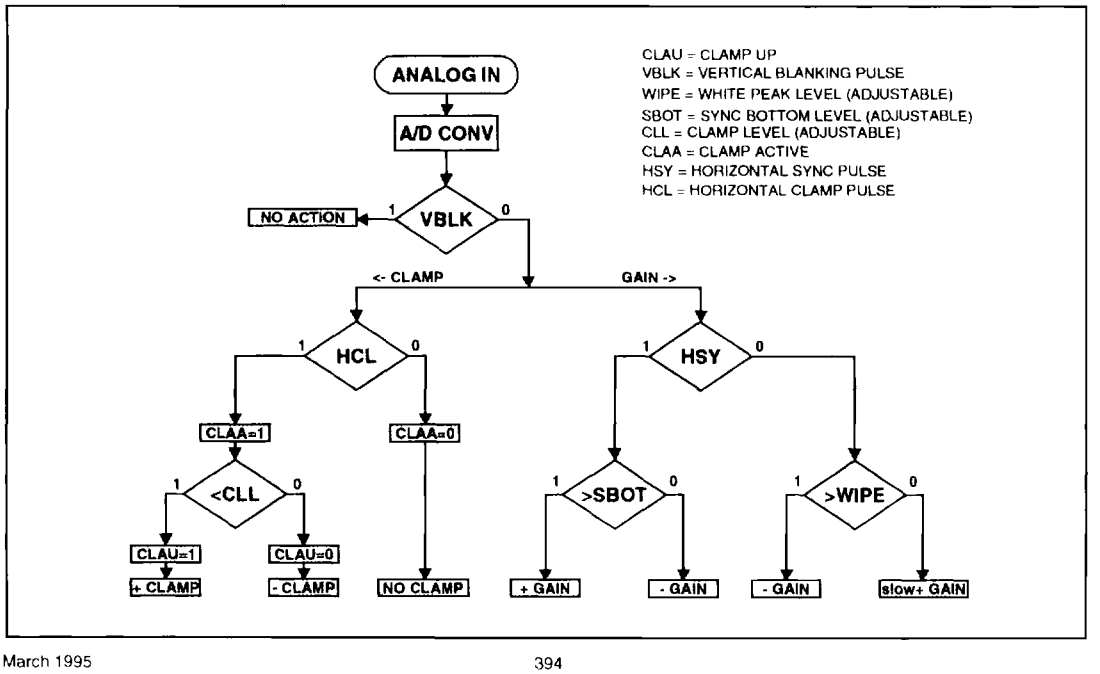
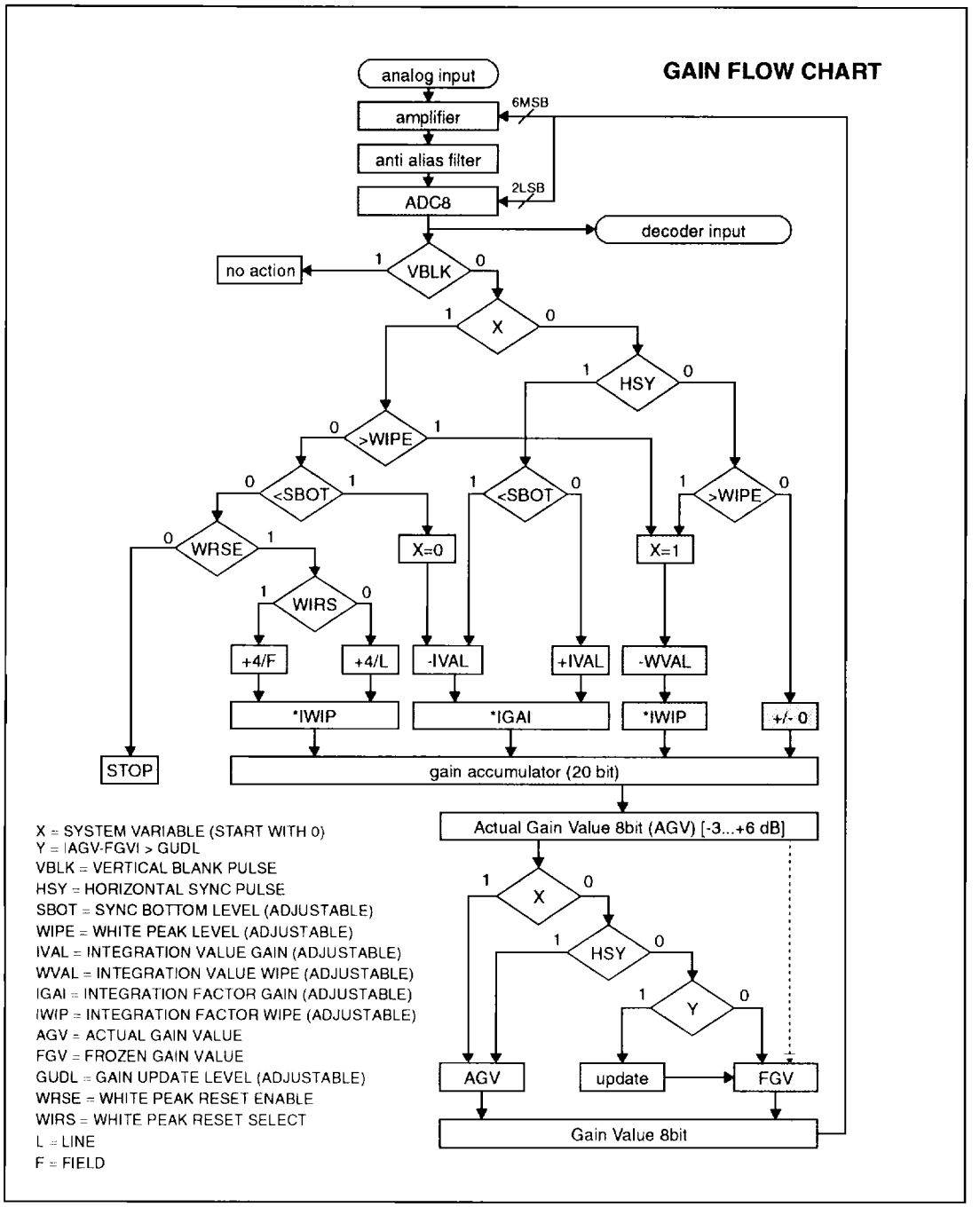


FIGURE 9. LUMINANCE AGC FLOWCHART



6. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all ground pins as well as all supply pins connected together.

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_{stg}	Storage temperature	-65	+150	°C
t_{amb}	Temperature under bias	-10	+80	°C
T_{amb}	Operating ambient temperature range	0	+70	°C
V_{DD}	Supply voltage digital	-0.5	+7.0	V
V_{DDA}	Supply voltage analog	-0.5	+7.0	V
V_I	Input voltage digital	-0.5	+7.0	V
V_I	Input voltage analog	-0.5	+7.0	V
$V_{diffGND}$	Difference voltage V_{SSAall} - V_{SSall}	-	100	mV
V_{ESD}	Electrostatic * handling for all pins	-	±2000	V
P_{tot}	total power dissipation	-	2.5	W
* Equivalent to discharging a 100pF capacitor through an 1.5kΩ series resistor				

TABLE 2. LIMITING VALUES

7. ELECTRICAL CHARACTERISTIC

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	LIMITS TYP	MAX	UNIT
Supply						
V_{DD1-5}	digital supply voltage range		4.5	5	5.5	V
I_{DD1-5}	digital total supply current		-	-	250	mA
$V_{DDA0,2-4}$	analog supply voltage range		4.75	5	5.25	V
$I_{DDA0,2-4}$	analog total supply current		-	-	150	mA
P_{tot}	total power dissipation		-	1.2	1.7	W
Analog part						
I_{clamp}	clamp current	V_i=1.25V_{DC}	-	±2	-	µA
$V_{i(pp)}$	input voltage (AC coupling necessary)	C_{coup}=10nF	0.5	1	1.38	V_{pp}
$\|Z_i\|$	input impedance	I_{clamp} off	200	-	-	kΩ
C_i	input capacitance		-	-	10	pF
a	channel crosstalk	f < 5MHz	-	-50	-	dB

TABLE 3. ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
ADCs						
B	analog bandwidth	-3dB	-	15	-	MHz
Φ_{diff}	differential phase (Amplifier and AAF=bypass)		-	2	-	deg
G_{diff}	differential gain (Amplifier and AAF=bypass)		-	2	-	%
f_{LLC}	clock rate ADC		11	-	16	MHz
DLE	DC differential linearity error		-	1/2	-	LSB
ILE	DC integral linearity error		-	1	-	LSB
Digital inputs						
$V_{IL.IIC}$	input voltage LOW	SDA and SCL	-0.5	-	1.5	V
$V_{IH.IIC}$	input voltage HIGH	SDA and SCL	3.0	-	V_{DD}+0.5	V
$V_{ILclocks}$	input voltage LOW	clocks	-0.5	-	0.6	V
$V_{IH.LLC}$	input voltage HIGH		2.4	-	V_{DD}+0.5	V
$V_{IH.XTALI}$	input voltage HIGH		3.0	-	VDD+0.5	V
V_{IL}	input voltage LOW	other inputs	-0.5	-	0.8	V
V_{IH}	input voltage HIGH	other inputs	2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current		-	-	10	µA
$C_{I.LLC}$	input capacitance	clocks	-	-	10	pF
C_I	input capacitance	other inputs	-	-	8	pF
$C_{I.IO}$	input capacitance	I/O at high impedance	-	-	8	pF
Digital outputs						
V_{LFCO}	output amplitude of LFCO (peak-to-peak value)	note 1	1.4	-	2.6	V
V_{OL}	output voltage LOW	note 2	0	-	0.6	V
V_{OH}	output voltage HIGH	note 2	2.4	-	V_{DD}	V
$V_{OLclocks}$	output voltage LOW	clocks	-0.5	-	0.6	V
$V_{OHclocks}$	output voltage HIGH	clocks	2.6	-	V_{DD}+0.5	V
Clock input timing (LLC)						
t_{LLC}	cycle time LLC		31	-	45	ns
δ	duty factor: t_{LLCH}/t_{LLC}		40	-	60	%
$t_{r.LLC}$	rise time	0.6V to 2.4V	-	-	5	ns
$t_{f.LLC}$	fall time	2.4V to 0.6V	-	-	5	ns
Control and CREF input timing (note 5)						
t_{SU}	input data set-up time		11	-	-	ns
$t_{HD.CREF}$	input data hold-time		3	-	-	ns

TABLE 3. ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
$t_{HD.FEIN}$	input data hold-time		3	-	-	ns
$t_{HD.other}$	input data hold-time	Note 5	6	-	-	ns
Data and control output timing (note 3)						
$C_{L.data}$	output load capacitance (data, HREF and VS)		15	-	50	pF
$C_{L.cont}$	output load capacitance (control)		7.5	-	25	pF
$t_{OH.data}$	output hold time	15 pF	13	-	-	ns
$t_{PD.data}$	propagation delay from negative edge of LLC (data, HREF and VS)	50 pF	-	-	29	ns
$t_{PD.cont}$	propagation delay from negative edge of LLC (control)	25 pF	-	-	29	ns
t_{PZ}	propagation delay from negative edge of LLC (to 3-state)	Note 4	-	-	15	ns
Clock output timing (LLC, LLC2)						
$C_{L.LLC}$	output load capacitance		15	-	40	pF
t_{LLC}	cycle time LLC		31.5	-	45	ns
t_{LLC2}	cycle time LLC2		63	-	90	ns
δ	duty factors: t_{LLCH}/t_{LLC} and t_{LLC2H}/t_{LLC2}		40	-	60	%
t_r	rise time LLC, LLC2	0.6V to 2.6V	-	-	5	ns
t_f	fall time LLC, LLC2	2.6V to 0.6V	-	-	5	ns
t_{dLLC2}	delay time LLC out to LLC2 out	at 1.5V, 40pF Note 6	-	-	8	ns
Data qualifier output timing (CREF)						
$t_{OH.CREF}$	output hold time	15 pF	4	-	-	ns
$t_{PD.CREF}$	propagation delay from positive edge of LLC	40 pF	-	-	20	ns
Horizontal PLL						
f_{Hn}	nominal line frequency	50 Hz field	-	15625	-	Hz
		60 Hz field	-	15734	-	Hz
Df_H/f_{Hn}	permissible static deviation	50 Hz field	-	-	5.6	%
		60 Hz field	-	-	6.7	%
Subcarrier PLL						
f_{Hn}	nominal subcarrier frequency	PAL	-	4433618	-	Hz
		NTSC	-	3579545	-	Hz
Df_H/f_{Hn}	lock in range		400	-	-	Hz

TABLE 3. ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Crystal oscillator						
f_n	nominal frequency	3rd harmonic	-	26.8	-	Mhz
Df/f_n	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistor R_S		-	50	80	Ω
	motional capacitance C_1		-	1.1 ±20%	-	fF
	parallel capacitance C_0		-	3.5 ±20%	-	pF
	Philips catalogue number:	9922 520 30004				

Notes to the characteristics:

1. The **LFCO** output level must be measured with a load circuit 10kΩ in parallel to 15pF.

2. The levels must be measured with load circuits, the loads used depend on the type of output stage. Control outputs (except HREF, VS); 1.2kΩ at 3V (TTL load), C_L=25pF: data outputs (and HREF, VS); 1.2kΩ at 3V (TTL load), C_L=50pF.

3. Data output signals are **YUV(15-0)**.
Control output signals are **HREF, VS, HS, HSY, HCL, RTCO, PLIN(HL), ODD(VL), GPSW0(VBLK).**
Effects of rise and fall times are included in the calculation of t_{OH}, t_{PD} and t_{PZ}. Timings and levels refer to drawings and conditions shown in Fig.8 on next page.

4. The minimum propagation delay from 3-state to data active related to falling edge of LLC is 0ns.

5. Other control input signals are **CGCE, VS, IICSA, HCL, HSY.**

6. LLC2 out is not active while CGCE=0

* Values to be fixed

TABLE 3. ELECTRICAL CHARACTERISTICS

8. TIMINGS

FIGURE 10. CLOCK/DATA TIMING

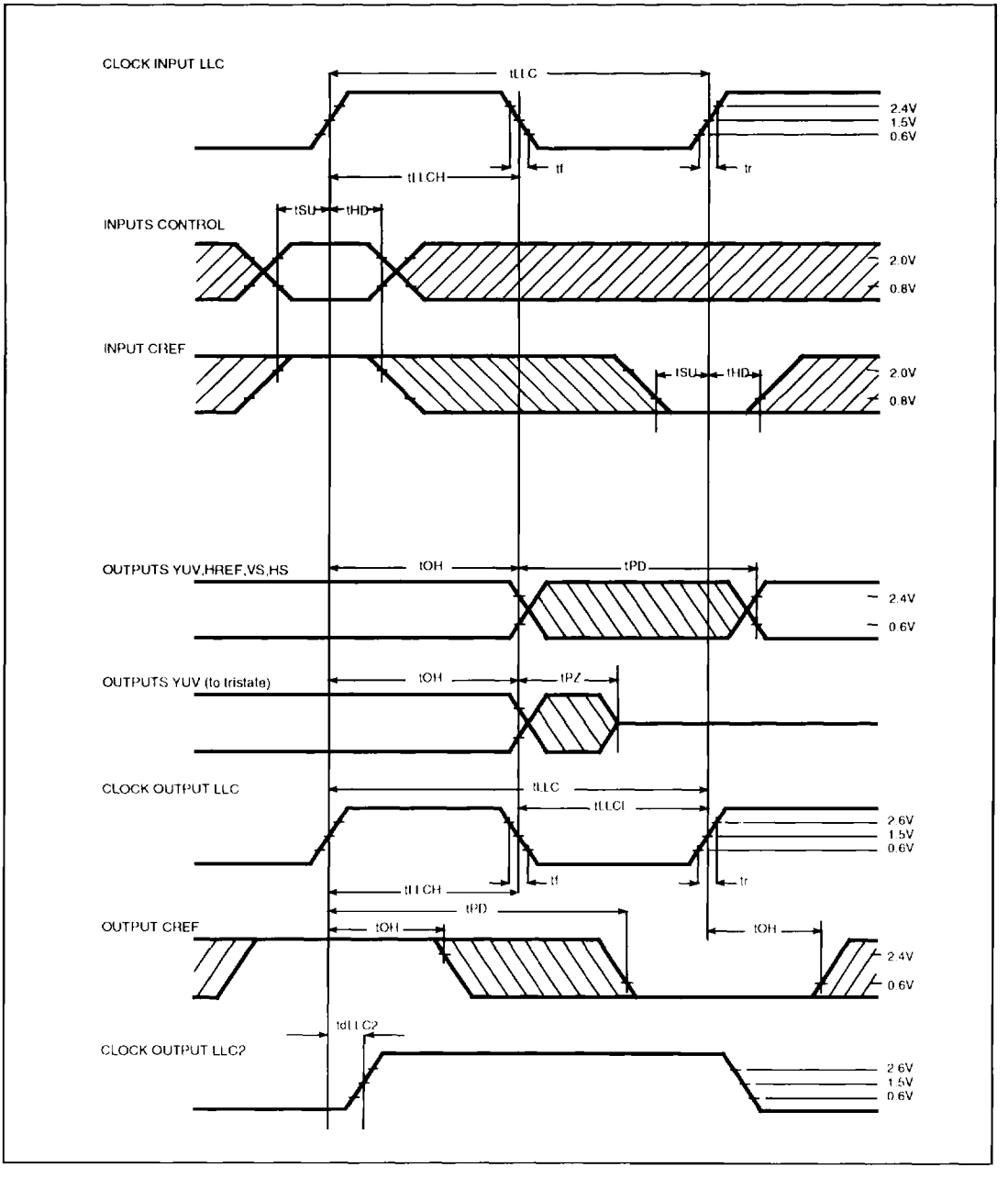


FIGURE 11. HORIZONTAL TIMING

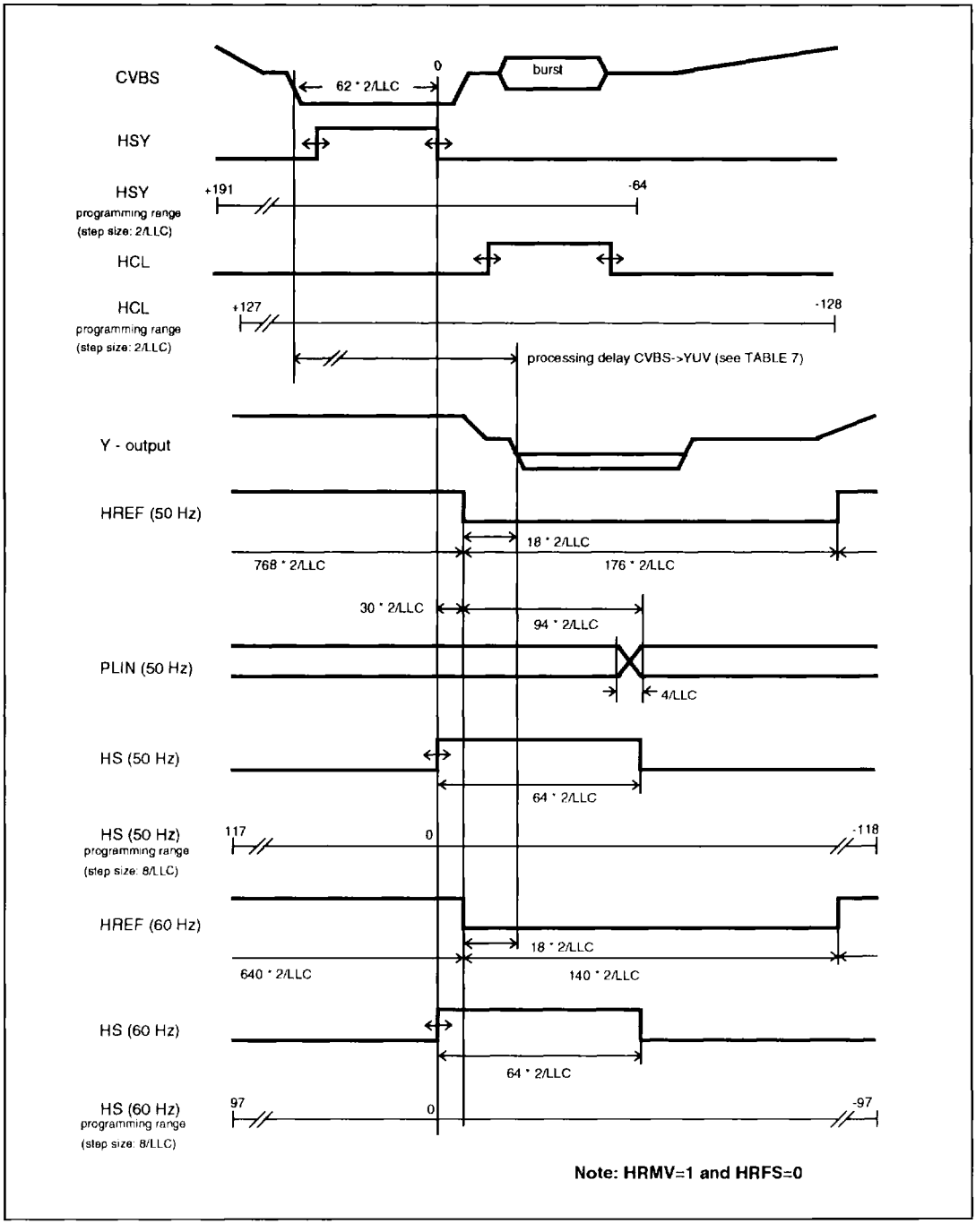


FIGURE 12. HREF TIMING

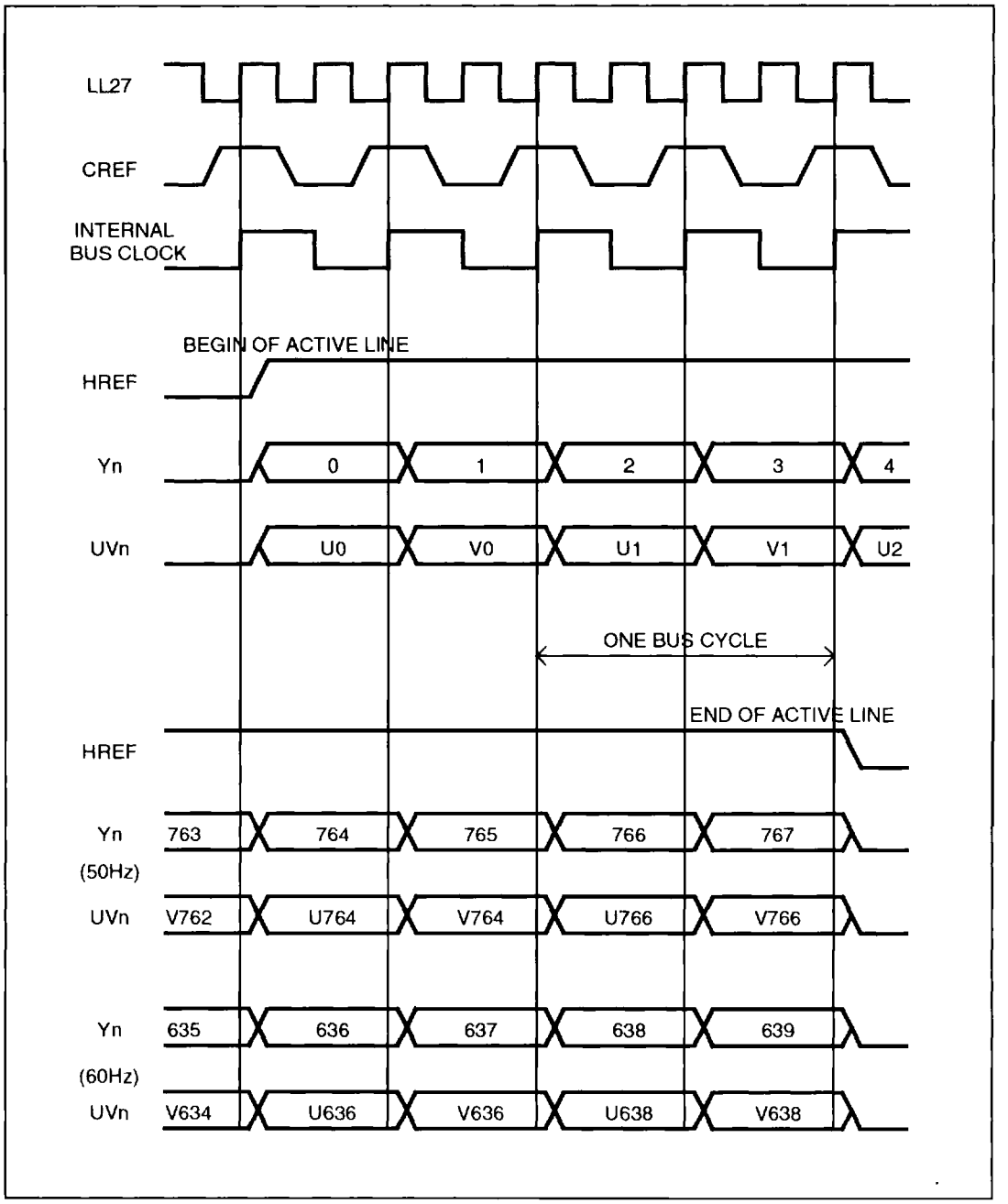
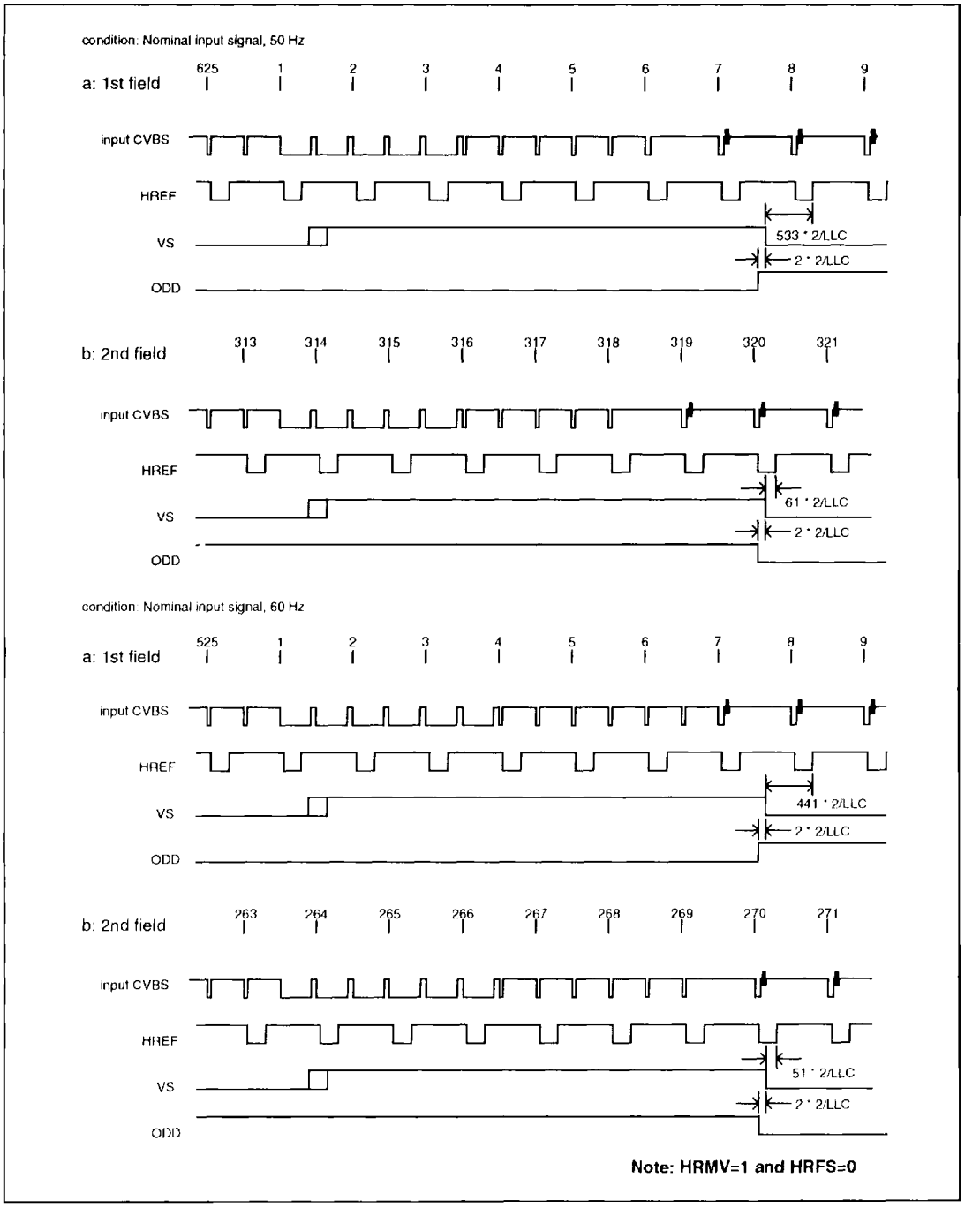
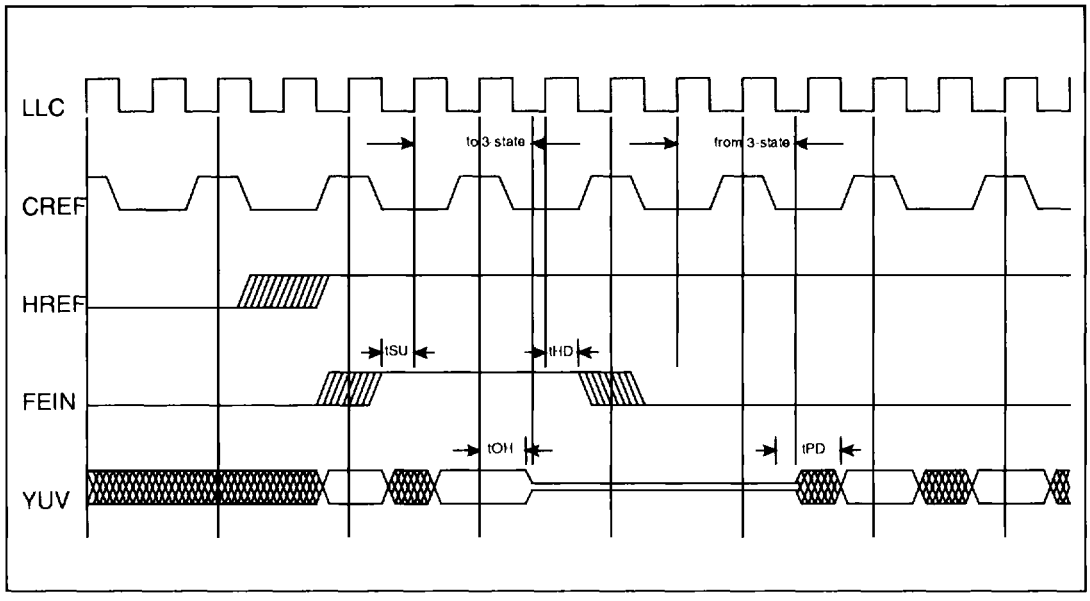


FIGURE 13. VERTICAL TIMING



9. DIGITAL OUTPUT CONTROL

FIGURE 14. FEIN TIMING

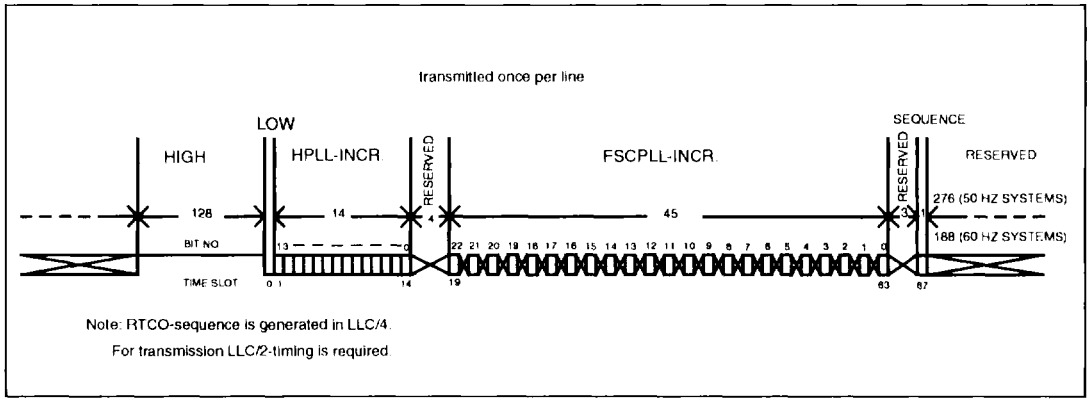


OEYC	FEIN	YUV(15:0)
0	0	Z
1	0	active
X	1	Z

TABLE 4. DIGITAL OUTPUT CONTROL

10. REALTIME CONTROL OUTPUT

FIGURE 15. REAL TIME CONTROL OUTPUT



11. OUTPUT FORMATS

BUS SIGNAL	Pixel Byte Sequence							
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV3	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV0	0	0	0	0	0	0	0	0
Y FRAME	0	1	2	3	4	5	6	7
UV FRAME	0				4			
Note:								
	Data rate				Sample frequency			
Y	LLC2				LLC2			
U					LLC4			
V					LLC4			

TABLE 5. 4:1:1 FORMAT

BUS SIGNAL	Pixel Byte Sequence					
Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	U7	V7	U7	V7	U7	V7
UV6	U6	V6	U6	V6	U6	V6
UV5	U5	V5	U5	V5	U5	V5
UV4	U4	V4	U4	V4	U4	V4
UV3	U3	V3	U3	V3	U3	V3
UV2	U2	V2	U2	V2	U2	V2
UV1	U1	V1	U1	V1	U1	V1
UV0	U0	V0	U0	V0	U0	V0
Y FRAME	0	1	2	3	4	5
UV FRAME	0		2		4	
Note:						
	Data rate		Sample frequency			
Y	LLC2		LLC2			
U			LLC8			
V			LLC8			

TABLE 6. 4:2:2 FORMAT

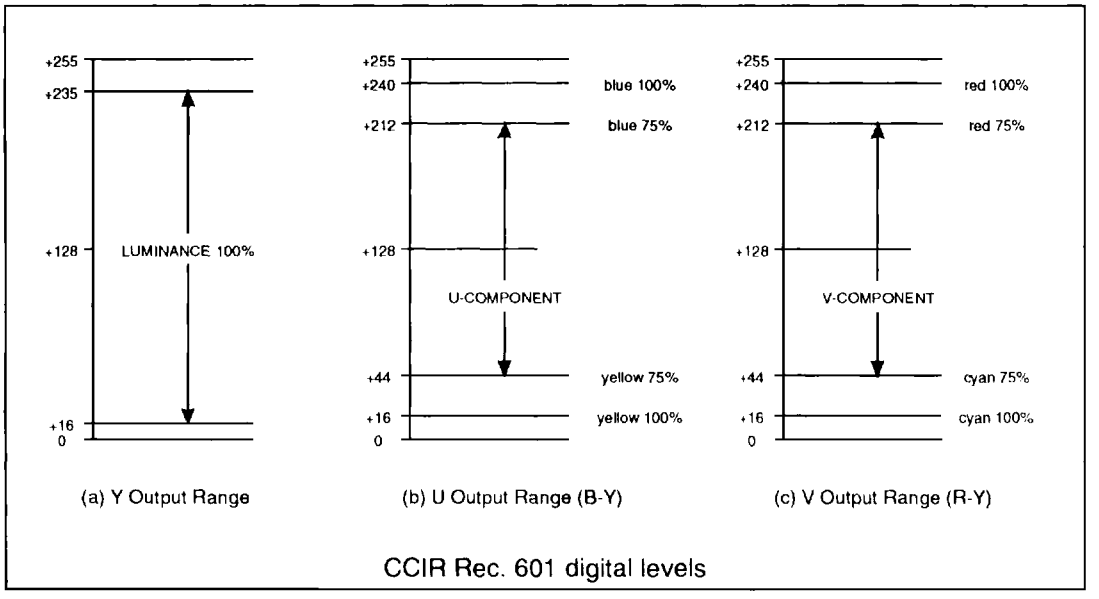
12. PROCESSING DELAY

TABLE 7. PROCESSING DELAY (CVBSIN - YUVOUT)

FUNCTION	ANALOG DELAY (typical) AIN21 -> ADCIN(AOUT) (ns)	DIGITAL DELAY ADCIN(AOUT) -> YUVOUT (1/LLC) [YDEL=0, CAD2/3=1]
without AMP + AAF	10	248
with AMP, without AAF	30	
with AMP + AAF (50Hz)	30+40	
with AMP + AAF (60Hz)	30+50	

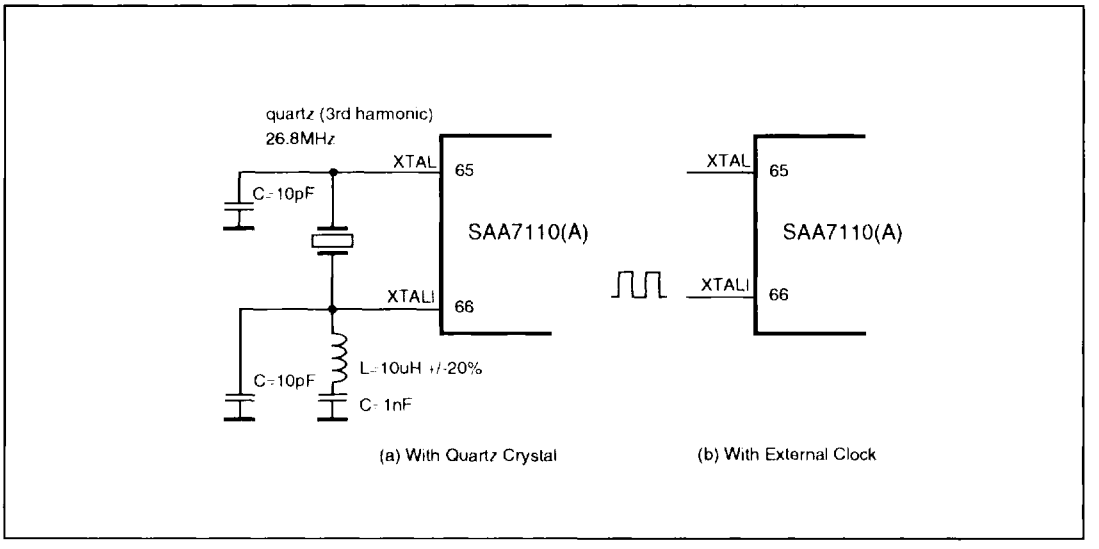
13. YUV OUTPUT SIGNAL RANGE

FIGURE 16. YUV OUTPUT SIGNAL RANGE



14. OSCILLATOR APPLICATION

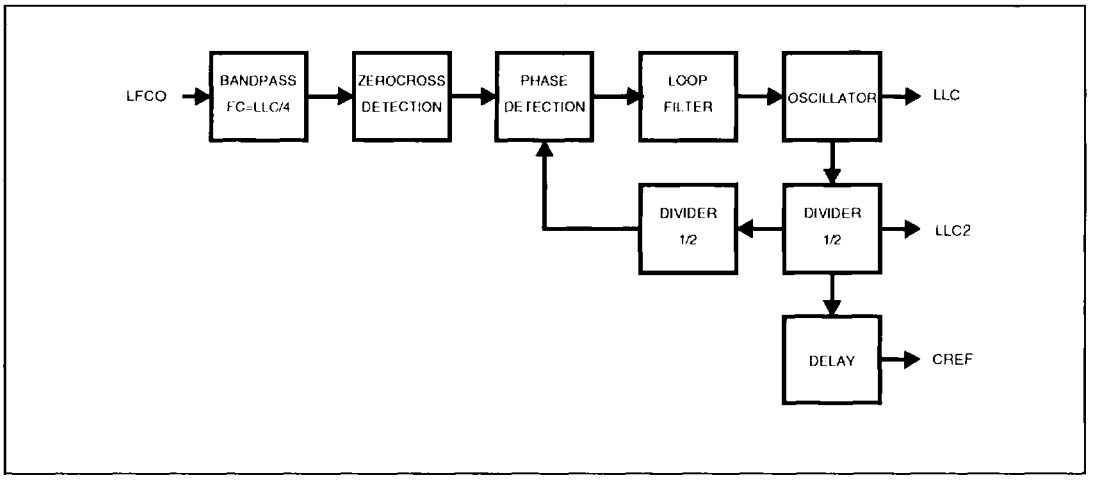
FIGURE 17. OSCILLATOR APPLICATION



15. CLOCK GENERATION CIRCUIT

The internal CGC generates the system clock LLC, LLC2 and the clock reference signal CREF. The internal generated LFCO (triangular waveform) is multiplied by four via the analog PLL (including phase detector, loop filter, VCO and frequency divider). The rectangular output signals have 50% duty factor.

FIGURE 18. CLOCK GENERATION CIRCUIT



16. CLOCK FREQUENCIES

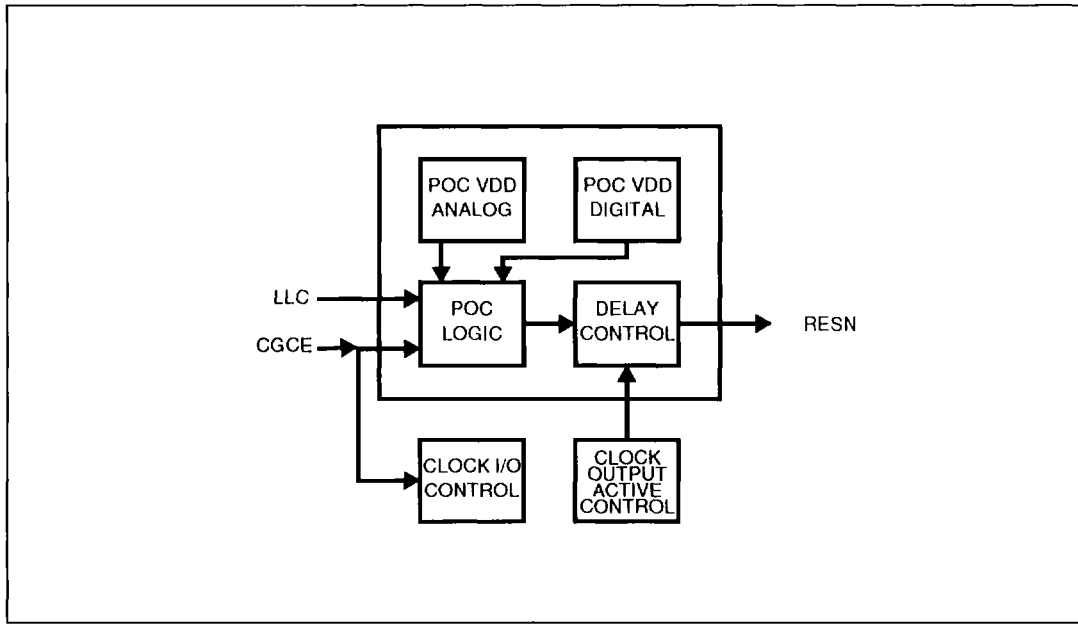
CLOCK	50Hz	60Hz
XTAL	26.8	
LLC	29.5	24.545454
LLC2	14.75	12.272727
LLC4	7.375	6.136136
LLC8	3.6875	3.068181

TABLE 8. SYSTEM CLOCK FREQUENCIES (MHZ)

17. POWER-ON CONTROL

Power-on reset is activated at power-on (only using internal CGC) and if the supply voltage decreases below 3.5 V. The RESN signal can be applied to reset other circuits of the digital TV system.

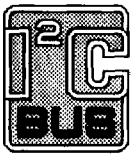
FIGURE 19. POWER-ON CONTROL



INTERNAL POWER ON CONTROL SEQUENCE	PIN OUTPUT STATUS	FUNCTION
DIRECTLY AFTER POWER ON ASYN-CHRONOUS RESET	Y(7:0), UV(7:0), RTCO, PLIN, ODD, GPSW, SDA, HREF, HS, VS, HCL, HSY --> high impedance state LLC, LLC2, CREF --> HIGH state	direct switching to high impedance (outputs) or input mode (I/Os) for 20 - 200ms
START SYNCHRO-NOUS IIC RESET SEQUENCE	LLC, LLC2, CREF became active	**starting IIC reset sequence**
STATUS after IIC RESET	Y(7:0), UV(7:0), HREF, HS --> held in high impedance state VS, HCL, HSY --> held in input function mode	**SA0Dh=7D**h (VTRC=0, RTSE=1, HRMV=1, SSTB=0, SECS=1), **SA0Eh=00**h (HPLL=0, OEHV=0, OEYC=0, CHRS=0, GPSW1=0), **SA31h=00**h (AOSL(1:0)=00, WIRS=0, WRSE=0, SQPB=0, VBLKA=0, PULIO=0)
STATUS after POWER ON CONTROL SEQUENCE	RTCO, PLIN, ODD, GPSW, SDA active	**After power on (reset sequence) a complete IIC transmission is required!**

TABLE 9. POWER-ON CONTROL SEQUENCE

18. IIC DESCRIPTION



19. IIC-BUS FORMAT

S	SLAVEADDRESS	A	SUBADDRESS	A	DATA (n bytes)*	A	P

S	start condition
SLAVEADDRESS	**1001 110X**b (IICSA=LOW) or **1001 111X**b (IICSA=HIGH)
A	acknowledge, generated by the slave
SUBADDRESS	subaddress byte, see reference table
DATA	data byte, see reference table
P	stop condition
X	read/write control bit X=0, order to write (the circuit is slave receiver) X=1, order to read (the circuit is slave transmitter)
SLAVEADDRESS	9Ch for write (IICSA=0) 9Dh for read (IICSA=0) 9Eh for write (IICSA=1) 9Fh for read (IICSA=1)
SUBADRESSES	00 h - 19h Decoder part 1Ah - 1Fh reserved 20h - 34h Frontend part
* If more than one byte DATA are transmitted, then auto-increment of the subadress is performed.	

TABLE 10. IIC FORMAT

19.1 IIC-BUS RECEIVER-TRANSMITTER OVERVIEW TABLE

OCF1-Receiver	Slave-Addresses 10011100b, 9Ch [IICSA=0] 10011110b, 9Eh [IICSA=1]

DMSD-SQP+BCS SLAVE RECEIVER (SU 00h-19h)

REGISTER FUNCTION	SUB ADDR	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Increment delay	00	007 IDEL7	006 IDEL6	005 IDEL5	004 IDEL4	003 IDEL3	002 IDEL2	001 IDEL1	000 IDEL0
Horizontal sync HSY begin 50 Hz	01	015 HSYB7	014 HSYB6	013 HSYB5	012 HSYB4	011 HSYB3	010 HSYB2	009 HSYB1	008 HSYB0
Horizontal sync HSY stop 50 Hz	02	023 HSYS7	022 HSYS6	021 HSYS5	020 HSYS4	019 HSYS3	018 HSYS2	017 HSYS1	016 HSYS0
Horizontal clamp HCL begin 50 Hz	03	031 HCLB7	030 HCLB6	029 HCLB5	028 HCLB4	027 HCLB3	026 HCLB2	025 HCLB1	024 HCLB0
Horizontal clamp HCL stop 50 Hz	04	039 HCLS7	038 HCLS6	037 HCLS5	036 HCLS4	035 HCLS3	034 HCLS2	033 HCLS1	032 HCLS0
Horizontal sync after PHI1 50 Hz	05	047 HPHI7	046 HPHI6	045 HPHI5	044 HPHI4	043 HPHI3	042 HPHI2	041 HPHI1	040 HPHI0
Luminance control	06	055 BYPS	054 PREF	053 BPSS1	052 BPSS0	051 CORI1	050 CORI0	049 APER1	048 APER0
Hue control	07	063 HUEC7	062 HUEC6	061 HUEC5	060 HUEC4	059 HUEC3	058 HUEC2	057 HUEC1	056 HUEC0
Color Killer Threshold QUAM	08	071 CKTQ4	070 CKTQ3	069 CKTQ2	068 CKTQ1	067 CKTQ0	066 XXX	065 XXX	064 XXX
Color Killer Thresh. SECAM	09	079 CKTS4	078 CKTS3	077 CKTS2	076 CKTS1	075 CKTS0	074 XXX	073 XXX	072 XXX
Sensitivity PAL switch	0A	087 PLSE7	086 PLSE6	085 PLSE5	084 PLSE4	083 PLSE3	082 PLSE2	081 PLSE1	080 PLSE0
Sensitivity SECAM switch	0B	095 SESE7	094 SESE6	093 SESE5	092 SESE4	091 SESE3	090 SESE2	089 SESE1	088 SESE0
Gain Control Chrominance	0C	103 COLO	102 LFIS1	101 LFIS0	100 XXX	099 XXX	098 XXX	097 XXX	096 XXX
Standard/mode control	0D*	111 VTRC	110 XXX	109 XXX	108 XXX	107 RTSE	106 HRMV	105 SSTB	104 SECS
I/O and clock control	0E*	119 HPLL	118 XXX	117 XXX	116 OEHV	115 OEYC	114 CHRS	113 XXX	112 GPSW
Control #1	0F	127 AUFD	126 FSEL	125 SXCR	124 SCEN	123 XXX	122 YDEL2	121 YDEL1	120 YDEL0
Control #2	10	135 XXX	134 XXX	133 XXX	132 XXX	131 XXX	130 HRFS	129 VNOI1	128 VNOI0
Chroma gain reference	11	143 CHCV7	142 CHCV6	141 CHCV5	140 CHCV4	139 CHCV3	138 CHCV2	137 CHCV1	136 CHCV0
Chroma saturation	12	151 XXX	150 SATN6	149 SATN5	148 SATN4	147 SATN3	146 SATN2	145 SATN1	144 SATN0
Luminance contrast	13	159 XXX	158 CONT6	157 CONT5	156 CONT4	155 CONT3	154 CONT2	153 CONT1	152 CONT0
Horizontal sync HSY begin 60 Hz	14	167 HS6B7	166 HS6B6	165 HS6B5	164 HS6B4	163 HS6B3	162 HS6B2	161 HS6B1	160 HS6B0
Horizontal sync HSY stop 60 Hz	15	175 HS6S7	174 HS6S6	173 HS6S5	172 HS6S4	171 HS6S3	170 HS6S2	169 HS6S1	168 HS6S0
Horizontal clamp HCL begin 60 Hz	16	183 HC6B7	182 HC6B6	181 HC6B5	180 HC6B4	179 HC6B3	178 HC6B2	177 HC6B1	176 HC6B0

TABLE 11. IIC OCF1

Horizontal clamp HCL stop 60 Hz	17	191 HC6S7	190 HC6S6	189 HC6S5	188 HC6S4	187 HC6S3	186 HC6S2	185 HC6S1	184 HC6S0
Horizontal sync after PHI1 60 Hz	18	199 HP6I7	198 HP6I6	197 HP6I5	196 HP6I4	195 HP6I3	194 HP6I2	193 HP6I1	192 HP6I0
Luminance bright-ness	19	207 BRIG7	206 BRIG6	205 BRIG5	204 BRIG4	203 BRIG3	202 BRIG2	201 BRIG1	200 BRIG0

DUAD SLAVE RECEIVER (SU 20h-32h)

REGISTER FUNCTION	SUB ADDR	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Analog Con-trol #1	20	007 AIND4	006 AIND3	005 AIND2	004 FUSE1	003 FUSE0	002 AINS4	001 AINS3	000 AINS2
Analog Con-trol #2	21	015 VBCO	014 MS34	013 MX241	012 MX240	011 MS24	010 REFS4	009 REFS3	008 REFS2
Mix Control #1	22	023 GACO1	022 GACO0	021 CSEL	020 YSEL	019 MUYC	018 CLTS	017 MX341	016 MX340
Clamp level Control 21	23	031 CLL217	030 CLL216	029 CLL215	028 CLL214	027 CLL213	026 CLL212	025 CLL211	024 CLL210
Clamp level Control 22	24	039 CLL227	038 CLL226	037 CLL225	036 CLL224	035 CLL223	034 CLL222	033 CLL221	032 CLL220
Clamp level Control 31	25	047 CLL317	046 CLL316	045 CLL315	044 CLL314	043 CLL313	042 CLL312	041 CLL311	040 CLL310
Clamp level Control 32	26	055 CLL327	054 CLL326	053 CLL325	052 CLL324	051 CLL323	050 CLL322	049 CLL321	048 CLL320
Gain Control Analog #1	27	063 HOLD	062 GASL	061 GAI25	060 GAI24	059 GAI23	058 GAI22	057 GAI21	056 GAI20
White Peak Control	28	071 WIPE7	070 WIPE6	069 WIPE5	068 WIPE4	067 WIPE3	066 WIPE2	065 WIPE1	064 WIPE0
Sync bottom Control	29	079 SBOT7	078 SBOT6	077 SBOT5	076 SBOT4	075 SBOT3	074 SBOT2	073 SBOT1	072 SBOT0
Gain Control Analog #2	2A	087 IWIP1	086 IWIP0	085 GAI35	084 GAI34	083 GAI33	082 GAI32	081 GAI31	080 GAI30
Gain Control Analog #3	2B	095 IGAI1	094 IGAI0	093 GAI45	092 GAI44	091 GAI43	090 GAI42	089 GAI41	088 GAI40
MIX Control #2	2C	103 CLS4	102 XXX	101 CLS3	100 CLS2	099 XXX	098 XXX	097 TWO3	096 TWO2
Integration value gain	2D	111 IVAL7	110 IVAL6	109 IVAL5	108 IVAL4	107 IVAL3	106 IVAL2	105 IVAL1	104 IVAL0
Blank pulse V SET	2E	119 VBPS7	118 VBPS6	117 VBPS5	116 VBPS4	115 VBPS3	114 VBPS2	113 VBPS1	112 VBPS0
Blank pulse V RESET	2F	127 VBPR7	126 VBPR6	125 VBPR5	124 VBPR4	123 VBPR3	122 VBPR2	121 VBPR1	120 VBPR0
ADCs Gain Control	30	135 XXX	134 WISL	133 GAS3	132 GAD31	131 GAD30	130 GAS2	129 GAD21	128 GAD20
MIX Control #3	31*	143 AOSL1	142 AOSL0	141 WIRS	140 WRSE	139 SQPB	138 AFCCS*	137 VBLKA	136 PULIO
Integration-value white peak	32	151 WVAL7	150 WVAL6	149 WVAL5	148 WVAL4	147 WVAL3	146 WVAL2	145 WVAL1	144 WVAL0
MIX Control #4	33	159 OFTS	158 XXX	157 CHSB	156 XXX	155 CAD3	154 CAD2	153 XXX	152 XXX

TABLE 11. IIC OCF1

Gain Update Level	34	167 MUD2	166 MUD1	165 GUDL5	164 GUDL4	163 GUDL3	162 GUDL2	161 GUDL1	160 GUDL0

Subadresses to be reset --> 0D to 7Dh, 0E and 31 to 00h after RESN=0 (CGCE=0) or POWER ON (CGCE=1)
Note: All reserved XXX-bits must be set to LOW, XX-bit: don't care
*AFCCS: don't care in SAA7110A (Due to improved anti alias filter function)

OCF1-Transmitter	**Slave-Addresses 10011101b, 9Dh [IICSA=0] 10011111b, 9Fh [IICSA=1]**

BYTE NO. 0 (transmitted if SSTB = 0 or after RESN has been 0)

VERSION STATUS BYTE	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID(7:0)	Indicates the version number of the IC e.g.: SAA7110A V1 = 01h

BYTE NO. 1 (transmitted if SSTB = 1)

STATUS BYTE FUNCTION	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	STTC	HLCK	FIDT	GLIM	XXX	WIPA	ALTD	CODE

STTC	Status Bit for horizontal time constant. Status LOW: TV-time constant, HIGH: VCR-time-constant
HLCK	Status Bit for locked horizontal frequency. Status LOW: locked, HIGH: unlocked
FIDT	Identification Bit for detected field frequency. Status LOW: 50 Hz, HIGH: 60 Hz
GLIM	Gain value for active luminance channel is limited (max or min), active HIGH
XXX	reserved
WIPA	White peak loop is activated, active HIGH
ALTD	Status HIGH: Line-alternating color burst has been detected (PAL or SECAM)
CODE	Status HIGH: Any color signal has been detected

TABLE 11. IIC OCF1

IIC-RECEIVER (SLAVE-ADDRESS 9Ch / 9Eh)

DMSD-SQP SLAVE RECEIVER (SU 00h-19h)

Subaddress 00 Increment delay IDEL **007-000**

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/LLC)	CONTROL BITS*							
		IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
-1...	-4	1	1	1	1	1	1	1	1
... -195	-780 (max. value for 60 Hz systems)	0	0	1	1	1	1	0	1
... -236	-944 (max. value for 50 Hz systems)	0	0	0	1	0	1	0	0
... -256	-1024 (outside central counter)**	0	0	0	0	0	0	0	0

Where:

* A sign bit, designated A08 and internally set to HIGH, indicates values are always negative.
** The horizontal PLL does not operate in this condition. The system clock frequency is set to a value fixed by the last update and is within +/-7.1% of the nominal frequency.

Subaddress 01 Horizontal sync begin 50 Hz HSYB **015-008**

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
+191...	-382	1	0	1	1	1	1	1	1
... -64	+128	1	1	0	0	0	0	0	0

Subaddress 02 Horizontal sync stop 50 Hz HSYS **023-016**

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
+191...	-382	1	0	1	1	1	1	1	1
... -64	+128	1	1	0	0	0	0	0	0

Subaddress 03 Horizontal clamp begin 50 Hz HCLB **031-024**

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
+127...	-254	0	1	1	1	1	1	1	1
... -128	+256	1	0	0	0	0	0	0	0

Subaddress 04 Horizontal clamp stop 50 Hz HCLS **039-032**

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
+127...	-254	0	1	1	1	1	1	1	1
... -128	+256	1	0	0	0	0	0	0	0

TABLE 12. IIC DETAIL SU00h-04h(000-039)

Subaddress 05 Horizontal sync start after PHI1 50 Hz HPHI									047-040
DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 8/LLC	CONTROL BITS							
		HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
+127...	Forbidden; outside available central counter range	0	1	1	1	1	1	1	1
... +118	Forbidden; outside available central counter range	0	1	1	1	0	1	1	0
+117...	-32 µs (max. negative value)	0	1	1	1	0	1	0	1
... -118	+31.7 µs (max. positive value)	1	0	0	0	1	0	1	0
-119...	Forbidden; outside available central counter range	1	0	0	0	1	0	0	1
... -128	Forbidden; outside available central counter range	1	0	0	0	0	0	0	0

Subaddress 06 Luminance control		055-048
Aperture factor APER		049-048
APERTURE FACTOR	CONTROL BITS	
	APER1	APER0
0 0	0	0
1 0.25	0	1
2 0.5	1	0
3 1	1	1
Corner correction CORI		050
CORING +/- LSBS IN 8 BIT	CONTROL BITS CORI	
0 0 (OFF)	0	0
1 1	0	1
2 2	1	0
3 3	1	1
Aperture bandpass (center frequency) BPSS		053-052

BANDPASS CENTER FREQ.		CONTROL BITS	
50 Hz	60 Hz	BPSS1	BPSS0
4.6 MHz	3.8 Mhz	0	0
4.3 MHz	3.4 MHz	0	1
3.0 MHz	2.5 MHz	1	0
3.2 MHz	2.7 MHz	1	1

TABLE 13. II DETAIL SU05h-06h(040-055)

Prefilter active PREF		054
PREFILTER		**CONTROL BIT PREF**
Bypassed		0
Active		1
Chrominance trap bypass BYPS		055
CHROMA TRAP	**MODE**	**CONTOL BIT BYPS**
Active	CVBS	0
Bypassed	S-Video	1

TABLE 13. II DETAIL SU05h-06h(040-055)

Subaddress 07 Hue phase control HUEC								**063-056**
HUE PHASE (DEG)	**CONTROL BITS**							
	HUEC7	**HUEC6**	**HUEC5**	**HUEC4**	**HUEC3**	**HUEC2**	**HUEC1**	**HUEC0**
+178.6...	0	1	1	1	1	1	1	1
... 0...	0	0	0	0	0	0	0	0
... -180	1	0	0	0	0	0	0	0

Subaddress 08 Control number 1					**071-064**
Color killer threshold QAM (PAL/NTSC) CKTQ					071-067
THRESHOLD (reference is nominal burst amplitude = 0 dB)	**CONTROL BITS**				
	CKTQ4	**CKTQ3**	**CKTQ2**	**CKTQ1**	**CKTQ0**
-30 dB...	1	1	1	1	1
... -24 dB...	1	0	0	0	0
... -18 dB	0	0	0	0	0

Subaddress 09 Control number 2					**079-072**
Color killer threshold SECAM CKTS					079-075
THRESHOLD (reference is nominal burst amplitude = 0 dB)	**CONTROL BITS**				
	CKTS4	**CKTS3**	**CKTS2**	**CKTS1**	**CKTS0**
-30 dB...	1	1	1	1	1
... -24 dB...	1	0	0	0	0
... -18 dB	0	0	0	0	0

Subaddress 0A PAL switch sensitivity PLSE								**087-080**
SENSITIVITY	**CONTROL BITS**							
	PLSE7	**PLSE6**	**PLSE5**	**PLSE4**	**PLSE3**	**PLSE2**	**PLSE1**	**PLSE0**
LOW	1	1	1	1	1	1	1	1
MEDIUM	1	0	0	0	0	0	0	0
HIGH	0	0	0	0	0	0	0	0

TABLE 14. II DETAIL SU07h-0Bh(056-095)

Subaddress 0B SECAM switch sensitivity SESE								095-088
SENSITIVITY	CONTROL BITS							
	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
LOW	1	1	1	1	1	1	1	1
MEDIUM	1	0	0	0	0	0	0	0
HIGH	0	0	0	0	0	0	0	0
Sensitivity HIGH means immediate sequence correction								

TABLE 14. II DETAIL SU07h-0Bh(056-095)

Subaddress 0C Gain control chrominance		103-096
AGC (Automatic Gain Control) - loop filter LFIS		102-101
AGC - LOOP FILTER TIME CONSTANT	CONTROL BITS	
	LFIS1	LFIS0
Slow	0	0
Medium	0	1
Fast	1	0
Actual chroma gain 'frozen'	1	1
Color on COLO		103
COLOUR ON	CONTROL BIT COLO	
Automatic color killer	0	
Color forced on	1	
Subaddress 0D Standard/mode control		**111-104**
SECAM mode bit SECS		104
FUNCTION	CONTROL BIT SECS	
other standards	0	
SECAM	1	
Status Byte select SSTB		105
FUNCTION	CONTROL BIT SSTB	
Statusbyte is Byte 0 (see Transmitter)	0	
Statusbyte is Byte 1 (see Transmitter)	1	
HREF-POSITION select HRMV		106
FUNCTION	CONTROL BIT HRMV	
HREF position like SAA7191 (8 LLC2 later)	0	
HREF normal position	1	

TABLE 15. IIC DETAIL SU0Ch-0Eh(096-119)

Real-time-outputs-mode select RTSE	107
FUNCTION	**CONTROL BIT RTSE**
PLIN switched to output pin 39 ODD switched to output pin 40	0
HL switched to output pin 39 VL switched to output pin 40	1
TV/VCR-mode select VTRC	111
FUNCTION	**CONTROL BIT VTRC**
TV mode	0
VTR mode	1
Subaddress 0E I/O and clock control	**119-112**
General purpose switch GPSW	112
FUNCTION	**CONTROL BIT GPSW**
switches directly pin 64 GPSW (application dependent) [VBLKA = 0]	0
	1

TABLE 15. IIC DETAIL SU0Ch-0Eh(096-119)

Select chrominance input CHRS	114
FUNCTION	**CONTROL BIT CHRS**
controlled by BYPS (subadress 06) normal position	0
digital chroma input switched to second input channel (see page 49, figure 20)	1
Output enable YUV-data OEYC	115
FUNCTION	**CONTROL BIT OEYC**
YUV-bus high impedance/input	0
Output YUV-bus active	1
Output enable horizontal/vertical sync OEHV	116
FUNCTION	**CONTROL BIT OEHV**
HS, HREF and VS high impedance/inputs	0
Output HS, HREF and VS active	1
Horizontal PLL clock HPLL	119
FUNCTION	**CONTROL BIT HPLL**
PLL closed	0
PLL open, horizontal frequency fixed	1

TABLE 16. IIC DETAIL SU0Eh-0Fh(114-127)

Subaddress 0F Control number 1				**127-120**
Luminance delay compensation YDEL				122-120
LUMINANCE DELAY COMPENSATION (steps in 2/LLC)	**CONTROL BITS**			
	YDEL2	**YDEL1**	**YDEL0**	
0	0	0	0	
3	0	1	1	
-4	1	0	0	
Enable or disable of sync and clamp pulses (HSY, HCL) SCEN				124
FUNCTION	**CONTROL BIT SCEN**			
Disable sync and clamp (set to HIGH)	0			
Enable sync and clamp	1			
SECAM cross color reduction SXCR				125
FUNCTION	**CONTROL BIT SXCR**			
Reduction OFF	0			
Reduction ON	1			
Field selection FSEL				126
FUNCTION	**CONTROL BIT FSEL**			
50 Hz, 625 lines	0			
60 Hz, 525 lines	1			
Automatic field detection AUFD				127
FUNCTION	**CONTROL BIT AUFD**			
Field state direct controlled via FSEL	0			
Automatic field detection	1			

TABLE 16. IIC DETAIL SU0Eh-0Fh(114-127)

Subaddress 10 Control number 2			**135-128**
Vertical noise reduction VNOI			129-128
FUNCTION	**CONTROL BITS**		
	VNOI1	**VNOI0**	
Normal mode	0	0	
Searching mode	0	1	
Free running mode	1	0	
Vertical noise reduction bypassed	1	1	
HREF select HRFS			130
FUNCTION	**CONTROL BIT HRFS**		
HREF matched to YUV output	0		
HREF matched to CVBS input	1		

TABLE 17. IIC DETAIL SU10h-13h(128-158)

Subaddress 11 Chrominance gain reference value CHCV								143-136
REFERENCE VALUE	CONTROL BITS							
	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
Maximum	1	1	1	1	1	1	1	1
CCIR-level for PAL	0	1	0	1	1	0	0	1
CCIR-level for NTSC	0	0	1	0	1	1	0	0
Minimum	0	0	0	0	0	0	0	0

Subaddress 12 Chrominance Saturation Control								150-144
GAIN	CONTROL BITS							
	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
1.999 (MAXIMUM)	0	1	1	1	1	1	1	1
1 (CCIR-level)	0	1	0	0	0	0	0	0
0 (COLOUR OFF)	0	0	0	0	0	0	0	0
-1 (inverse chroma)	1	1	0	0	0	0	0	0
-2 (inverse chroma)	1	0	0	0	0	0	0	0

Subaddress 13 Luminance Contrast Control								158-152
GAIN	CONTROL BITS							
	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
1.999 (MAXIMUM)	0	1	1	1	1	1	1	1
70(CCIR-level)	0	1	0	0	0	1	1	0
1	0	1	0	0	0	0	0	0
0 (LUMINANCE OFF)	0	0	0	0	0	0	0	0
-1 (inverse luminance)	1	1	0	0	0	0	0	0
-2 (inverse luminance)	1	0	0	0	0	0	0	0

TABLE 17. IIC DETAIL SU10h-13h(128-158)

Subaddress 14 Horizontal sync begin 60 Hz HS6B									167-160
DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HS6B7	HS6B6	HS6B5	HS6B4	HS6B3	HS6B2	HS6B1	HS6B0
+191...	-382	1	0	1	1	1	1	1	1
... -64	+128	1	1	0	0	0	0	0	0

Subaddress 15 Horizontal sync stop 60 Hz HS6S									175-168
DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HS6S7	HS6S6	HS6S5	HS6S4	HS6S3	HS6S2	HS6S1	HS6S0
+191...	-382	1	0	1	1	1	1	1	1
... -64	+128	1	1	0	0	0	0	0	0

TABLE 18. IIC DETAIL SU14h-18h(160-199)

Subaddress 16 Horizontal clamp begin 60 Hz HC6B									183-176
DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HC6B7	HC6B6	HC6B5	HC6B4	HC6B3	HC6B2	HC6B1	HC6B0
+127...	-254	0	1	1	1	1	1	1	1
... -128	+256	1	0	0	0	0	0	0	0

Subaddress 17 Horizontal clamp stop 60 Hz HC6S									191-184
DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HCL67	HC6S6	HC6S5	HC6S4	HC6S3	HC6S2	HC6S1	HC6S0
+127...	-254	0	1	1	1	1	1	1	1
... -128	+256	1	0	0	0	0	0	0	0

Subaddress 18 Horizontal sync start after PHI1 60 Hz HP6I									199-192
DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 8/LLC	CONTROL BITS							
		HP6I7	HP6I6	HP6I5	HP6I4	HP6I3	HP6I2	HP6I1	HP6I0
+127...	Forbidden; outside available central counter range	0	1	1	1	1	1	1	1
... +98	Forbidden; outside available central counter range	0	1	1	0	0	0	1	0
+97...	-32 µs (max. negative value)	0	1	1	0	0	0	0	1
... -97	+31.7 µs (max. positive value)	1	0	0	1	1	1	1	1
-98...	Forbidden; outside available central counter range	1	0	0	1	1	1	1	0
... -128	Forbidden; outside available central counter range	1	0	0	0	0	0	0	0

TABLE 18. IIC DETAIL SU14h-18h(160-199)

Subaddress 19 Luminance brightness control									207-200
OFFSET	CONTROL BITS								
	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0	
255 (bright)	1	1	1	1	1	1	1	1	
139 (CCIR-level)	1	0	0	0	1	0	1	1	
128	1	0	0	0	0	0	0	0	
0 (dark)	0	0	0	0	0	0	0	0	

TABLE 19. IIC DETAIL SU19h(200-207)

DUAD SLAVE RECEIVER (SU 20h-32h)		
Subaddress 20 Analog control #1		**007-000**
Analog input select 2 AINS2		000
FUNCTION	**CONTROL BIT AINS2**	
Analog input AI22 selected	0	
Analog input AI21 selected	1	
Analog input select 3 AINS3		001
FUNCTION	**CONTROL BIT AINS3**	
Analog input AI32 selected	0	
Analog input AI31 selected	1	
Analog input select 4 AINS4		002
FUNCTION	**CONTROL BIT AINS4**	
Analog input AI42 selected	0	
Analog input AI41 selected	1	
Analog function select FUSE		004-003
FUNCTION	**CONTROL BITS FUSE(1:0)**	
	FUSE1	**FUSE0**
AMPLIFIER + ANTI ALIAS FILTER bypassed	0	0
	0	1
AMPLIFIER active	1	0
AMPLIFIER + ANTI ALIAS FILTER active	1	1
Analog input disable 2 AIND2		005
FUNCTION	**CONTROL BIT AIND2**	
Analog inputs 2 enabled	0	
Analog inputs 2 disabled	1	
Analog input disable 3 AIND3		006
FUNCTION	**CONTROL BIT AIND3**	
Analog inputs 3 enabled	0	
Analog inputs 3 disabled	1	

TABLE 20. IIC DETAIL SU20h(000-006)

Analog input disable 4 AIND4	007
FUNCTION	**CONTROL BIT AIND4**
Analog inputs 4 enabled	0
Analog inputs 4 disabled	1

TABLE 21. IIC DETAIL SU20h-21h(007-015)

Subaddress 21 Analog control #2		**015-008**
Reference select channel 2 REFS2		008
FUNCTION	**CONTROL BIT REFS2**	
Automatic clamping active	0	
Reference level selected	1	
Reference select channel 3 REFS3		009
FUNCTION	**CONTROL BIT REFS3**	
Automatic clamping active	0	
Reference level selected	1	
Reference select channel 4 REFS4		010
FUNCTION	**CONTROL BIT REFS4**	
Automatic clamping active	0	
Reference level selected	1	
MUXC select channel 24 MS24		011
FUNCTION	**CONTROL BIT MS24**	
Analog MUX2 controlled by MX24	0	
Analog MUX2 controlled by MUXC	1	
Analog MUX2 control MX24		013-012
FUNCTION	**CONTROL BITS MX24(1:0)**	
	MX241	**MX240**
ADDER mode	0	0
ch2 on, ch4 off	0	1
ch2 off, ch4 on	1	0
both off	1	1
MUXC select channel 34 MS34		014
FUNCTION	**CONTROL BIT MS34**	
Analog MUX3 controlled by MX34	0	
Analog MUX3 controlled by MUXC	1	
Vertical blanking control off VBCO		015
FUNCTION	**CONTROL BIT VBCO**	
vertical blanking on	0	
vertical blanking off	1	

TABLE 21. IIC DETAIL SU20h-21h(007-015)

Subaddress 22 Mix control #1		**023-016**
Analog MUX3 control MX34		017-016
FUNCTION	**CONTROL BITS MX34(1:0)**	
	MX341	**MX340**
ADDER mode	0	0
ch3 on, ch4 off	0	1
ch3 off, ch4 on	1	0
both off	1	1
Clamp function test CLTS		018
FUNCTION	**CONTROL BIT CLTS**	
normal clamp mode	0	
CLAAn, CLAUn adjusted via CLL32 value for testing (do not use)	1	
Fast digital multiplexing channel 2/3 active MUYC		019
FUNCTION	**CONTROL BIT MUYC**	
normal mode on CHR channel	0	
multiplex mode on CHR channel for test purpose only (do not use)	1	
Luminance select YSEL		020
FUNCTION	**CONTROL BIT YSEL**	
AD converter 2 -> CVBS	0	
AD converter 3 -> CVBS	1	
Chrominance select CSEL		021
FUNCTION	**CONTROL BIT CSEL**	
AD converter 3 -> CHR (MUXC not inverse (MUYC=1))	0	
AD converter 2 -> CHR (MUXC inverse (MUYC=1))	1	
Automatic gain control GACO		023-022
FUNCTION	**CONTROL BITS GACO(1:0)**	
	GACO1	**GACO0**
automatic gain control off	0	0
automatic gain control channel 2	0	1
automatic gain control channel 3	1	0
automatic gain control channel 4	1	1

TABLE 22. IIC DETAIL SU22h-23h(016-031)

Subaddress 23 Clamp level control 21 CLL21								031-024
DECIMAL CLAMP LEVEL	CONTROL BITS							
	CLL217	CLL216	CLL215	CLL214	CLL213	CLL212	CLL211	CLL210
1...	0	0	0	0	0	0	0	1
... 64...	0	1	0	0	0	0	0	0
... 128...	1	0	0	0	0	0	0	0
... 254	1	1	1	1	1	1	1	0

TABLE 22. IIC DETAIL SU22h-23h(016-031)

Subaddress 24 Clamp level control 22 CLL22								039-032
DECIMAL CLAMP LEVEL	CONTROL BITS							
	CLL227	CLL226	CLL225	CLL224	CLL223	CLL222	CLL221	CLL220
1...	0	0	0	0	0	0	0	1
... 64...	0	1	0	0	0	0	0	0
... 128...	1	0	0	0	0	0	0	0
... 254	1	1	1	1	1	1	1	0
Subaddress 25 Clamp level control 31 CLL31								**047-040**
DECIMAL CLAMP LEVEL	CONTROL BITS							
	CLL317	CLL316	CLL315	CLL314	CLL313	CLL312	CLL311	CLL310
1...	0	0	0	0	0	0	0	1
... 64...	0	1	0	0	0	0	0	0
... 128...	1	0	0	0	0	0	0	0
... 254	1	1	1	1	1	1	1	0
Subaddress 26 Clamp level control 32 CLL32								**055-048**
DECIMAL CLAMP LEVEL	CONTROL BITS							
	CLL327	CLL326	CLL325	CLL324	CLL323	CLL322	CLL321	CLL320
1...	0	0	0	0	0	0	0	1
... 64...	0	1	0	0	0	0	0	0
... 128...	1	0	0	0	0	0	0	0
... 254	1	1	1	1	1	1	1	0

TABLE 23. IIC DETAIL SU24h-SU27h(032-063)

Subaddress 27 Gain control analog #1								**063-056**
Static gain control channel 2 GAI2								061-056
DECIMAL MULTI-PLIER	**GAIN (STEP SIZE = 0.19 dB)**	**CONTROL BITS**						
			GAI25	**GAI24**	**GAI23**	**GAI22**	**GAI21**	**GAI20**
0...	-2.82 dB		0	0	0	0	0	0
... 15...	0 dB		0	0	1	1	1	1
... 31...	+3 dB		0	1	1	1	1	1
... 47...	+6 dB		1	0	1	1	1	1
... 63	+9 dB		1	1	1	1	1	1

Gain mode select GASL	062
FUNCTION	**CONTROL BIT GASL**
difference value integration	0
fix value integration	1

Automatic gain control integration HOLD	063
FUNCTION	**CONTROL BIT HOLD**
AGC active	0
AGC integration hold (freeze)	1

TABLE 23. IIC DETAIL SU24h-SU27h(032-063)

Subaddress 28 White peak control WIPE								**071-064**
DECIMAL WHITE PEAK LEVEL	**CONTROL BITS**							
	WIPE7	**WIPE6**	**WIPE5**	**WIPE4**	**WIPE3**	**WIPE2**	**WIPE1**	**WIPE0**
128...	1	0	0	0	0	0	0	0
... 254	1	1	1	1	1	1	1	0
255 (White peak control off)	1	1	1	1	1	1	1	1

Subaddress 29 Sync bottom control SBOT								**079-072**
DECIMAL SYNC BOTTOM LEVEL	**CONTROL BITS**							
	SBOT7	**SBOT6**	**SBOT5**	**SBOT4**	**SBOT3**	**SBOT2**	**SBOT1**	**SBOT0**
1...	0	0	0	0	0	0	0	1
... 254	1	1	1	1	1	1	1	0

TABLE 24. IIC DETAIL SU28h-2Bh(064-093)

Subaddress 2A Gain control analog #2								**087-080**
Static gain control channel 3 GAI3								085-080
DECIMAL MULTI-PLIER	**GAIN (STEP SIZE = 0.19 dB)**	**CONTROL BITS**						
			GAI35	**GAI34**	**GAI33**	**GAI32**	**GAI31**	**GAI30**
0...	-2.82 dB		0	0	0	0	0	0
... 15...	0 db		0	0	1	1	1	1
... 31...	+ 3 dB		0	1	1	1	1	1
... 47...	+6 dB		1	0	1	1	1	1
... 63	+9 dB		1	1	1	1	1	1

Integration factor white peak IWIP		087-086
FUNCTION	**CONTROL BITS IWIP(1:0)**	
	IWIP1	**IWIP0**
fast	0	0
I	0	1
I	1	0
slow	1	1

Subaddress 2B Gain control analog #3								**095-088**
Static gain control channel 4 GAI4								093-088
DECIMAL MULTI-PLIER	**GAIN (STEP SIZE = 0.19 dB)**	**CONTROL BITS**						
			GAI45	**GAI44**	**GAI43**	**GAI42**	**GAI41**	**GAI40**
0...	-2.82 dB		0	0	0	0	0	0
... 15...	0 db		0	0	1	1	1	1
... 31...	+ 3 dB		0	1	1	1	1	1
... 47...	+6 dB		1	0	1	1	1	1
... 63	+9 dB		1	1	1	1	1	1

TABLE 24. IIC DETAIL SU28h-2Bh(064-093)

Integration factor normal gain IGAI		095-094
FUNCTION	**CONTROL BITS IGAI(1:0)**	
	IGAI1	**IGAI0**
slow	0	0
I	0	1
I	1	0
fast	1	1

TABLE 25. IIC DETAIL SU2Bh-2Eh(094-119)

Subaddress 2C Mix control #2	**103-096**
Two's complement channel 2 TWO2	096
FUNCTION	**CONTROL BIT TWO2**
unipolar	0
two's complement (normal mode)	1
Two's complement channel 3 TWO3	097
FUNCTION	**CONTROL BIT TWO3**
unipolar	0
two's complement (normal mode)	1
Clamp level select channel 2 CLS2	100
FUNCTION	**CONTROL BIT CLS2**
CLL21 active	0
CLL22 active	1
Clamp level select channel 3 CLS3	101
FUNCTION	**CONTROL BIT CLS3**
CLL31 active	0
CLL32 active	1
Clamp level select channel 4 CLS4	103
FUNCTION	**CONTROL BIT CLS4**
CLL2n active	0
CLL3n active	1

Subaddress 2D Integration value gain IVAL								**111-104**
DECIMAL INTEGRATION VALUE GAIN	**CONTROL BITS**							
	IVAL7	**IVAL6**	**IVAL5**	**IVAL4**	**IVAL3**	**IVAL2**	**IVAL1**	**IVAL0**
1...	0	0	0	0	0	0	0	1
... 255	1	1	1	1	1	1	1	1

Subaddress 2E Blank pulse VBLK-set VBPS									**119-112**
DECIMAL MULTI-PLIER	**SET LINE NUMBER step size = 2**	**CONTROL BITS**							
		VBPS7	**VBPS6**	**VBPS5**	**VBPS4**	**VBPS3**	**VBPS2**	**VBPS1**	**VBPS0**
0...	0 after ^VS	0	0	0	0	0	0	0	0
...131... (max. for 60Hz)	262 after ^VS	1	0	0	0	0	0	1	1
...156 (max. for 50Hz)	312 after ^VS	1	0	0	1	1	1	0	0

TABLE 25. IIC DETAIL SU2Bh-2Eh(094-119)

Subaddress 2F Blank pulse VBLK-reset VBPR									127-120
DECIMAL MULTIPLIER	RESET LINE NUMBER step size = 2	CONTROL BITS							
		VBPR7	VBPR6	VBPR5	VBPR4	VBPR3	VBPR2	VBPR1	VBPR0
0...	0 after ^VS	0	0	0	0	0	0	0	0
...131... (max. for 60Hz)	262 after ^VS	1	0	0	0	0	0	1	1
...156 (max. for 50Hz)	312 after ^VS	1	0	0	1	1	1	0	0

Subaddress 30 ADCs gain control		135-128
Fix gain A/D converter channel 2 GAD2		129-128
FUNCTION	CONTROL BITS GAD2(1:0)	
	GAD21	GAD20
0 dB	0	0
0.05 dB	0	1
0.10 dB	1	0
0.15 dB	1	1
Gain A/D select channel 2 GAS2		130
FUNCTION	CONTROL BIT GAS2	
fix gain via IIC GAD2	0	
automatic gain via loop	1	
Fix gain A/D converter channel 3 GAD3		132-131
FUNCTION	CONTROL BITS GAD3(1:0)	
	GAD31	GAD30
0 dB	0	0
0.05 dB	0	1
0.10 dB	1	0
0.15 dB	1	1
Gain A/D select channel 3 GAS3		133
FUNCTION	CONTROL BIT GAS3	
fix gain via IIC GAD3	0	
automatic gain via loop	1	
White peak mode select WISL		134
FUNCTION	CONTROL BIT WISL	
difference value integration	0	
fix value integration	1	

Subaddress 31 Mix control #3		143-136
Pulses I/O control PULIO		136
FUNCTION	CONTROL BIT PULIO	
HCL, HSY -> input pins	0	
HCL, HSY -> output pins	1	

TABLE 26. IIC DETAIL SU2Fh-31h(120-143)

Pin function switch VBLKA	137
FUNCTION	**CONTROL BIT VBLKA**
GPSW active (normal)	0
VBLK test output active	1

DMSD-SQP bypassed SQPB	139
FUNCTION	**CONTROL BIT SQPB**
DMSD-data to YUV output	0
A/D-data to YUV output for test purpose only (do not use)	1

White peak slow up integration enable WRSE	140
FUNCTION	**CONTROL BIT WRSE**
hold in white peak mode	0
slow up integration with one value in H or V (dependent on WIRS)	1

White peak slow up integration select WIRS	141
FUNCTION	**CONTROL BIT WIRS**
slow up integration with one value per line	0
slow up integration with one value per field	1

Analog test select AOSL	143-142	
FUNCTION	**CONTROL BITS AOSL(1:0)**	
	AOSL1	**AOSL0**
AOUT connected to ground	0	0
AOUT connected to input AD2	0	1
AOUT connected to input AD3	1	0
AOUT connected to channel 4	1	1

Subaddress 32 Integration value white peak IVAL								**151-144**
DECIMAL INTEGRATION VALUE WHITE PEAK	**CONTROL BITS**							
	WVAL7	**WVAL6**	**WVAL5**	**WVAL4**	**WVAL3**	**WVAL2**	**WVAL1**	**WVAL0**
1...	0	0	0	0	0	0	0	1
... 127 (max.)	0	1	1	1	1	1	1	1

Subaddress 33 Mix control #4	**159-152**
Clock select AD2 CAD2	154
FUNCTION	**CONTROL BIT CAD2**
LLC for test purpose only (do not use)	0
LLC/2	1

TABLE 27. IIC DETAIL SU31h-33h(137-154)

Clock select AD3 CAD3	155
FUNCTION	**CONTROL BIT CAD3**
LLC for test purpose only (do not use)	0
LLC/2	1

Change sign bit UV data CHSB	157
FUNCTION	**CONTROL BIT CHSB**
UV output unipolar	0
UV output two's complement	1

Output format select OFTS	159
FUNCTION	**CONTROL BIT OFTS**
4:1:1 format	0
4:2:2 format	1

Subaddress 34 Gain update level **167-160**

Gain update level GUDL 165-160

DECIMAL	HYSTERESIS for 8bit gain	update I new gain - old gain I =	CONTROL BITS GUDL(5:0)					
			GUDL5	GUDL4	GUDL3	GUDL2	GUDL1	GUDL0
0...	0 LSB	>0	0	0	0	0	0	0
... 7...	+/- 7 LSB	>7	0	0	0	1	1	1
>31	OFF	always	1	X	X	X	X	X

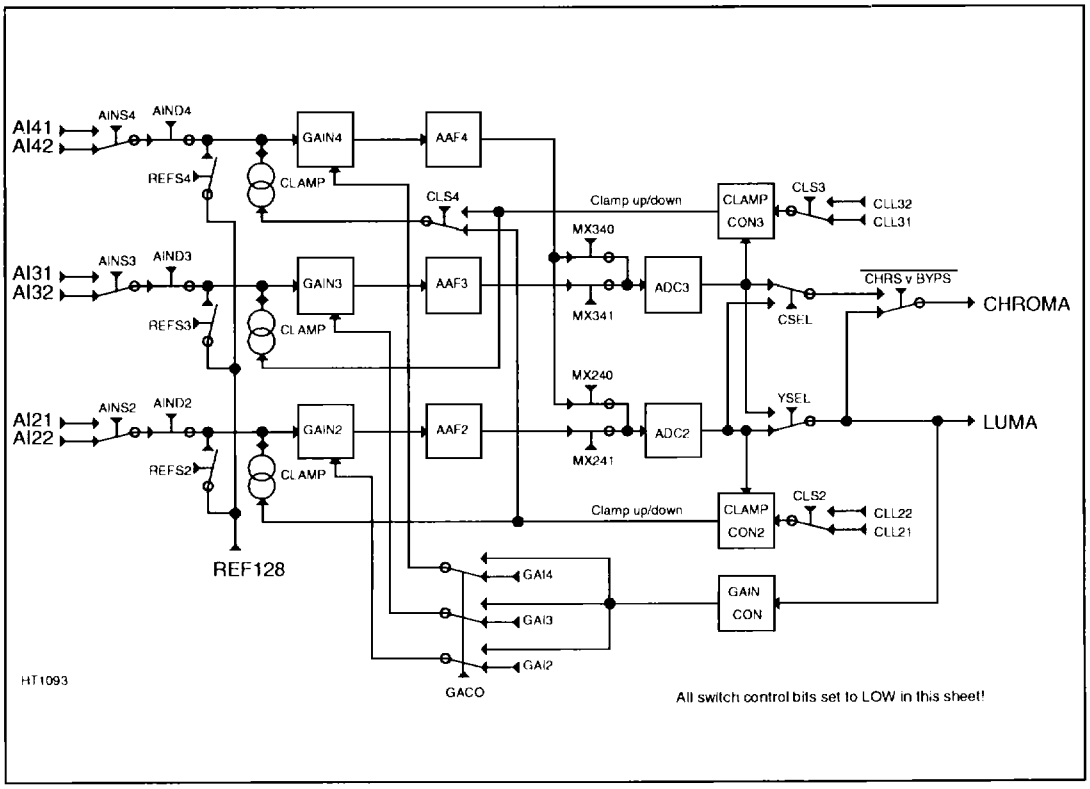
MUXC phase delay MUD2(1) 167-166

FUNCTION	CONTROL BITS	
	MUD2	MUD1
no phase delay	0	0
1 LLC cycle phase delay for CLAA path	0	1
2 LLC cycle phase delay for CLAA path	1	0
3 LLC cycle phase delay for CLAA path	1	1

TABLE 28. IIC DETAIL SU33h-34h(155-167)

19.2 SOURCE SELECTION MANAGEMENT

FIGURE 20. SOURCE SELECTION OVERVIEW



INPUT	EXAMPLE1		EXAMPLE2		EXAMPLE3		EXAMPLE4	
	SIGNAL	MODE	SIGNAL	MODE	SIGNAL	MODE	SIGNAL	MODE
AIN21	CVBS1	0	CVBS1	0	Y1	6	Y1	6
AIN22	CVBS2	1	C2	7	C2	7	CVBS2	1
AIN31	CVBS3	2	Y2		Y2		CVBS3	2
AIN32	CVBS4	3	C3	8	C3	8	CVBS4	3
AIN41	CVBS5	4	Y3		Y3		CVBS5	4
AIN42	CVBS6	5	CVBS6	5	C1	6	C1	6

TABLE 29. SOURCE SELECTION MANAGEMENT example table

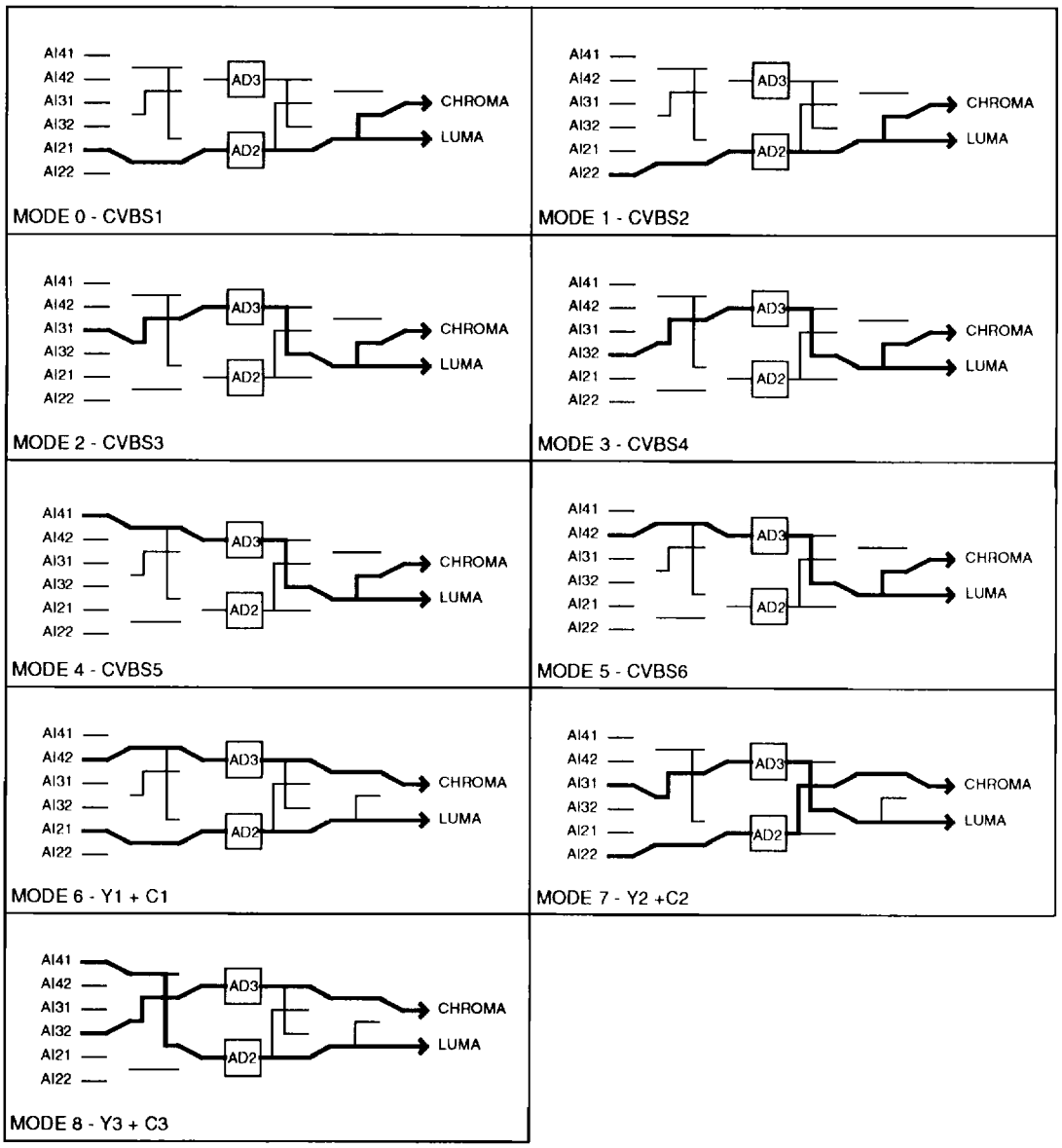


TABLE 30. SOURCE SELECTION MANAGEMENT example sheets

MODE	0	1	2	3	4	5	6	7	8	9
AIND4	1	1	1	1	0	0	0	1	0	
AIND3	1	1	0	0	1	1	1	0	0	
AIND2	0	0	1	1	1	1	0	0	1	
FUSE1 FUSE0	1 1									
AINS4	X	X	X	X	1	0	0	X	1	
AINS3	X	X	1	0	X	X	0	1	0	
AINS2	1	0	X	X	X	X	1	0	X	
VBC0	0									
MS34	0									
MX241	0	0	X	X	X	X	0	0	1	
MX240	1	1	X	X	X	X	1	1	0	
MS24	0									
REFS4	1	1	1	1	0	0	0	1	0	
REFS3	1	1	0	0	1	1	1	0	0	
REFS2	0	0	1	1	1	1	0	0	1	
GACO1 GACO0	0 1	0 1	1 0	1 0	1 1	1 1	0 1	1 0	1 1	
CSEL	X	X	X	X	X	X	0	1	0	
YSEL	0	0	1	1	1	1	0	1	0	
MUYC	0									0
CLTS	0									0
MX341	X	X	0	0	1	1	1	0	0	
MX340	X	X	1	1	0	0	0	1	1	
CLS4	X	X	X	X	1	1	1	X	0	
GABL	0									
CLS3	X	X	0	0	0	0	1	0	1	
CLS2	0	0	X	X	X	X	0	1	X	
4 LSB	0011									0011
BYPS	0	0	0	0	0	0	1	1	1	
SU20h	D9h	D8h	BAh	B8h	7Ch	78h	59h	9Ah	3Ch	
SU21h	16h	16h	05h	05h	03h	03h	12h	14h	21h	
SU22h	40h	40h	91h	91h	D2h	D2h	42h	B1h	C1h	
SU2Ch	03h	03h	03h	03h	83h	83h	A3h	13h	23h	
SU06h	0XXXXXXX						1XXXXXXX			
SU30h*	44h	44h	60h	60h	60h	60h	44h	60h	44h	

Note: CLL21=65d, CLL22=128d, CLL31=65d, CLL32=128d, GAI4=15d, GAI3=15d, GAI2=15d; X set to 0
*Optional: values for AD-gain (+2LSB's gain resolution) active [not active: for all modes 40h]

TABLE 31. SOURCE SELECTION MANAGEMENT IIC control

19.3 ANTI-ALIAS FILTER CURVES

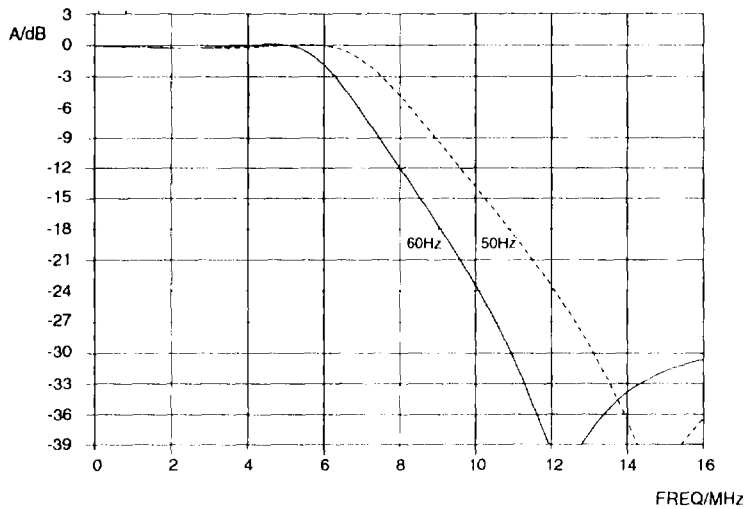


FIGURE 21. ANTI ALIAS FILTERCURVE SAA7110A

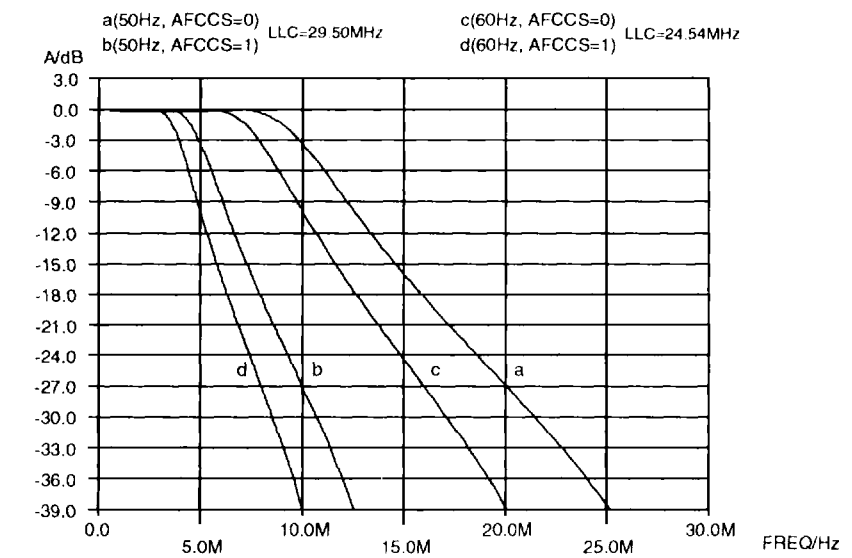
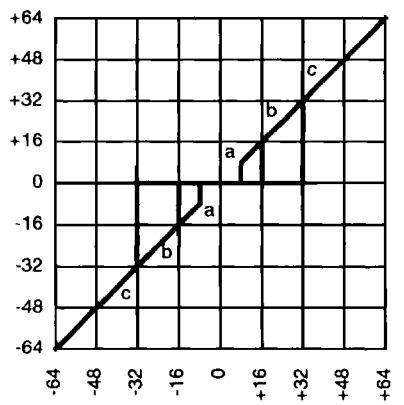


FIGURE 22. ANTI ALIAS FILTERCURVE SAA7110

19.4 CORING FUNCTION

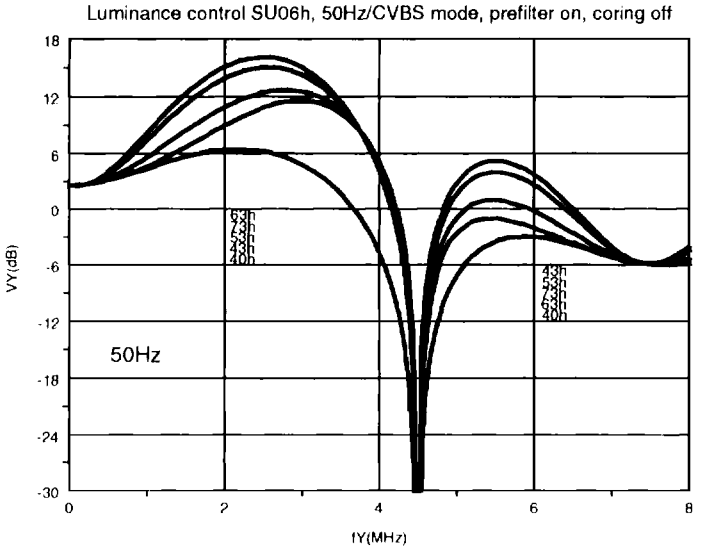


Coring function adjustment by subadress 06h to affect the bandfilter output signal. The thresholds are related to the 13-bit word width in the luminance processing part and influence the 1LSB to the 3LSB (Y0 to Y2) with respect to the 8-bit luminance output.

	CORI1	CORI0
a	0	1
b	1	0
c	1	1

TABLE 32. CORING

19.5 LUMINANCE FILTER CURVES



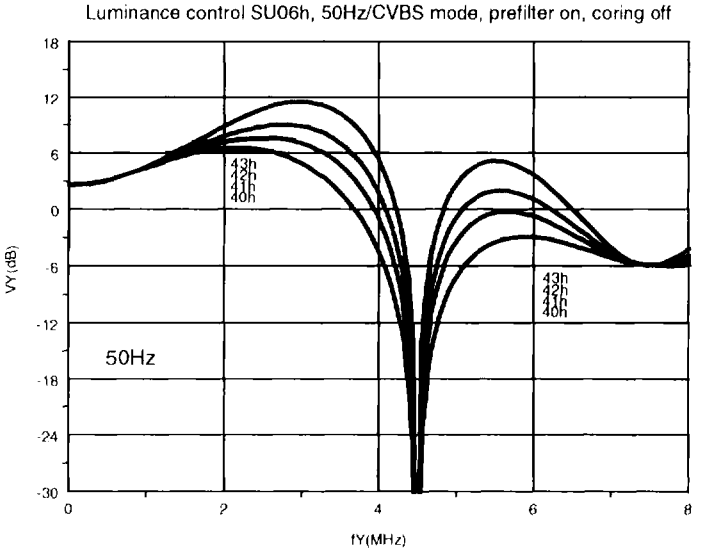
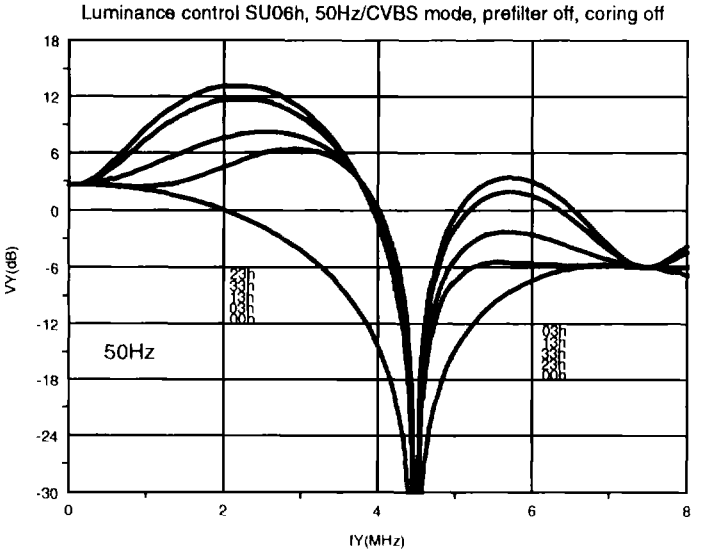


TABLE 33. LUMINANCE FILTER CURVES



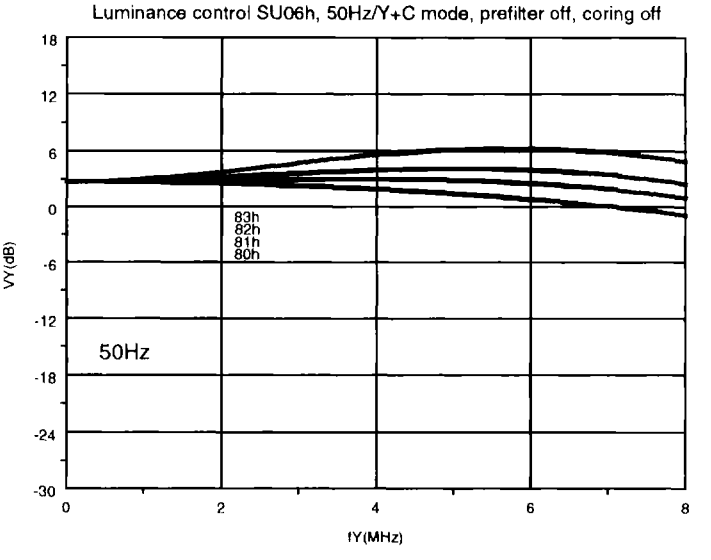
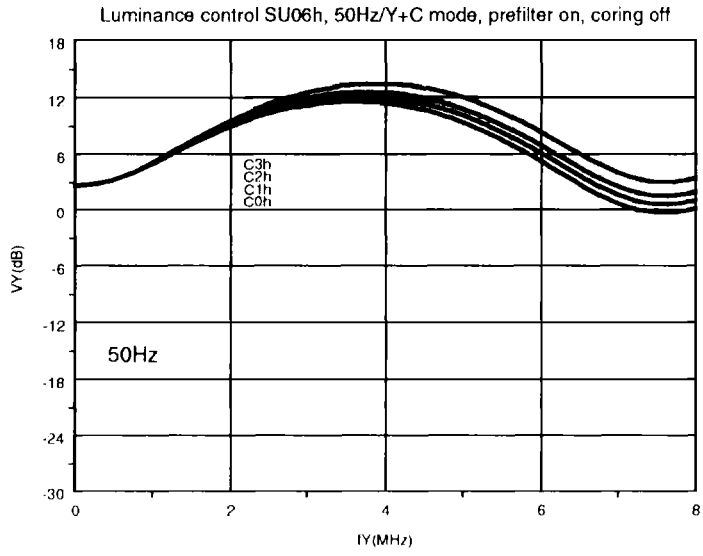


TABLE 33. LUMINANCE FILTER CURVES



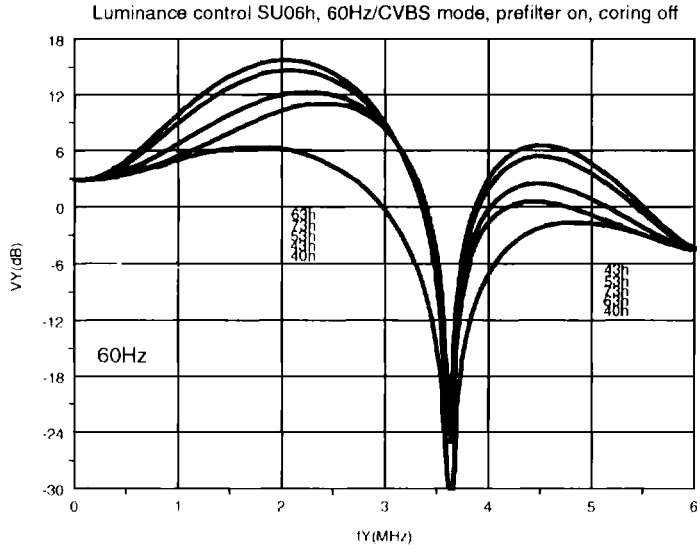


TABLE 33. LUMINANCE FILTER CURVES

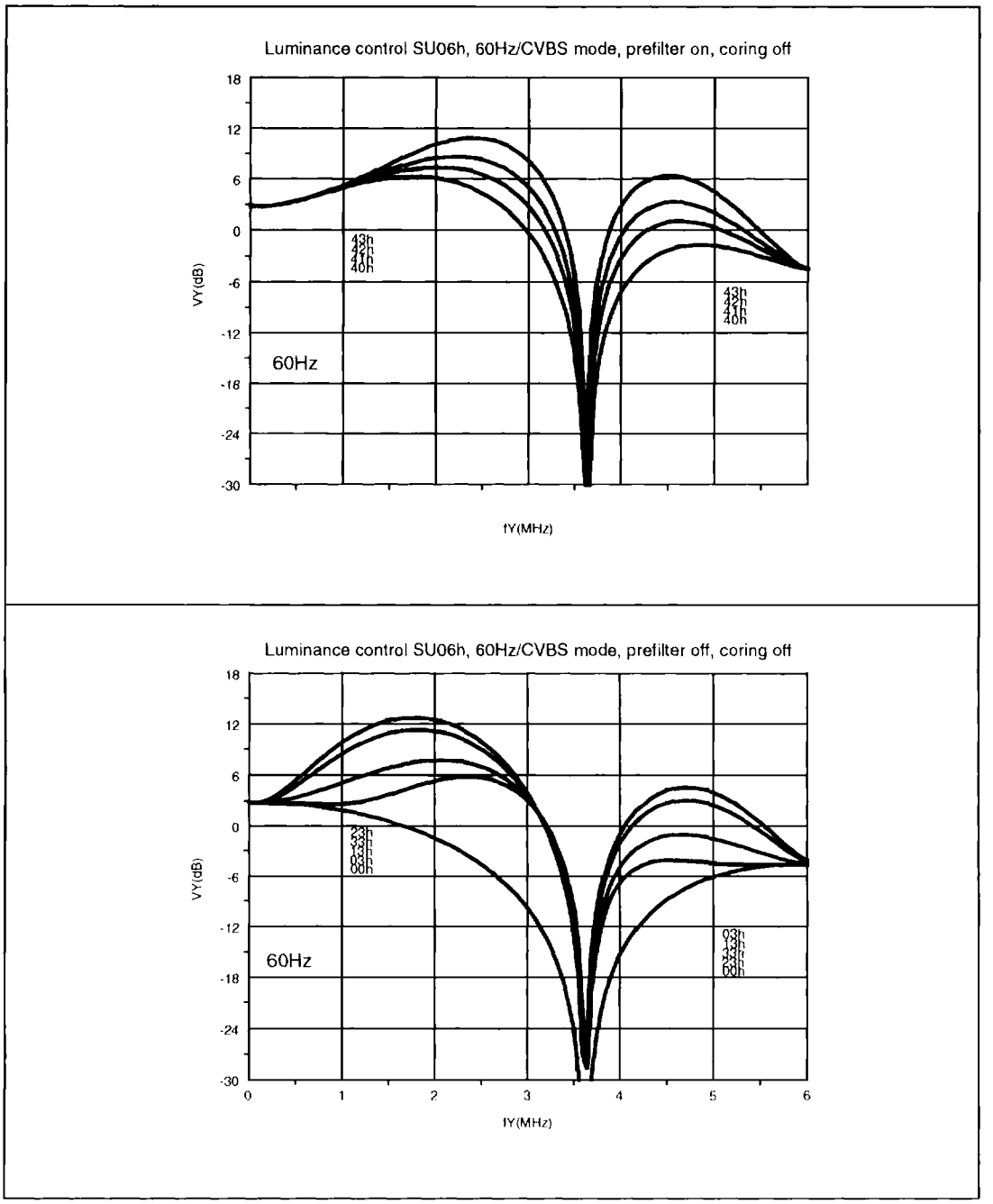
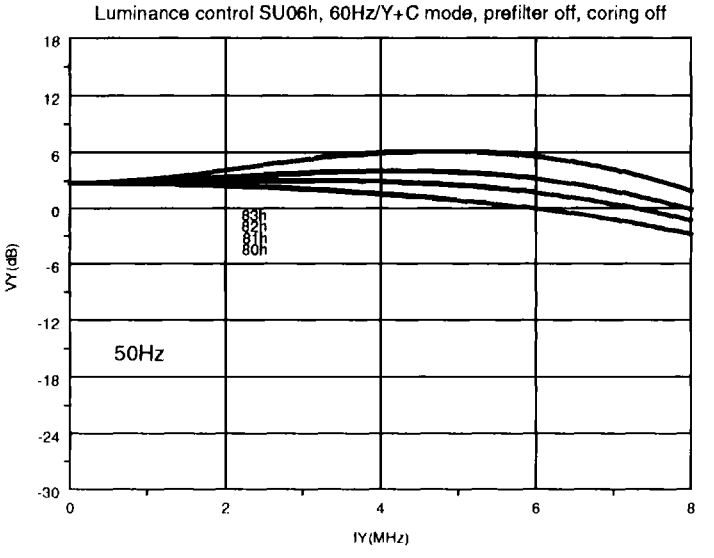


TABLE 33. LUMINANCE FILTER CURVES



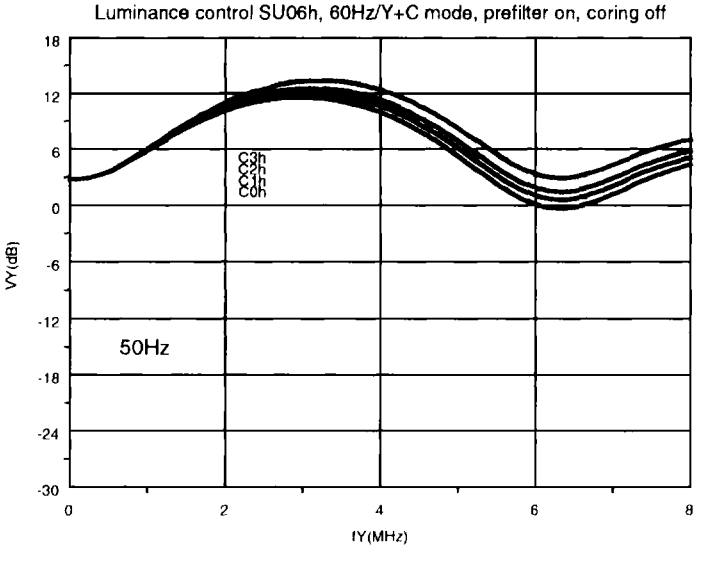


TABLE 33. LUMINANCE FILTER CURVES

20. IIC START SETUP

The following values are optimized for the EBU colour bar (100% white and 75% chrominance amplitude) input signal. The decoder output signal level fulfills the CCIR Rec.601 specification. The input of 100% color bar level is possible, but the signal (white) peak function reduces the digital luminance output. With another setup it is possible to proceed 100% color bar signal without luminance amplitude reduction. The way is to modify the AD input range for this input level by reducing the gain reference value (SBOT > 06h) and adjusting the digital Y output level with contrast and brightness control.

SUB	NAME	FUNCTION	VALUES(bin)								(hex)
			7	6	5	4	3	2	1	0	start
00	IDEL(7:0)	Increment delay	0	1	0	0	1	1	0	0	4C
01	HSYB(7:0)	Horizontal sync HSY begin 50Hz	0	0	1	1	1	1	0	0	3C
02	HSYS(7:0)	Horizontal sync HSY stop 50Hz	0	0	0	0	1	1	0	1	0D
03	HCLB(7:0)	Horizontal clamp HCL begin 50Hz	1	1	1	0	1	1	1	1	EF
04	HCLS(7:0)	Horizontal clamp HCL stop 50Hz	1	0	1	1	1	1	0	1	BD
05	HPHI(7:0)	Horizontal sync after PHI1 50Hz	1	1	1	1	0	0	0	0	F0
06	BYPS, PREF, BPSS(1:0), BF-BY, CORI(1:0), APER(1:0)	Luminance control	0	0	0	0	0	0	0	0	00
07	HUEC(7:0)	Hue control	0	0	0	0	0	0	0	0	00
08	CKTQ(4:0), XXX	Colour killer threshold PAL	1	1	1	1	1	X	X	X	F8
09	CKTS(4:0), XXX	Colour killer threshold SECAM	1	1	1	1	1	X	X	X	F8
0A	PLSE(7:0)	PAL switch sensitivity	0	1	1	0	0	0	0	0	60
0B	SESE(7:0)	SECAM switch sensitivity	0	1	1	0	0	0	0	0	5B
0C	COLO, LFIS(1:0), XXXXX	Gain control chrominance	0	0	0	X	X	X	X	X	00
0D	VTRC, XXX, RTSE, HRMV, SSTB, SECS	Standard/Mode control	0	X	X	X	0	1	1	0	06
0E	HPLL, XX, OEHV, OEYC, CHRS, X, GPSW	I/O and clock control	0	X	X	1	1	0	X	0	18
0F	AUFD, FSEL, SXCR, SCEN, X, YDEL(2:0)	Control #1	1	0	0	1	X	0	0	0	90
10	XXXXX, HRFS, VNOI(1:0)	Control #2	X	X	X	X	X	0	0	0	00
11	CHCV(7:0) PAL	Chroma gain reference	0	1	0	1	1	0	0	1	59
	CHCV(7:0) NTSC		0	0	1	0	1	1	0	0	2C
12	SATN(7:0)	Chroma saturation	0	1	0	0	0	0	0	0	40
13	CONT(7:0)	Luminance contrast	0	1	0	0	0	1	1	0	46
14	HS6B(7:0)	Horizontal sync HSY begin 60Hz	0	1	0	0	0	0	1	0	42
15	HS6S(7:0)	Horizontal sync HSY stop 60Hz	0	0	0	1	1	0	1	0	1A
16	HC6B(7:0)	Horizontal clamp HCL begin 60Hz	1	1	1	1	1	1	1	1	FF
17	HC6S(7:0)	Horizontal clamp HCL stop 60Hz	1	1	0	1	1	0	1	0	DA
18	HP6I(7:0)	Horizontal sync after PHI1 60Hz	1	1	1	1	0	0	0	0	F0
19	BRIG(7:0)	Luminance brightness	1	0	0	0	1	0	1	1	8B
1A-1F	reserved										

TABLE 34. IIC START SETUP

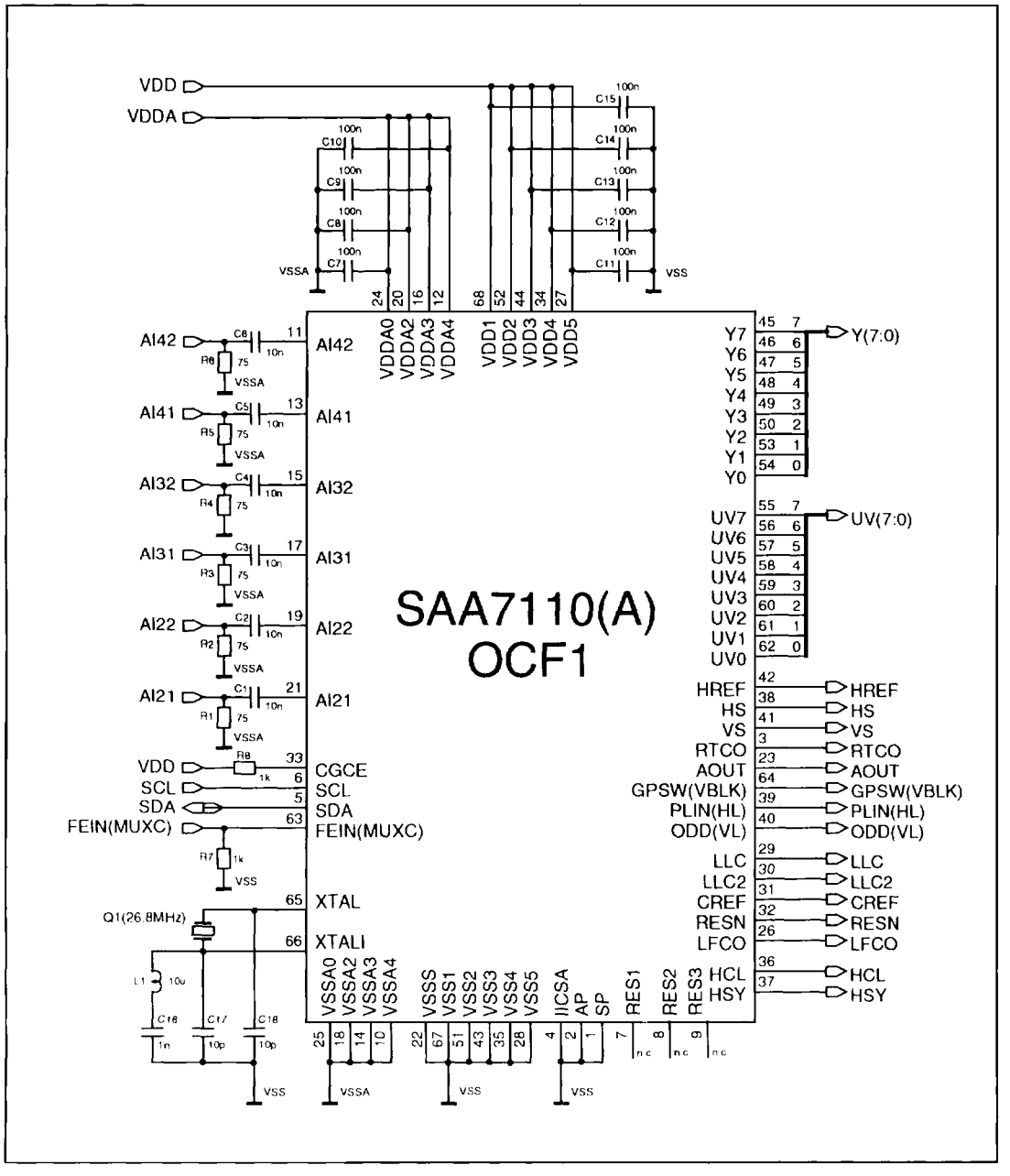
20	AIND4, AIND3, AIND2, FUSE(1:0), AINS4, AINS3, AINS2		Analog control #1	1	1	0	1	1	0	0	1	D9
21	VBCO, MS34, MX24(1:0), MS24, REFS4, REFS3, REFS2		Analog control #2	0	0	0	1	0	1	1	0	16
22	GACO(1:0), CSEL, YSEL, MUYC, CLTS, MX34(1:0)		Mix control #1	0	1	0	0	0	0	0	0	40
23	CLL21(7:0)		Clamp level control channel 2 1	0	1	0	0	0	0	0	1	41
24	CLL22(7:0)		Clamp level control channel 2 2	1	0	0	0	0	0	0	0	80
25	CLL31(7:0)		Clamp level control channel 3 1	0	1	0	0	0	0	0	1	41
26	CLL32(7:0)		Clamp level control channel 3 2	1	0	0	0	0	0	0	0	80
27	HOLD, GASL, GAI2(5:0)		Gain control analog #1	0	1	0	0	1	1	1	1	4F
28	WIPE(7:0)		White peak control	1	1	1	1	1	1	1	0	FE
29	SBOT(7:0)		Sync bottom control	0	0	0	0	0	0	0	1	01
2A	IWIP(1:0), GAI3(5:0)		Gain control analog #2	1	1	0	0	1	1	1	1	CF
2B	IGAI(1:0), GAI4(5:0)		Gain control analog #3	0	0	0	0	1	1	1	1	0F
2C	CLS4, X, CLS3, CLS2, XX, TWO3, TWO2		Mix control #2	0	X	0	0	X	X	1	1	03
2D	IVAL(7:0)		Integration value gain	0	0	0	0	0	0	0	1	01
2E	VBPS(7:0)	50Hz	Vertical blanking pulse SET	1	0	0	1	1	0	1	0	9A
		60Hz		1	0	0	0	0	0	0	1	81
2F	VBPR(7:0)	50Hz	Vertical blanking pulse RESET	0	0	0	0	0	0	1	1	03
		60Hz		0	0	0	0	0	0	1	1	03
30	X, WISL, GAS3, GAD3(1.0), GAS2, GAD2(1:0)		ADCs gain control	X	1	0	0	0	0	0	0	44
31	AOSL(1:0), WIRS, WRSE, SQPB, X, VBLKA, PULIO		Mix control #3	0	1	1	1	0	X*	0	1	71
32	WVAL(7:0)		Integration value white peak	0	0	0	0	0	0	1	0	02
33	OFTS, X, CHSB, X, CAD2, CAD3, XX		Mix control #4	1	X	0	X	1	1	X	X	8C
34	MUD2, MUD1, GUDL(5:0)		Gain update level	0	0	0	0	0	0	1	1	03

Note: Values recommended for a CVBS (PAL or NTSC) signal, input AI21 via A/D channel 2 (MODE 0), and 4:2:2 CCIR output signal level; all X values must be set to LOW, X* value don't care; HPHI and HP6I -> application dependent.

TABLE 34. IIC START SETUP

21. APPLICATION SHEET

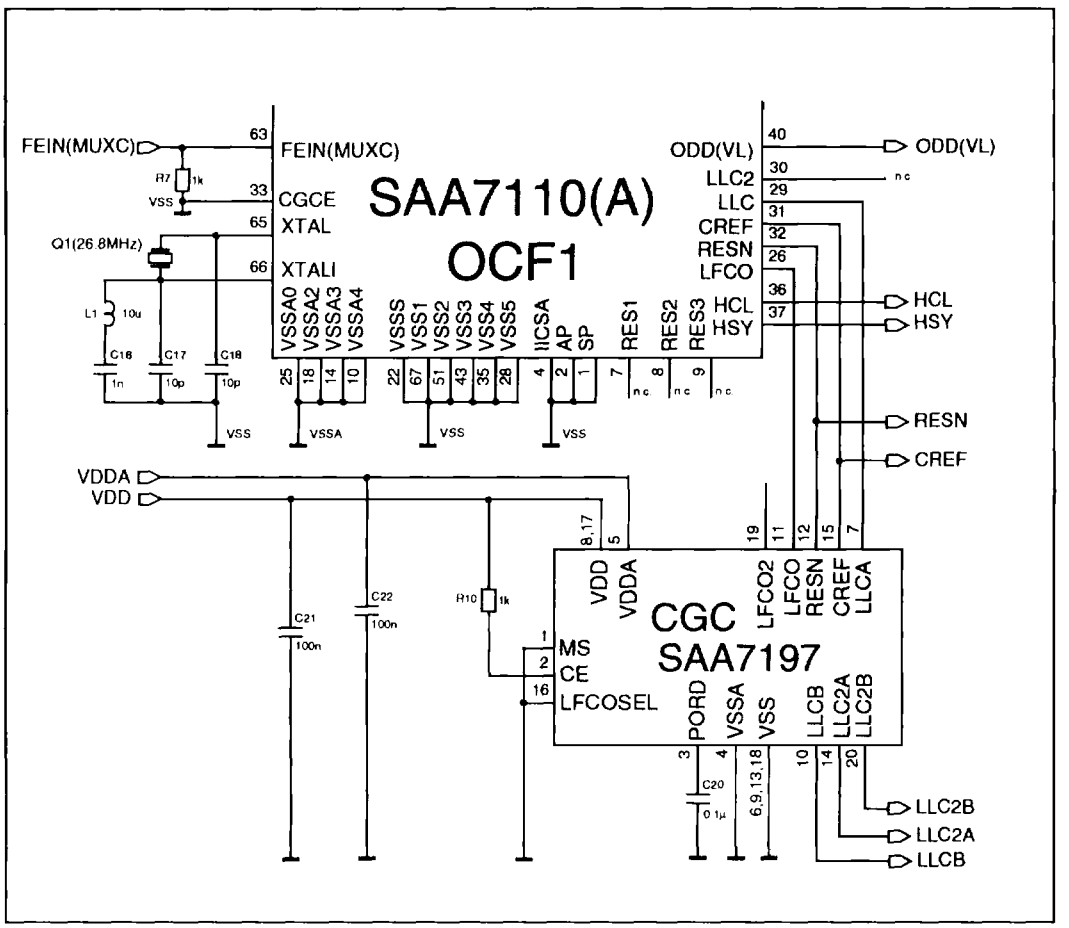
FIGURE 23. OCF1 APPLICATION SHEET



Note: Unused analog inputs should be not connected!

21.1 APPLICATION WITH EXTERNAL CGC

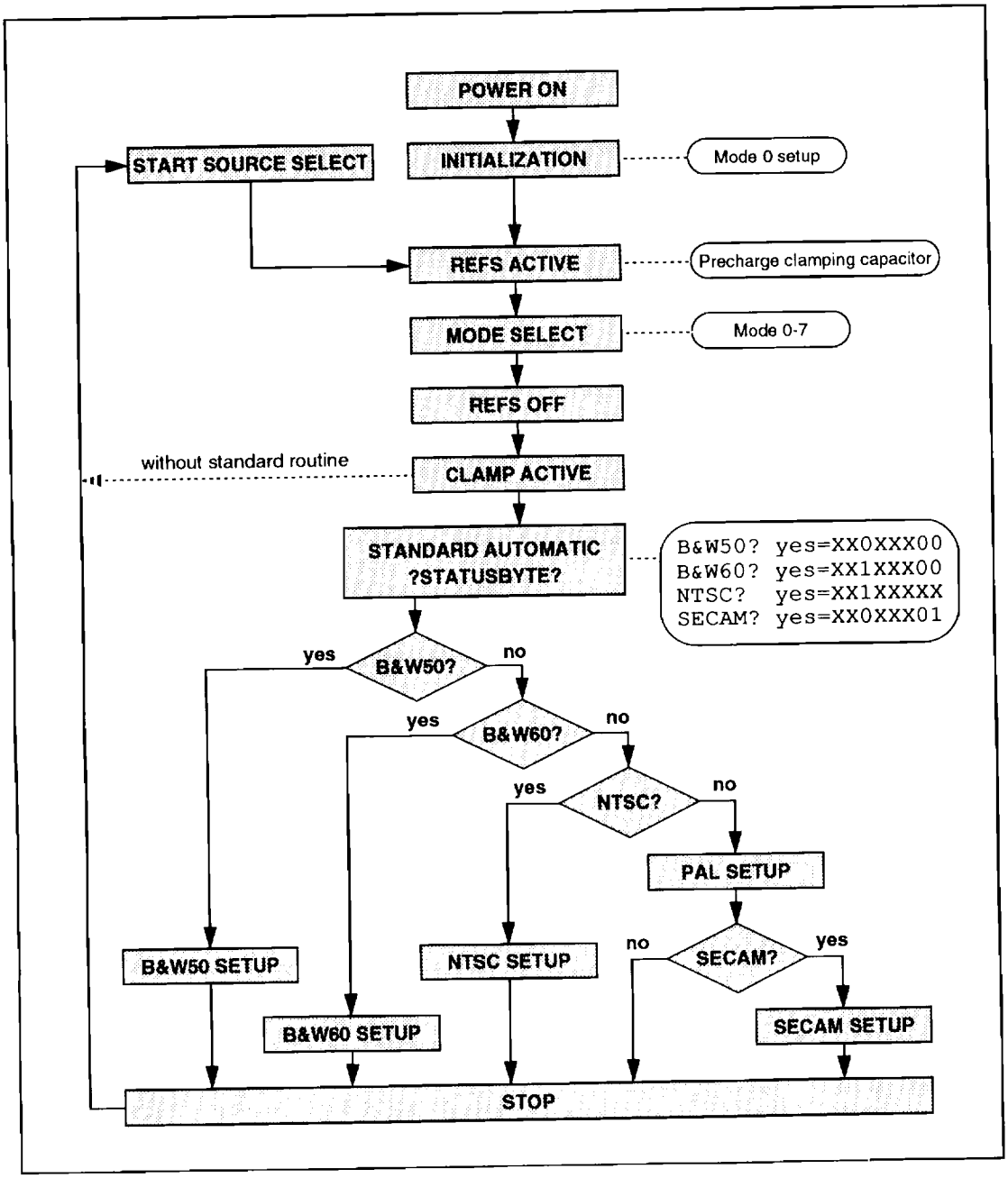
FIGURE 24. APPLICATION WITH EXTERNAL CGC



The OCF1 supports for special applications the use of an external Clock Generator Circuit (CGC, SAA7197). For normal operation the build in CGC fulfills all requirements.

22. STARTUP, SOURCE SELECT AND STANDARD DETECTION FLOW EXAMPLE

FIGURE 25. SOFTWARE FLOW EXAMPLE



MODE 0 STARTUP and STANDARD Procedure

```
SLAVE 9C            !OCF1 NTSC-setup
SUB 00 WRITE
4C 3C 0D EF BD F0 00 00
F8 F8 60 60 00 06 18 90
00 2C 40 46 42 1A FF DA
F0 8B 00 00 00 00 00 00
D9 17 40 41 80 41 80 4F
FE 01 CF 0F 03 01 81 03
44 75 01 8C 03
SUB 21 WRITE 16     !REFS OFF CLAMP AKTIV

READ 1              !Status?

#STANDARD
IF 1 @XX0XXX00      !NO COLOR
THEN GOTO BW_50Hz
ENDIF
IF 1 @XX1XXX00      !NO COLOR
THEN GOTO BW_60Hz
ENDIF
SUB 06 WRITE 00
ENDIF
IF 1 @XX1XXXXX      !60Hz
THEN GOTO NTSC
ENDIF
IF 1 @XX0XXXXX      !50Hz
THEN GOTO PAL
ENDIF

#BW_50Hz
PRINT "BLACK&WHITE"
SUB 06 WRITE 80
SUB 2E WRITE 9A     !VBPS
GOTO STOP

#BW_60Hz
PRINT "BLACK&WHITE"
SUB 06 WRITE 80
SUB 2E WRITE 81     !VBPS
GOTO STOP

#NTSC
SUB 0D WRITE 06     !SECS -> 0
SUB 11 WRITE 2C     !CHCV
SUB 2E WRITE 81     !VBPS
PRINT "NTSC"
GOTO STOP

#PAL
SUB 0D WRITE 06     !SECS -> 0
SUB 11 WRITE 59     !CHCV
SUB 2E WRITE 9A     !VBPS
PAUSE %150          !150ms
IF 1 @XX0XXX01
THEN GOTO SECAM
ELSE PRINT "PAL"
GOTO STOP

#SECAM
SUB 0D WRITE 07     !SECS -> 1
PRINT "SECAM"
GOTO STOP

#STOP
```

MODE 0 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 0
SUB 20 WRITE D9     !AI21 ACTIVE
SUB 21 WRITE 17     !REFS ON
SUB 22 WRITE 40     !AD2->LUMA and CHROMA
SUB 2C WRITE 03     !CLAMP SELECT
SUB 30 WRITE 44     !Gain AD2 active
SUB 31 WRITE 75     !AOSL -> 01b

SUB 21 WRITE 16     !REFS OFF CLAMP AKTIV
```

MODE 1 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 1
SUB 20 WRITE D8     !AI22 ACTIVE
SUB 21 WRITE 17     !REFS ON
SUB 22 WRITE 40     !AD2->LUMA and CHROMA
SUB 2C WRITE 03     !CLAMP SELECT
SUB 30 WRITE 44     !Gain AD2 active
SUB 31 WRITE 75     !AOSL -> 01b

SUB 21 WRITE 16     !REFS OFF CLAMP AKTIV
```

MODE 2 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 2
SUB 20 WRITE BA     !AI31 ACTIVE
SUB 21 WRITE 07     !REFS ON
SUB 22 WRITE 91     !AD3->LUMA and CHROMA
SUB 2C WRITE 03     !CLAMP SELECT
SUB 30 WRITE 60     !Gain AD3 active
SUB 31 WRITE B5     !AOSL -> 10b

SUB 21 WRITE 05     !REFS OFF CLAMP AKTIV
```

MODE 3 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 3
SUB 20 WRITE B8     !AI32 ACTIVE
SUB 21 WRITE 07     !REFS ON
SUB 22 WRITE 91     !AD3->LUMA and CHROMA
SUB 2C WRITE 03     !CLAMP SELECT
SUB 30 WRITE 60     !Gain AD3 active
SUB 31 WRITE B5     !AOSL -> 10b

SUB 21 WRITE 05     !REFS OFF CLAMP AKTIV
```

MODE 4 Source Select Procedure

Space for notes:

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 4
SUB 20 WRITE 7C     !AI41 ACTIVE
SUB 21 WRITE 07     !REFS ON
SUB 22 WRITE D2     !AD3->LUMA and CHROMA
SUB 2C WRITE 83     !CLAMP SELECT
SUB 30 WRITE 60     !Gain AD3 active
SUB 31 WRITE B5     !AOSL -> 10b

SUB 21 WRITE 03     !REFS OFF CLAMP AKTIV
```

MODE 5 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 5
SUB 20 WRITE 78     !AI41 ACTIVE
SUB 21 WRITE 07     !REFS ON
SUB 22 WRITE D2     !AD3->LUMA and CHROMA
SUB 2C WRITE 83     !CLAMP SELECT
SUB 30 WRITE 60     !Gain AD3 active
SUB 31 WRITE B5     !AOSL -> 10b

SUB 21 WRITE 03     !REFS OFF CLAMP AKTIV
```

MODE 6 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 80     !Y+C MODE 6
SUB 20 WRITE 59     !AI21=Y, AI42=C
SUB 21 WRITE 17     !REFS ON
SUB 22 WRITE 42     !AD2->LUMA, AD3->CHR
SUB 2C WRITE A3     !CLAMP SELECT
SUB 30 WRITE 44     !Gain AD2 active
SUB 31 WRITE 75     !AOSL -> 01

SUB 21 WRITE 12     !REFS OFF CLAMP AKTIV
```

MODE 7 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 80     !Y+C MODE 7
SUB 20 WRITE 9A     !AI31=Y, AI22=C
SUB 21 WRITE 17     !REFS ON
SUB 22 WRITE B1     !AD3->LUMA, AD2->CHR
SUB 2C WRITE 13     !CLAMP SELECT
SUB 30 WRITE 60     !Gain AD3 active
SUB 31 WRITE B5     !AOSL -> 10b

SUB 21 WRITE 14     !REFS OFF CLAMP AKTIV
```

MODE 8 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 80     !Y+C MODE 8
SUB 20 WRITE 3C     !AI41=Y, AI32=C
SUB 21 WRITE 27     !REFS ON
SUB 22 WRITE C1     !AD2->LUMA, AD3->CHR
SUB 2C WRITE 23     !CLAMP SELECT
SUB 30 WRITE 44     !Gain AD2 active
SUB 31 WRITE 75     !AOSL -> 01

SUB 21 WRITE 21     !REFS OFF CLAMP AKTIV
```