TMS27LV010A 1 048 576-BIT UV ERASABLE LOW VOLTAGE PROGRAMMABLE ROM
TMS27LV010A 1 048 576-BIT LOW VOLTAGE ONE-TIME PROGRAMMABLE ROM

SMLS113–DECEMBER 1992

- **Organization . . . 128K × 8**
- **Single 3.3-V Power Supply**
- **Operationally Compatible With Existing 1-Megabit EPROMs**
- **Industry Standard 32-Pin Dual-In-line Package (DIP), 32-Lead Plastic Leaded Chip Carrier (PLCC), and 32-Lead Thin Small Outline Package (TSOP)**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

'27LV010A-20	200	ns
'27LV010A-25	250	ns
'27LV010A-30	300	ns

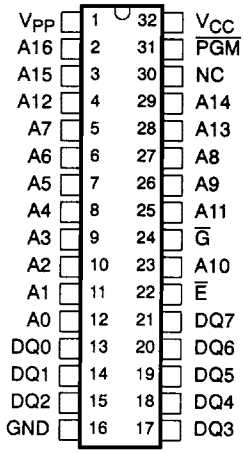
- **8-Bit Output For Use in Microprocessor-Based Systems**
- **Very High-Speed Low Voltage SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 3.6 V)**
  - **Active . . . 54 mW Worst Case**
  - **Standby . . . 0.09 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168 Hour Burn-In and Choices of Operating Temperature Ranges**

description

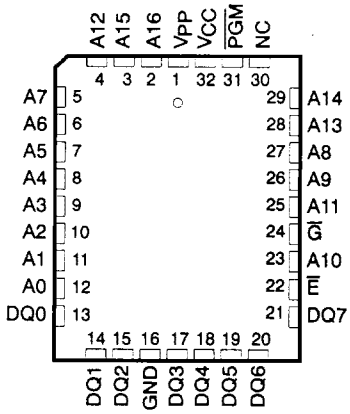
The TMS27LV010A EPROM series are 1 048 576-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27LV010A OTP PROM series are 1 048 576-bit, one-time, electrically programmable read-only memories.

J AND N PACKAGES†
(TOP VIEW)



FM PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
$\overline{PGM}$	Program
DQ0–DQ7	Inputs (programming)/Outputs
V_{CC}	3.3-V Supply
V_{PP}	12.75-V Power Supply‡

‡ Only in program mode.

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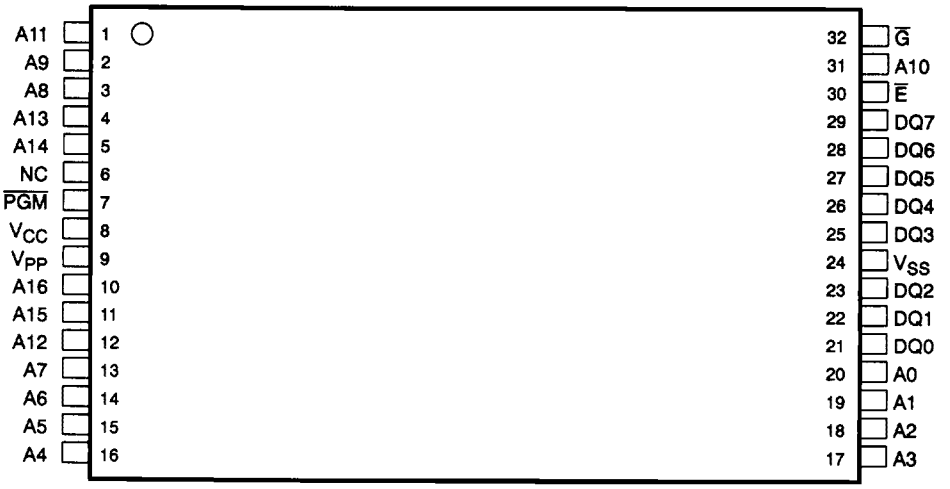
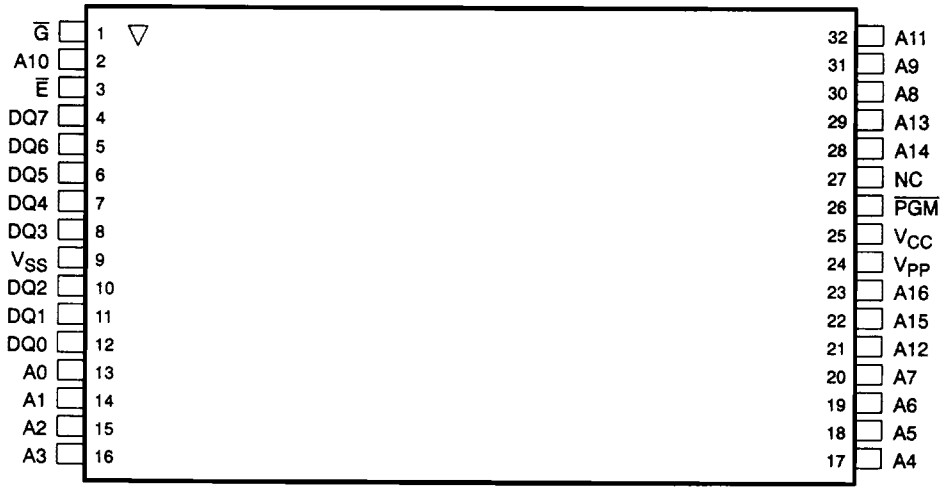
TMS27LV010A OTP PROM
DD PACKAGE†
(TOP VIEW)



TMS27LV010A OTP PROM
DU PACKAGE†
REVERSE PINOUT
(TOP VIEW)



† The packages shown are for pinout reference only.

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These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27LV010A EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27LV010A EPROM CDIP is also offered with two choices of temperature ranges, 0°C to 70°C and –40°C to 85°C (JL and JE suffixes). The TMS27LV010A EPROM CDIP is also offered with 168 hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27LV010A OTP PROM is offered in a plastic dual-in-line package (N suffix), a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix), and a 32-lead thin small-outline package (DD and DU suffixes). TMS27LV010A OTP PROM is offered with two choices of temperature ranges of 0°C to 70°C (NL, FML, DDL, and DUL suffixes) and – 40°C to 85°C (NE, FME, DDE, and DUE suffixes). (See table below.)

TMS27LV010A	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HOUR BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
EPROM	JL	JE	JL4	JE4
OTP PROM	FML	FME	FML4	FME4
	NL	NE	NL4	NE4
	DDL	DDE	DDL4	DDE4
	DUL	DUE	DUL4	DUE4

These EPROMs and OTP PROMs operate from a single 3.3-V supply (in the read mode), thus are ideal for use in portable systems. One other 12.75-V supply is needed for programming. All programming signals are TTL level. These devices are programmable using the Low Voltage SNAP! Pulse programming algorithm. The Low Voltage SNAP! Pulse programming algorithm uses a V_{PP} of 12.75 V and a V_{CC} of 5 V for a nominal programming time of thirteen seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

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operation

The seven modes of operation are listed in the following table. The read mode requires a single 3.3-V supply. All inputs are TTL level except for V_{PP} during programming (12.75 V for Low Voltage SNAP! Pulse), and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	D7

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

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read/output disable

When the outputs of two or more TMS27LV010A EPROMs or TMS27LV010A OTP PROMs are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27LV010A EPROM and OTP PROM is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 15 mA to 250 μA by applying a high TTL input on $\overline{E}$ and to 25 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27LV010A EPROM)

Before programming, the TMS27LV010A EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27LV010A EPROM, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

initializing (TMS27LV010A OTP PROM)

The one-time programmable TMS27LV010A OTP PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

Low Voltage SNAP! Pulse programming

The TMS27LV010A EPROM is programmed using the TI Low Voltage SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of thirteen seconds. Actual programming time will vary as a function of the programmer used.

The Low Voltage SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 12.75 V, V_{CC} = 5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$. Data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the Low Voltage SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 3.3\ V \pm 10\%$.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 12.75 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

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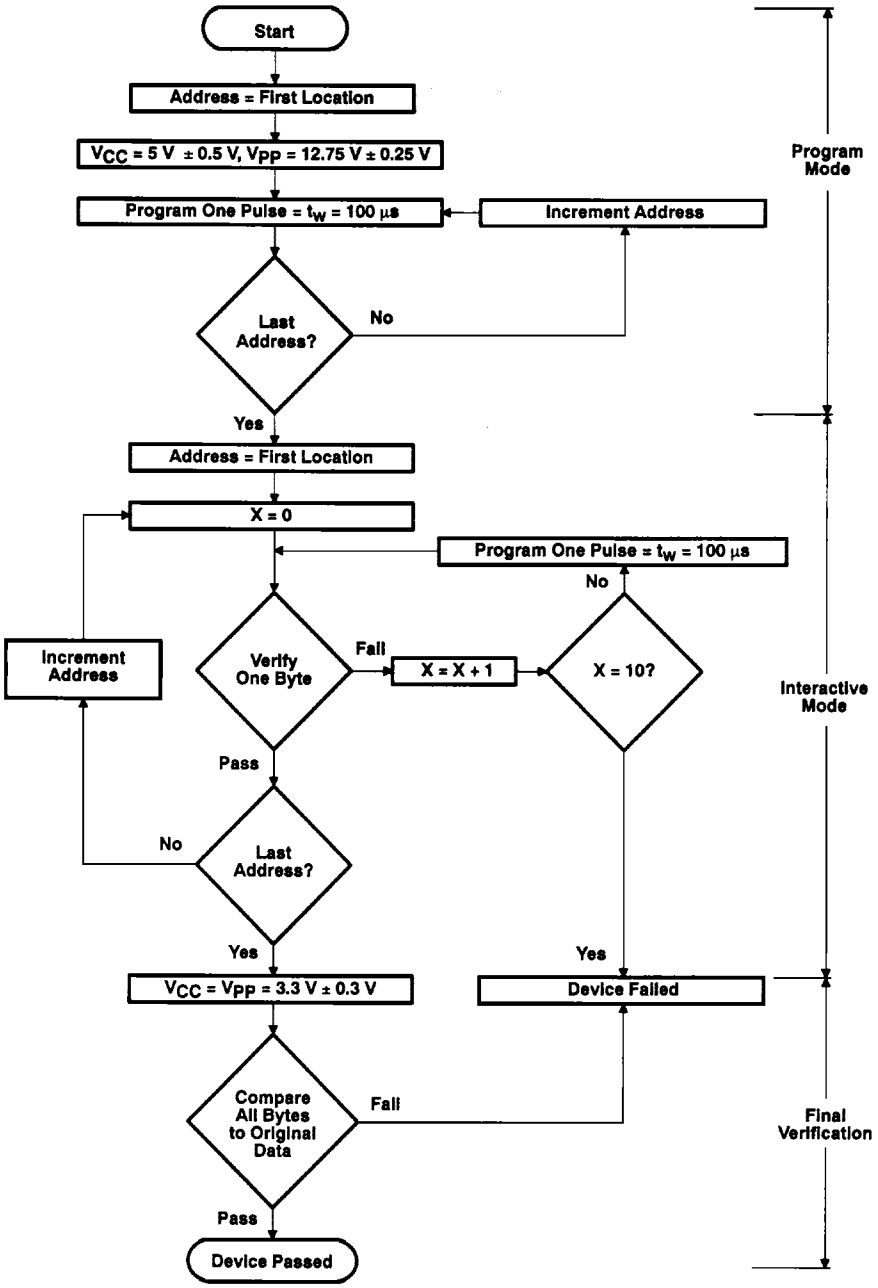


Figure 1. Low Voltage SNAP! Pulse Programming Flowchart

signature mode

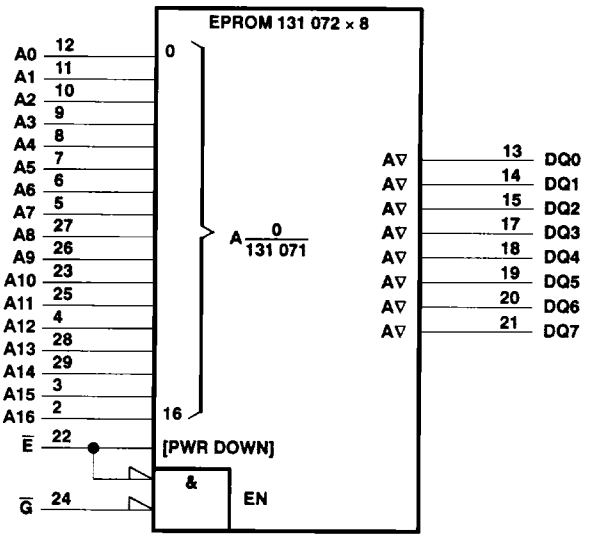
The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All addresses must be held low. The signature code for these devices is 97D7. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code D7 (Hex), as shown by the signature mode table below.

signature mode†

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	1	0	1	0	1	1	1	D7

† $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_H, A10–A16 = V_{IL}, $V_{PP} = V_{CC}$.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. J package illustrated.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} ..... – 0.6 to 14 V
Input voltage range, All inputs except A9 ..... – 0.6 to VCC + 1 V
A9 ..... – 0.6 to 13.5 V
Output voltage range, with respect to VSS (see Note 1) ..... – 0.6 V to VCC + 1 V
Operating free-air temperature range (JL, NL, FML, DDL, and DUL) ..... 0°C to 70°C
Operating free-air temperature range (JE, NE, FME, DDE, and DUE) ..... – 40°C to 85°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS27LV010A-20 TMS27LV010A-25 TMS27LV010A-30			UNIT
			MIN	TYP	MAX	
V_{CC} Supply voltage	Read mode (see Note 2)		3	3.3	3.6	V
	Low Voltage SNAP! programming algorithm		4.5	5	5.5	V
V_{PP} Supply voltage	Read mode (see Note 3)		$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	V
	Low Voltage SNAP! Pulse programming algorithm		12.5	12.75	13	V
V_{IH} High-level dc input voltage		TTL	2.0		$V_{CC}+0.5$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.5$	
V_{IL} Low-level dc input voltage		TTL	−0.5		0.8	V
		CMOS	−0.5		GND+0.2	

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. During programming, V_{PP} must be maintained at 12.75 V ± 0.25 V.

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electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −100 µA	V_{CC}−0.2		V
			I_{OH} = −2 mA	2.4		
V_{OL}	Low-level output voltage		I_{OL} = 2 mA		0.4	V
			I_{OL} = 100 µA		0.2	
I_I	Input current (leakage)		V_I = 0 to 3.6 V		±1	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 3.6 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 12.75 V		30	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{E}$ = V_{IH}, V_{CC} = 3.6 V		250	µA
		CMOS-input level	$\overline{E}$ = V_{CC} ± 0.2 V, V_{CC} = 3.6 V		25	
I_{CC2}	V_{CC} supply current (active) (output open)		$\overline{E}$ = V_{IL}, V_{CC} = 3.6 V, $\overline{G}$ = V_{IH}, F = 5 MHz		15	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		4	8	pF
C_o	Output capacitance	V_O = 0, f = 1 MHz		6	10	pF

† Capacitance measurements are made on sample basis only.
‡ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'27LV010A-20		'27LV010A-25		'27LV010A-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input t_r ≤ 20 ns, Input t_f ≤ 20 ns		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first§		0	35	0	35	0	35	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		ns

§ Value calculated from 0.5-V delta to measured output level.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing waveform).
5. Common test conditions apply for t_{dis} except during programming.

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switching characteristics for programming: V_{CC} = 5 V and V_{PP} = 12.75 V (Low Voltage SNAP! Pulse), T_A = 25°C (see Note 4)

	PARAMETER	MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 5 V and V_{PP} = 12.75 V (Low Voltage SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	Low Voltage SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing waveform).

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PARAMETER MEASUREMENT INFORMATION

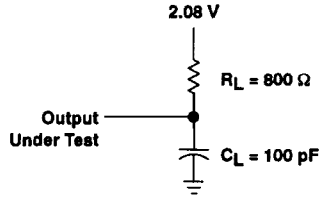
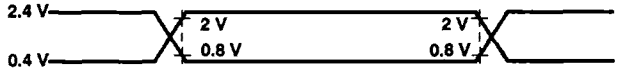


Figure 2. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

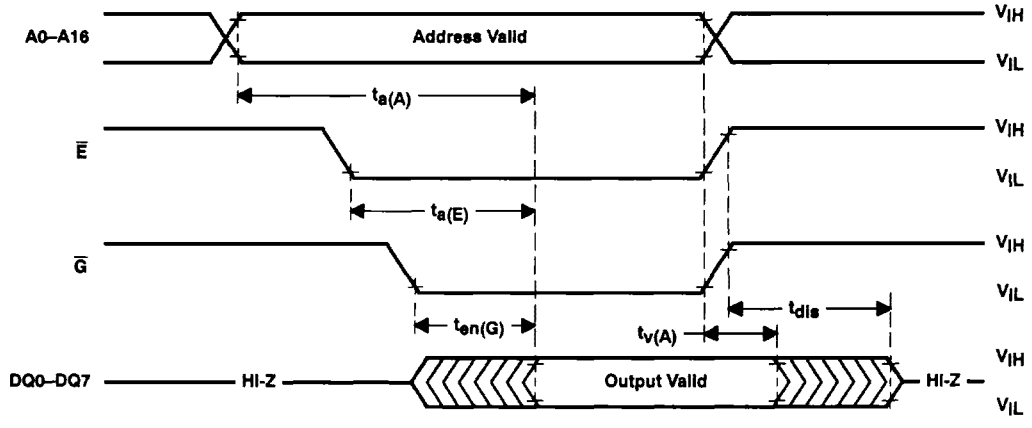


Figure 3. Read Cycle Timing

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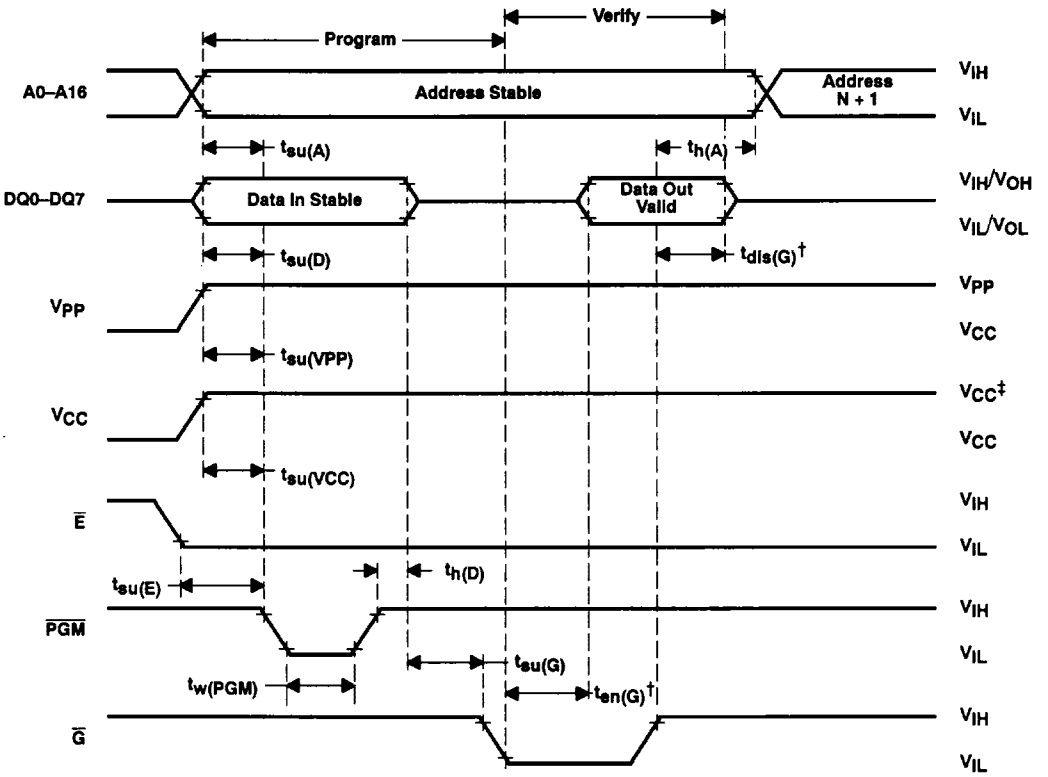
PROGRAMMING INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 12.75-V V_{PP} and 5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (Low Voltage SNAP! Pulse Programming)

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