82485
SECOND LEVEL CACHE CONTROLLER FOR THE i486™ MICROPROCESSOR

- **High Performance**
  - **— Zero Wait State Access on Cache Hit**
  - **— One Clock Bursting**
  - **— Two-Way Set Associative**
  - **— Write Protect Attribute Per Tag**
  - **— Start Memory Cycles in Parallel**
- **Easy to Use**
  - **— Matches i486™ Microprocessor Bus Timing**
  - **— Supports Invalidation Cycles**
  - **— Maintains Memory on Writes**
- **High Integration**
  - **— Single Chip Tag RAM and Controller**
  - **— No Logic Needed for CPU and Cache Connection**
  - **— Maps Full 4 Gigabyte Address Space**
- **Flexible System Configurations**
  - **— Supports 64K or 128K Cache Memory Per Controller**
  - **— Allows Multiple Controllers for Larger Cache Size**
  - **— Supports Non-Cacheable Memory Areas**

The 82485 is a second-level cache controller designed to improve the performance of i486™ Microprocessor systems. One 82485 cache controller supports 64K or 128K bytes of second level cache memory that maps to the entire 4 Gigabytes of the i486 microprocessor address space. The controller is completely software transparent. Several controllers may be cascaded to provide larger cache sizes. One controller plus SRAMs provides a 64K or a 128K cache. External EPROM can be cached yet remain write protected. The 82485 is fully compatible with the i486 microprocessor. All i486 CPU bus cycles and timings are supported.

A complete, optional second level cache controller using the 82485 is available as the 485Turbocache Module from Intel (data sheet order number 240722).

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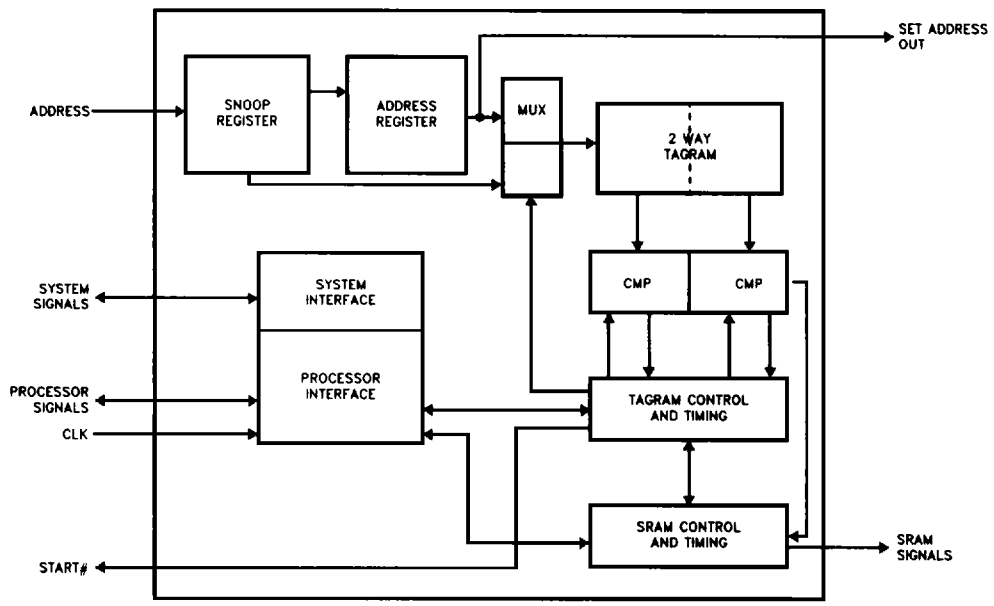
82485 Internal Block Diagram



For the complete data sheet on this device, contact Intel's Literature Distribution Dept., (800) 548-4725.

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