Intel® IXF3204 Quad T1/E1/J1 Framer with Intel® On-Chip PRM

Datasheet

Product Features

- Quad T1/E1/J1 Framer
- Software selectable and fully independent T1/E1/J1 operation
- Support for T1/E1/J1 standards:
  - —T1: T1-SF, T1-ESF, Lucent* SLC®96
  - —E1: PCM30, G.704, G.706, G.732 ISDN PRI
  - —J1: J1-SF and J1-ESF
- Programmable transmit/receive slip buffers
- On-chip Intel® Performance Report Messaging per ANSI T1.231, T1.403, and ITU G.826
- 24 fully independent HDLC controllers with 128-byte transmit/receive FIFOs support GR-303 and V5.1/5.2 standards
- FDL Support:
  - —DL support for ESF per ANSI T1.403 or AT&T* TR54016 (T1/J1)
  - —DDL bit access for Lucent SLC®96
  - —Sa bit access for E1
- 256-PBGA package, 17 mm x 17 mm
- Operating temperature -40 °C to 85 °C
- Diagnostics:
  - —BERT generators and analyzers for extensive on-chip error testing at DS-0, DS-1, and E1 rates
  - —Pseudo-random and programmable bit-sequence generator and monitoring
  - —Per-link diagnostics and loopbacks
- Programmable system backplane data rates at 1x/2x/4x/8x of T1/E1 data rates for support of MVIP, H-MVIP, H.100, and CHI
- Support for fractional T1/E1
- Signaling:
  - —Support for T1/E1 CAS and T1/E1 CCS
  - —Signaling state-change indication
  - —Signaling freeze/debounce per DS-1
  - —Signaling force per DS-0
- Red/Yellow/AIS alarm indication
- Intel®/Motorola* 8-bit processor interface
- Industry-standard P1149.1 JTAG test port
- Low-power 1.8/3.3-V CMOS technology with 5-V tolerant I/Os

Applications

- Integrated Multi-service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for Asynchronous Transfer Mode (also known as ‘IMA’)
- Frame-relay access devices
- Channel service unit (CSU) / Data Service Unit (DSU) equipment
- Wireless base stations, radio network controllers
- Routers

Document Number: 278594
Revision Number: 003
Revision Date: December 2, 2003

Contents

Figures

Tables

Revision History

IXF3204 Datasheet - Revision Number 003 Revision Date: December 2003	
Page Number	**Description**
183	Section 24.1, “Motorola Processor Timing”. Table 67 through Table 70 table text changed.
187	Section 24.2, “Intel® Processor Timing”. • The table text changed for the following tables: Table 71 and Table 72 • The Note changed for the following figures: Figure 55 and Figure 56
191	Chapter 27.0, “Package Markings”. New chapter added.
192	Chapter 28.0, “Product and Order Information”. New chapter added.

IXF3204 Datasheet - Revision Number 002 (Sheet 1 of 7) Revision Date: June 2003	
Page Number	**Description**
Throughout	References to “Bellcore” changed to “Telcordia”.
19	New chapter, Chapter 1.0, “Introduction to Document”.
20	Chapter 1.0, “Product Summary” changed to become Chapter 2.0.
20	Old Section 1.1, “Description”, changed to new Section 2.1, “Description”. Text was reorganized and rewritten and includes text previously on the “Product Features” front page.
22	Old Figure 2, “LXT3104/IXF3204 System Interface” became new Figure 1, “Intel® IXF3204 Framer System Backplane Block Diagram”.
23	Old Figure 1, “IXF3204 Block Diagram” changed to new Figure 2, “Intel® IXF3204 Framer High-Level Block Diagram”. Arrows in figure changed.
23	Old Figure 3, “IXF3204 Detailed Block Diagram”, became Figure 3, 'Intel® IXF3204 Framer Detailed Block Diagram”.
-	Deleted un-numbered section titled “Applications”.
24	Added new section heading, Section 2.2, “Conventions and Terminology”.
24	Old Section 1.3, “T1/E1 Nomenclature”, changed to Section 2.2.1, “Conventions and Terminology for T1/E1”. Text changed.
25	Old Section 1.4, “IXF3204 Nomenclature”, changed to Section 2.2.2, “Conventions and Terminology for IXF3204 Framer”. Text changed.
25	Old Section 1.2, “Reference Material”, moved and changed to Section 2.3, “Related Documents”. Text in table changed.
26	Chapter 2, “IXF3204 Signal Descriptions” changed to Chapter 3.0, “Signal Descriptions”, and text changed throughout.
26	New Section 3.1, “Signal Groupings” added. Removed package information and replaced with a reference to Chapter 27.0, “Mechanical Specifications”.
26	Old Figure 4, “IXF3204 Logical Symbol” changed to new Figure 4, “Intel® IXF3204 Framer Signal Groupings”. Included in the microprocessor interface signals I/M#, MTYPE, and RESETB.
27	Section 2.1, “Ball Description”, changed to Section 3.2, “Ball Descriptions”. Table 1, “IXF3204 Ball Description”, was divided into tables that matched the signal groupings in Figure 4. Re-numbered tables start with Table 2.
37	Chapter 3, “Feature Set”, changed to Chapter 4.0, “Feature Set and Indicators”.

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37	New Section 4.1, “Feature Set”, added.
37	Old Table 2, “Line and Framing”, changed to Table 10, “Line and Framing Features”. Text changed.
40	Old Table 3, “Slip Buffers”, changed to Table 11, “Slip Buffer Features”. Text changed.
40	Old Table 4, “Signaling” changed to new Table 12, “Signaling Features”. Text changed.
41	Old Table 5, “T1 Performance Monitoring”, changed to new Table 13, “T1 Performance Monitoring Features”. Text changed.
43	Old Table 6, “E1 Performance Monitoring”, changed to new Table 14, “E1 Performance Monitoring Features”. Text changed.
43	Old Table 9, “Data Link”, moved to Section 4.1, “Feature Set” and became new Table 15, “Data-Line Features”. Text changed.
45	Old Table 10, “Embedded HDLC Controller”, moved to Section 4.1, “Feature Set” and became new Table 16, “Embedded High-Level Data-Link Controller Features”. Text changed.
46	Old Table 11, “Interfaces”, moved to Section 4.1, “Feature Set” and became new Table 17, “Interface Features”. Text changed.
47	Old Table 12, “Maintenance/Diagnostics”, moved to Section 4.1, “Feature Set” and became new Table 18, “Maintenance/Diagnostics Features”. Text changed.
48	Added new Table 19, “Pattern Generator/Receiver and BERT Features.
49	Added new numbered section, Section 4.2, “Indicators”, and changed text that starts section. Text in tables changed.
49	Old Table 7, “Main T1 Indicators”, changed to new Table 20. Text changed.
51	Old Table 8, “Main E1 Indicators”, changed to new Table 21. Text changed.
53	Old Chapter 4, “Initialization” changed to Chapter 5.0, “Initialization, Reset, and Interrupts”.
53	Added a new numbered section, Section 5.1, “Initialization”. Text changed.
53	Old Section 4.1, “Software Reset”, changed to new Section 5.2, “Reset”. Text changed.
53	Old Section 4.2, “Interrupt Handling”, changed to new Section 5.3, “Interrupt Handling”. Text and figures changed throughout this section and subsections.
55	Old Figure 6, “Interrupt Mapping”, changed to new Figure 6, “Intel® IXF3204 Framer Interrupt Handling - Register STB”. Figure changed.
56	Chapter 5, “T1 Framer” changed to Chapter 6.0, “T1 Framers”. Throughout, relabelled sections with “T1” so that on-line readers can better orient themselves to where they are within the document. Text changed throughout chapter.
58	Old Section 5.1.2, “Zero Code Suppression”, changed to new Section 6.1.2, “T1 Zero Code Suppression”. Text changed.
59	Old Section 5.2.1, “Alarm Indication Signal”, changed to new Section 6.2.1, “T1 Alarm Indication Signal”. Text changed.
60	Old Section 5.3, “BPV Error Insertion” changed to new Section 6.3, “T1 Insertion of Line Errors”. Text changed.
61	Old Section 5.4, “T1 Framing” changed to new Section 6.4. Text and table changed.
62	Old Section 5.5, “Superframe (SF)/D4 Format” changed to new Section 6.5, “T1 Superframe”. Text changed.
63	Old Figure 7, “SF Frame Structure” changed to “T1 SF Frame Structure”. In the figure, changed SF-96 to SF-12.
64	Old Section 5.6.1, “Description”, changed to new Section 6.6.1, “T1 SLC®96 Description”. Table 24, “T1 SLC®96 Frame Structure” (previously titled “SLC-96 Framing”) moved to this section from old Section 5.6.2, “Framing Algorithm”.
67	Old Figure 8, “SF Structure”, changed to new Figure 8, “T1 SLC®96 Frame Structure”.
68	Old Section 5.7, “ESF” changed to new Section 6.7, “T1 Extended SuperFrame”. Text changed.

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68	Old Section 5.7.2, “CRC-6 Procedures” changed to new Section 6.7.2, “T1 ESF CRC-6 Procedures”. Text changed.
69	Added new Section 6.7.2.1, “T1 ESF CRC-6 Options on the Transmit Side”, and moved here text from old Section 5.7.2, “CRC-6 Procedures”. Text changes include the following: “T1 through E6” changed to “C1 through C6.”
69	Added new Section 6.7.2.2, “T1 ESF CRC-6 Options on the Receive Side”, and moved here text from old Section 5.7.2, “CRC-6 Procedures”.
72	Old Section 5.8.1, “False Framing Protection”, changed to Section 6.8.1, “T1 False Framing Protection”. Table 26, “T1 False Framing Protection”, Row “SLC®96” text changed.
72	Old Section 5.8.2, “Maximum Average Reframe Time”, changed to new Section 6.8.2, “T1 Maximum Average Reframe Time”. Text changed.
73	Old Table 19, “Out Of Frame (OOF) Criteria Options changed to new Table 28, “T1 Out Of Frame Criteria Options”. Footer Note 1 text changed.
75	Old Section 5.11, “T1 Alarms” changed to new Section 6.11, “T1 Alarm Overview””. Moved information previously in the bullets to new sections that discuss the alarms.
75	Old Section 5.11.1, “Red Alarm Detection” changed to new Section 6.12, “T1 Red Alarm”. Changed reference to ‘N’ number to ‘M’ number. Old sections on the topic of J1 Yellow alarms removed from this section.
76	New section heading added, Section 6.13, “T1 Yellow Alarm”.
76	Old Section 5.11.2, “Yellow Arm Detection”, changed to new Section 6.13.1, “T1 Yellow Alarm Detection”, and text changed.
76	Old Section 5.11.3, “Yellow Alarm Transmission”, changed to new Section 6.13.2, “T1 Yellow Alarm Transmission”, and text changed.
77	New section heading added, Section 6.14, “T1 Blue Alarm”.
77	Old Section 5.11.4, “Blue Alarm Detection”, changed to new Section 6.14.1, “T1 Blue Alarm Detection”. Text changed.
77	Old Section 5.11.5, “Blue Alarm Transmission”, changed to new Section 6.14.2, “T1 Blue Alarm Transmission”. Text changed.
78	Old Section 6.1, “J1 Operation”, changed to new Section 7.1, “J1 Frame Operations”. Text changed.
78	Old section heading, Section 6.2, “Multiframe Structures”, deleted. Text from this section moved to new Section 7.1, “J1 Frame Operations”.
79	Old section 6.2.1, “12-Frame Multiframe”, changed to new Section 7.1.1, “J1 Frame Operation - Modified 12-Frame Multiframe”. Text changed.
80	Old section 6.2.2, “24-Frame Multiframe”, changed to new Section 7.1.2, “J1 Frame Operation - Modified 24-Frame Multiframe”. Text changed.
81	Added new Section 7.2, “J1 Alarm Overview”, and subsequent subsections. Information came from old Chapter 5, “T1 Framer”.
81	Added new Section 7.3, “J1 Yellow Alarm”, and subsequent subsections. Information came from old Chapter 5, “T1 Framer” and old sections 5.11.2.2, “J1 SF”, 5.11.2.4, “J1 ESF FDL”, 5.11.3.2, “J1 SF”, and 5.11.3.4, “J1 ESF FDL”.
85	Old Section 7.2.4, “Bipolar Violation (BPV) Error Injection”, changed to new Section 8.3, “E1 Insertion of Line Errors” and text changed.
89	Old section 7.5.1, “Description”, changed to new Section 8.6.1, “E1 CRC-4 Multiframe Description”. Text changed, including information on the NFAS frames.
90	Old section 7.5.3, “CRC Interworking”, changed to new Section 8.6.3, “E1 CRC-4 Multiframe Interworking” and text changed.
91	Old section 7.5.6, “CRC Multiframe Transmission”, changed to new Section 8.6.6, “E1 CRC-4 Multiframe Transmission”, and text changed.

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94	Old Section 7.7, “Simultaneous CAS and CRC Multiframes”, changed to new Section 8.9, “E1 Simultaneous CAS and CRC Multiframes”. Deleted the numbered section headings, Section 7.7.1, “Description” and Section 7.7.2, “Transmission”. Text changed throughout Section 8.9, “E1 Simultaneous CAS and CRC Multiframes”.
95	Old Section 7.8, “E1 Alarms” changed to new Section 8.10, “E1 Alarm Overview”. Moved information previously in the bullets to the sections that discuss the alarms.
97	Old Section 7.8.5, “AIS Alarm”, changed to new Section 8.15, “E1 Alarm: AIS” and text changed.
100	Old Section 7.11.1, “Sa/Si Bit Reception and Codewords”, changed to new Section 8.18.1, “E1 Sa/Si Bit Reception and Codewords”, and text changed.
101	Old Section 7.11.2, “Sa/Si Transmission and Codewords”, changed to new Section 8.18.2, “E1 Sa/Si Transmission and Codewords”, and text changed.
101	Old Section 7.12, “Fractional E1” changed to new Section 8.19, “Fractional E1 Mode”. Text changed.
103	Old Section 9.1, “Signaling Overview”, changed to new Section 10.1, “Signaling Overview”, and text changed.
104	Old Section 9.2.1, “T1 Robbed-Bit Signaling”, changed to new Section 10.2.1, “T1 Channel-Associated Signaling: Robbed Bit”. Text changed and Table 37, “T1 Robbed-Bit Signalling Use”, changed.
105	New Table 38, “SLC®96 Nine-State Signaling Mode Bit Mapping”.
105	New numbered Section 10.2.2, “T1 Channel-Associated Signaling: Per Time-Slot Enable”.
107	Old Section 9.4, “Signaling Access”, changed to new Section 10.4, “Signaling Access”. Deleted the old numbered Section 9.4.1, “Dedicated System Backplane Signaling Ports” and included this information under new Section 10.4, “Signaling Access”. Text changed.
104	Old Section 9.5, “Signaling Processing Options”, changed to new Section 10.5, “Signaling Processing Options”. Text in old Section 9.5.2.1, “Signaling Force” moved to under new Section 10.5, “Signaling Processing Options”.
109	Old Chapter 10, “Alarm Handling”, changed to new Chapter 11.0, “Alarm Processing”. Text under chapter heading moved to new Section 11.1, “Alarm Detection and Reporting”.
110	Old Section 10.1, “Alarm Integration”, changed to new Section 11.2, “Alarm Integration”, and text changed.
111	Old Section 10.2, “Alarm Handling”, changed to new Section 11.3, “Alarm Handling and Consequent Actions”. Text changed.
111	Old Table 29, “Consequent Actions”, changed to new Table 41, “Consequent Actions”. Text changed.
114	Old Section 11.2, “Functional Description”, changed to new Section 12.2, “FDL Module Messages”, and text changed.
114	Old Section 11.3, “On-Chip Performance Report Monitoring (PRM)”, changed to Section 12.3, “FDL Performance Report Messaging”, and text changed.
115	Old Section 11.4, “Derived Data Link (DDL)”, changed to new Section 12.4, “FDL Derived Data Link Message”, and text changed.
116	Old Section 11.7, “Bit Oriented Protocol (BOP) Module”, changed to new Section 12.6, “FDL Bit-Oriented Protocol Module for Messages”.
117	Old Section 11.6, “Common Channel Signaling (CCS)”, changed to new Section 12.7, “FDL Common Channel Signaling Messages”, and text changed.
117	Old Section 11.8, “Interactions with the Facility Data Link (FDL) Module”, changed to new Section 12.8, “FDL Module Interactions”. Changed the order of subsections.
118	Old Section 11.8.4, “Transmission of On-Chip PRM Messages” moved to new Section 12.8.1, “Interactions with Performance Report Monitoring”, and text changed.

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120	Old Section 11.8.1, “Reception of MOP Messages” changed to new Section 12.8.2, “Interactions with Message-Oriented Protocol Module”. Text previously in old section concerning priority of MOP, PRM, and BOP messages moved to new Section 12.8, “FDL Module Interactions”.
120	Old Figure 14, “Reception of a BOP” became new Figure 14, “Reception of a BOP Message”. Figure changed.
120	Old Section 11.8.6, “Transmission of BOP”, moved to new Section 12.8.3, “Interactions with Bit-Oriented Protocol”, and text changed.
122	Old Chapter 12, “Slip Buffers”, changed to new Chapter 13.0, “Slip Buffers”. Text was reorganized and changed.
127	Old Section 13.3.1.1, “MVIP Bus”, divided into new numbered Section 14.3.1, “MVIP Bus” and new numbered Section 14.3.2, “H-MVIP Bus”. Text and figures changed in Section 14.3.2.
128	Old Section 13.3.1.3, “1.544 Mbps ST Bus”, changed to new Section 14.3.4, “1.544-MHz ST Bus”. Figure changed.
129	Old Section 13.3.1.4, “2.048 Mbps ST Bus”, changed to new Section 14.3.5, “2.048-MHz ST Bus”.
129	Old Section 13.3.1.5, “CHI Bus”, changed to new Section 14.3.6, “CHI Bus”. Position of text referring to Figure 23, “CHI Bus Data-Only Stream at 1x”, was placed before (instead of after) the figure. Text and figure changed.
131	Old Section 13.3.3, “Concentration Modes”, changed to new Section 14.5, “Backplane Concentration Modes”. Text changed in the last sentence.
131	Old Section 13.3.5, “Byte Enforcements”, changed to new Section 14.7, “Backplane Byte Enforcements”. Added information on “Specific value” and other text changed.
135	New numbered Section 15.1, “Clock and Frame-Pulse Timing Configuration”. Text and figure changed.
138	Old Section 14.12, “Rx Backplane Multi-Frame Pulse Configurations”, and old Section 14.13, “TxBackplane Multi-Frame Pulse Configurations”, merged into new Section 15.11, “Rx and Tx Backplane Multiframe Pulse Configurations”, and text changed.
143	Old Section 15.2, “Payload LoopBack (PLB) Mode”, changed to new Section 16.2, “Payload Loopback”, and text changed.
145	Old Chapter 16, “Bit Error Rate Tester (BERT)”, changed to new Chapter 17.0, “Bit Error Rate Tester”. Text immediately following the chapter header moved to new Section 17.1, “BERT Description”, and text changed.
146	Old Section 16.1, “BERT Analyzer”, changed to new Section 17.2, “BERT Analyzer”, and text changed.
147	Old Figure 36, “BERT Analyzer”, changed to new Figure 37, “BERT Analyzer”, and figure changed.
148	Old Figure 37, “BERT Generator”, changed to new Figure 38, “BERT Generator”, and figure changed.
149	Old Section 16.3, “Supported Patterns”, changed to new Section 17.4, “Supported BERT Patterns”. Added new Table 45, “Supported Patterns” to list information not previously in a tabular format.
151	Old Chapter 17, “HDLC Controller”, changed to new Chapter 18.0, “High-Level Data Link Controller”. Text immediately following the chapter header changed.
152	Old Section 17.2, “Functional Description”, changed to new Section 18.2, “HDLC Functional Description”. Text that starts with the words “Messages are signals conforming to an HDLC protocol...” moved to a new Section 18.2.1, “HDLC Protocols”. Text changed. Old Figure 38, “HDLC Frame Format” changed to new Figure 39, “HDLC Protocol Frame Format”.
153	New Section 18.2.2, “HDLC Field Descriptions - LAPB, LAPD, and LAPV5”.

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154	In old Section 17.2, “Functional Description”, text that starts with the words “The EA bit indicates the final byte...” and old Figure 39, “Address Field Format for LAPD Messages”, and old Figure 40, “Address Field Format, for LAPV5 Message”, moved to a new Section 18.2.3, “HDLC Address Field Format - LAPD and LAPV5. Text and figures changed.
155	In old Section 17.2, “Functional Description”, text that starts with the words “To avoid the situation of opening...” moved to new Section 18.2.4, “HDLC Message Processing and Detection”, and text changed.
156	In old Section 17.2, “Functional Description”, text that starts with the words “An HDLC message is aborted if a sequence...” and text that starts with the words “The HDLC module can perform address matching...” moved to new Section 18.2.5, “HDLC Address Matching”, and text changed.
157	In old Section 17.2, “Functional Description”, text that starts with the words “If transparent mode is configured, then no flag checking...” moved to new Section 18.2.6, “HDLC Transparent Mode Operation”.
158	Old Section 17.3, “Reception of a Message” changed to new Section 18.3, “HDLC Message Reception Process”. Text changed.
159	Old Section 17.3.2, “Steps to Configure the HDLC Receive Path” moved to new Section 18.3.1,”Steps to Configure the Receive HDLC Path” for more accurate presentation of when processes occur. Text changed.
160	Old Section 17.3.1, “Reading a Received Message” moved to new Section 18.3.2,”Reading an HDLC Message” for more accurate presentation of when processes occur. Text changed.
161	Old Figure 42, “Reading a Received Message” changed to new Figure 43, “Receiving an HDLC Message”. Figure changed.
162	Old Section 17.4, “Transmission of a Message” moved to new Section 18.4, “HDLC Message Transmission Process”, and text changed.
164	Old Section 17.4.2, “Steps to Configure the HDLC Transmit Path” moved to new Section 18.4.1, ”Steps to Configure the HDLC Transmit Path”, for more accurate presentation of when processes occur. Text changed.
163	Old Section 17.4.1, “Sending a Message” moved to new Section 18.4.2,”Sending an HDLC Message” for more accurate presentation of when processes occur. Text changed.
164	Old Figure 44, “Sending a Message” changed to new Figure 45, “Sending an HDLC Message”. Figure changed.
165	Old Chapter 18, “Performance Monitoring moved to new Section 19.0, “Performance Monitoring”. In some cases, moved acronyms to the chapter on acronyms. Deleted other acronyms.
166	Old Section 18.1.1, “T1 Near End” changed to new Section 19.1.1, “T1 Near-End Performance Elements”, and text changed.
167	Old Section 18.1.2, “T1 Far End” changed to new Section 19.1.2, “T1 Far-End Performance Elements”, and text changed.
168	Old Section 18.2, “E1 Performance Elements”, changed to new Section 19.2, “E1 Performance Elements”. Text previously in old Section 18.2.1, “E1 Near End” and old Section 18.2.2, “E1 Far End”, moved to new Section 19.2.1, “E1 Error Ratios” and Section 19.2.2, “E1 Total Time Available and Unavailable”. Text added.
170	New Section 19.2.3, “E1 Near-End Performance Elements”.
170	New Section 19.2.4, “E1 Far-End Performance Elements”.
171	Old Section 18.3, “Generic Elements”, changed to new Section 19.3, “Generic Performance Elements”, and text changed.
172	Old Section 18.5.1, “On-Chip PRM Reception”, changed to new Section 19.5.1, “PRM Reception”. Deleted old Figure 45, “Rx On-Chip PRM Scenarios”. Text changed in section.
173	Old Chapter 19, “Host Interface”, changed to new Chapter 20.0, “Host Processor Interface”. Text under chapter heading moved to new Section 20.1, “Host Processor Configuration Modes”. New text added.

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173	Old Table 36, “Configuration Modes of the Host Interface” changed to new Table 55, “Configuration Modes for Host Processor Interface”, and table headings changed.
173	Old Section 19.1, “Access Window”, changed to new Section 20.2, “Host Processor Access Window”, and text changed.
174	Old Table 37, “Pin Names Relation Between IXF3204 and Target Processor”, changed to new Table 56, “Correspondence between Intel® IXF3204 Framer and Target Processors”.
-	Old Chapter 20, “JTAG Boundary Scan” deleted.
175	Old Table 43, “Absolute Maximum Ratings”, changed to new Table 57, “Absolute Maximum Ratings”. Values previously TBD (to be determined) now listed.
175	Old Table 44, “Operating Conditions”, changed to new Table 58, “Operating Conditions”, and some values changed.
179	Old Chapter 23.0, “System Interface Timing”, retitled to new Chapter 23.0, “System Backplane Timing”.
180	Old Figure 51, “Receive Clock Timing Diagram”, changed to new Figure 48, “System Backplane Receive Timing Diagram” and figure changed.
182	Old Figure 52, “Transmit Clock Timing Diagram”, changed to new Figure 49, “System Backplane Transmit Timing Diagram” and figure changed.
183	Old Chapter 24, “Host Interface Timing Specifications”, changed to new Section 24.0, “Host Processor Interface Timing”.
183	Old Section 24.1, “Timing Diagrams” changed to new Section 24.1, “Motorola* Processor Timing”.
187	New numbered Section 24.2, “Intel® Processor Timing”.

IXF3204 Datasheet - Revision Number 001 Revision Date: August 2002	
Page Number	**Description**
-	Initial release.

1.0 Introduction to Document

The audience for this document is design engineers. The purpose of this document is to provide design information on the Intel® IXF3204 Quad T1/E1/J1 Framer with Intel® On-Chip Performance Report Messaging.

The rest of this document is organized as follows:

Document Number: 278594
Revision Number: 003
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2.0 Product Summary

2.1 Description

Overview. The Intel® IXF3204 Quad T1/E1/J1 Framer with Intel® On-Chip Performance Report Messaging (called the 'IXF3204 framer' with 'PRM') is a four-port framer. The IXF3204 framer can be used for T1/E1/J1 and Integrated Service Digital Network (ISDN) primary-rate interfaces that operate at either 1.544 Mbps or 2.048 Mbps. Each port can be configured for either T1, E1, or J1 operation, using an Application Program Interface (API) supplied by Intel. Each of the four framers operates completely independently.

The IXF3204 framer can be used for voice and data applications, as it incorporates 24 independent high-level data-link controllers (HDLCs). The HDLCs can be allocated to any time slot in the four T1/E1/J1 links the IXF3204 framer supports, simplifying implementation of scalable Telcordia* GR-303, V5.1, and V5.2 interfaces. Each framer has a receive and transmit framer and a receive and transmit slip buffer. The IXF3204 framer supports a direct interface with the Intel® LXT3104 Quad T1/E1/J1 Long/Short Haul Line Interface Unit or other LIUs from Intel® or other manufacturers.

The IXF3204 framer has an 8-bit bus that supports interfaces to both Intel® processors and Motorola processors. The time-division multiplex (TDM) interface supports bus rates from 1.544 MHz to 16.384 MHz. Supported industry-standard buses include MVIP, H-MVIP, H.100, and CHI. The internal registers are directly addressable through the processor interface.

The IXF3204 framer provides extensive support to data-link channels such as Lucent SLC®96 Derived Data Link (DDL), Facility Data Link (FDL), National bits (the 'Sa' bits), and Common Channel Signaling (CCS).

PRM. To comply with ANSI T1.231, T1.403, and ITU G.826 specifications, the On-chip Intel® Performance Report Messaging (PRM) is used for comprehensive performance monitoring. PRM processing occurs automatically, with data stored on the IXF3204 framer. An internal database with performance-monitor units (accessible by a host processor) provides status and performance parameters already integrated and filtered according to the available configurations. As a result, the host processor can offload to the IXF3204 framer the management of parameters associated with IXF3204 framer functions. Among the standards the IXF3204 framer supports are ANSI T1.231 (T1) and ITU G.826 (E1), ETSI ETS 300 011, and ETSI ETS 300 233.

Ports. Each of the ports supports the following frame structures: T1-D4 SF, T1-ESF, T1-SLC®96, J1-12, J1-24, E1-FAS/NFAS, E1-CRC4, E1-CAS, E1-CRC4/CAS, G.704, and G.706. In addition, the ports support E1-CRC4 interworking as defined in ITU G.706.

Each port is independent in timing and format from the other ports. For plesiochronous applications (that is, applications that are almost but not quite synchronous), the IXF3204 framer provides independent two-frame-deep slip buffers in both transmit and receive directions. (For minimum-delay applications, smaller elastic store depths are available.)

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System Backplane. The system backplane can be configured for different rates and waveforms. The backplane has connections for data, signaling, and framing indications. The clock can be run at speeds of 1x, 2x, 4x, and 8x of the nominal value. The Pulse-Code Modulation (PCM) highway can be configured for various industry-standard buses such as the following:

- CT-Bus H.100 (Computer Telephony bus, H.100 specification)
- CHI (Concentration Highway Interface)
- GCI (General-Circuit Interface, a 4-wire bus interface specification developed by Alcatel*, Italatel*, GPT*, and Siemens AG*)
- H-MVIP (High-Density Multi-Vendor Integration Protocol)
- IOM (ISDN-Oriented Modular interface)
- MVIP (Multi-Vendor Integration Protocol)
- SCSA S.100 (Signal Computing System Architecture, S.100 standard)

Test and Diagnostics. Test and diagnostic functions are provided through a full set of loopbacks and a Bit Error Rate Test (BERT) module. Local loopback, dual loopback, payload loopback, line loopback, and per-time slot loopbacks are available. The BERT module can manage simultaneously either up to eight generators or up to eight analyzers. Any generator and analyzer is available for each port and can be set to any time slot or set of time slots.

Also available is subrate testing, which uses a mask to define which bits in the time slots are tested. The generators and analyzers can be set to operate on either the line side or system side. Bipolar Violation (BPV) frame or Cyclic Redundancy Check (CRC) errors can be inserted in the Tx line direction.

Signaling Support. The IXF3204 framer provides signaling support (either robbed-bit or TS16 CAS) for all ports.

- In the Rx direction, signaling information is available either at the system backplane bus or from an internal table that the host processor can access. The freeze and de-bouncing functions are programmable.
- In the Tx direction, signaling is sent to the line side from either (1) the data available at the system backplane bus or (2) a ‘force’ table the user generates.
- In both Rx and Tx directions, the number of signaling states available is four, nine, and sixteen.

The IXF3204 framer provides extensive support to data-link channels such as DDL and FDL. The user can select the Sa bits to use in the E1 stream to manage the data-link channel. The IXF3204 framer can generate PRM and detect it automatically.

When the IXF3204 framer receives T1.403 PRM, the internal far-end database can be updated when the interrupt is enabled, after which the host processor can be informed. When the host processor requests it, the IXF3204 framer can send PRM. Otherwise, the IXF3204 framer can generate PRM internally every second.

The IXF3204 framer generates an internal database with performance-monitor units. The database, which the host processor can access, holds near-end and far-end parameters in accordance with ANSI T1.231, ITU G.821, and ITU G.826.

Alarm and Error Condition Management. Defects, alarms, and error conditions at DS1/E1 levels that are detected and reported include Alarm Indication Signal (AIS), Loss of Signal (LOS), yellow alarm, and TS16 AIS. Integration times are applied to provide failure indications such as LOS, loss of frame (LOF), or AIS. Possible consequent actions of alarms and errors include the following.

- For the backplane, the possible consequent action is that one of the following can be sent to the backplane: a user-defined pattern, an AIS, or an Auxiliary Pattern (AUXP).
- For the line side, the possible consequent action is that one of the following can be sent to the line side: AIS, AUXP, a Remote End Block Error (REBE), or codewords.

Packaging. The IXF3204 framer has a 17 mm x 17 mm plastic ball-grid array (PBGA) package to enable the design of multi-service line cards with multiple ports.

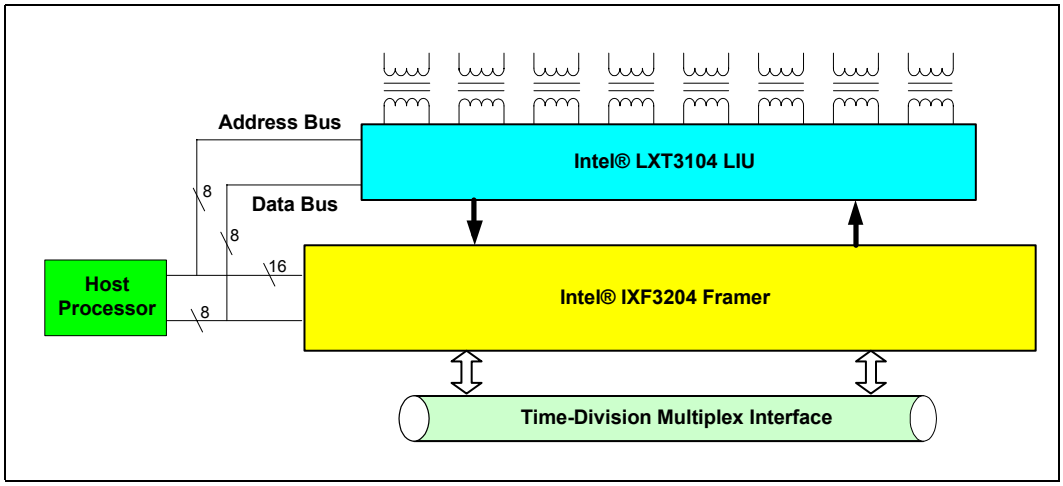
Interfaces to Other Devices.

The IXF3204 framer can interface directly with the following:

- Intel® LXT3104 Quad T1/E1/J1 Long Haul/Short Haul (LH/SH) Line Interface Unit (LIU)
- LIUs from other manufacturers

Figure 1 shows a block diagram of the system backplane of the IXF3204 framer with the Intel® LXT3104 Quad T1/E1/J1 Long/Short Haul Line Interface Unit.

Figure 1. Intel® IXF3204 Framer System Backplane Block Diagram



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Block diagrams.

Figure 2 shows a high-level block diagram of the IXF3204 framer.

Figure 2. Intel® IXF3204 Framer High-Level Block Diagram

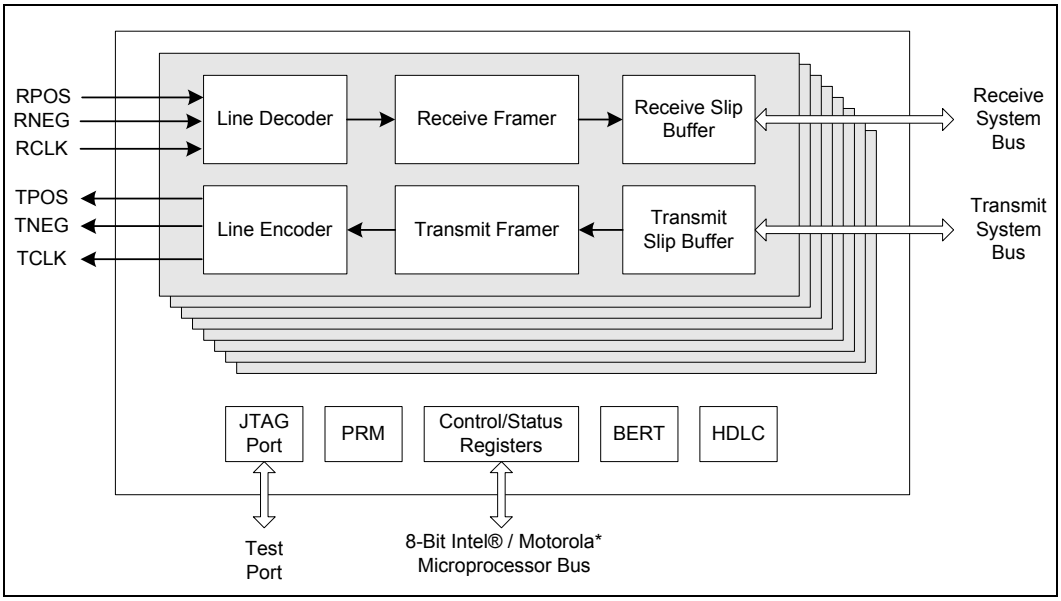
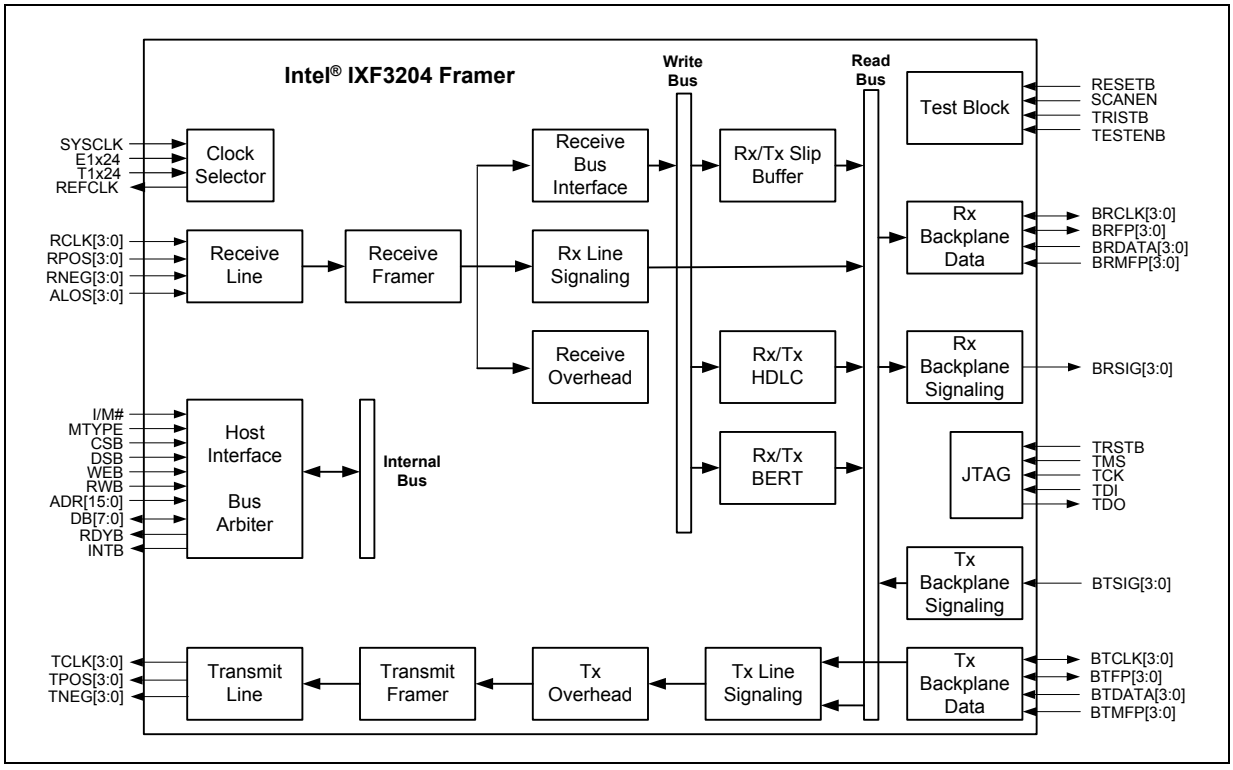


Figure 3 shows a detailed block diagram of the IXF3204 framer.

Figure 3. Intel® IXF3204 Framer Detailed Block Diagram



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2.2 Conventions and Terminology

This section describes the conventions and terminology used throughout this document, which follows telecommunication industry-standard conventions.

2.2.1 Conventions and Terminology for T1/E1

- Telecommunications conventions. This document follows conventions used in the telecommunications industry, such as the following:
  - — Frame numbering increases sequentially with time.
  - — For bit ordering, unless otherwise stated, the most-significant bit (MSB) is transmitted first and is designated Bit 1.
- T1/E1 conventions. Both T1 and E1 conventions define the numbering of bits within a time slot to be designated ‘Bit 1’ through ‘Bit 8’, with Bit 1 defined as the MSB.
  - — Numbering of bits within a frame:
    - T1 numbering is from 1 to 193, with bit 1 being the ‘F’ (framing) bit.
    - E1 numbering is from 1 to 256, with bits 1 to 8 occupying the FAS/NFAS word time slot (time slot 0).
  - — Numbering of ‘channels’ (a T1 term) and ‘time slots’ (an E1 term):
    - T1 sequentially numbers channels beginning with ‘1’.
    - E1 sequentially numbers time slots beginning with ‘0’.
  - — Numbering in multiframe structures:
    - T1 sequentially numbers frames beginning with ‘1’.
    - E1 sequentially numbers frames beginning with ‘0’.
- Terms
  - — ‘Channels’ and ‘time slots’ are used interchangeably.
  - — ‘Out Of Frame’ (OOF) and ‘Loss Of Frame’ (LOF) are used interchangeably.
  - — T1 ‘Yellow Alarm’ and ‘Remote Alarm Indication’ (RAI) are synonymous.
  - — ‘Blue Alarm’ and ‘Alarm Indication Signal’ (AIS) are synonymous.

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2.2.2 Conventions and Nomenclature for Intel® IXF3204 Framer

The IXF3204 framer is a quad device, meaning that it supports up to four T1/E1/J1 links. The links are numbered sequentially, beginning with zero (0) and ending with three (3).

A link is defined as the standard 4-wire receive/transmit pair T1/E1/J1 interface. The terms *link*, *port*, and *span* are used interchangeably in this document.

Time slots for:

- T1 are numbered 0 to 23.
- E1 are numbered 0 to 31.

Channel numbering for T1 is as follows:

- T1 channel 1 corresponds to TS0 (time slot 0).
- T1 channel 2 corresponds to TS1, and so on.

2.3 Related Documents

Table 1. Related Documents for Intel® IXF3204 Framer

Product/Document Name	Document Number
Intel® IXF3204 API Software Developer's Manual	253046

3.0 Signal Descriptions

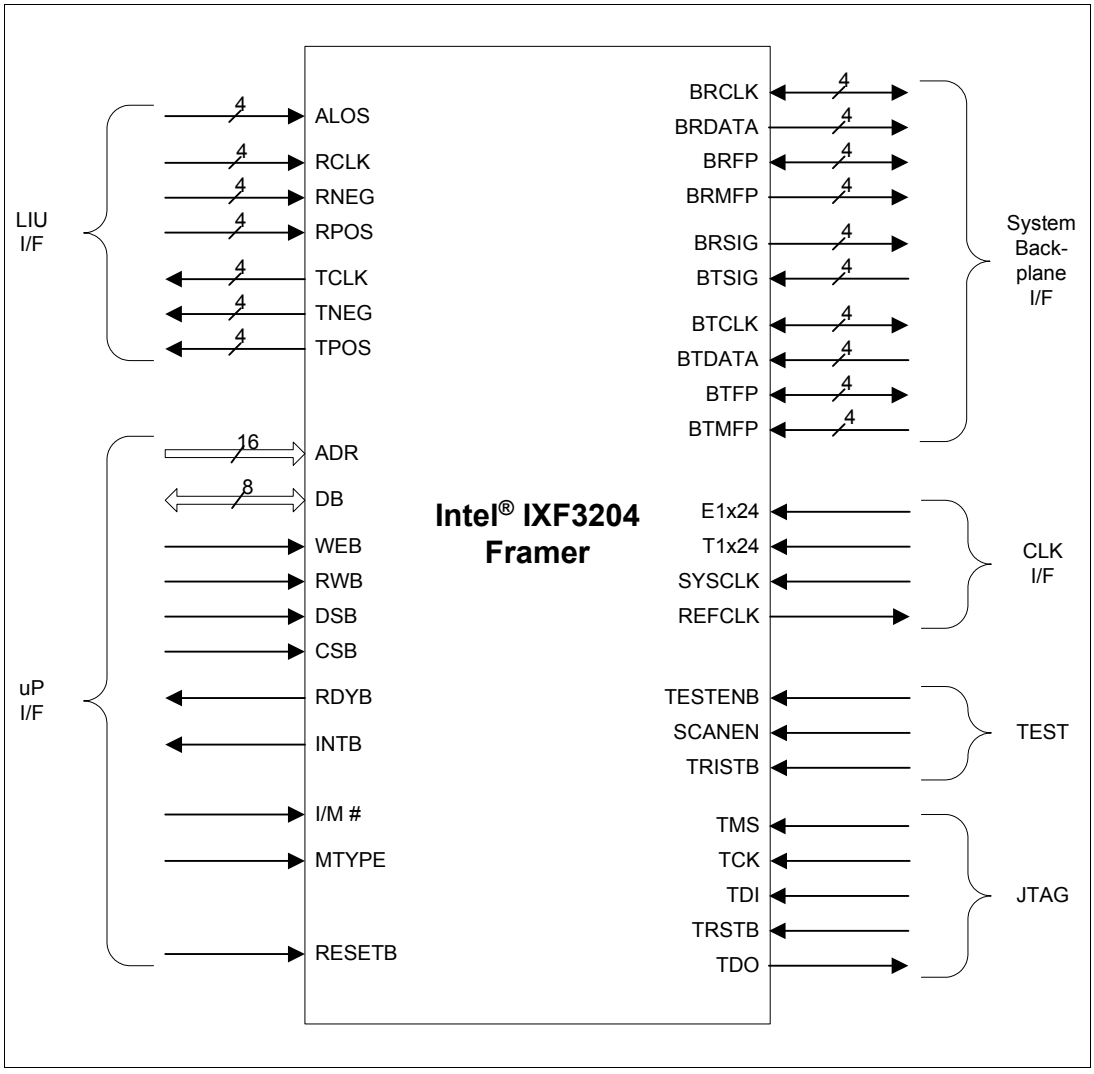
This chapter discusses both logical groupings of signals and ball descriptions.

- For the ball assignments, see Chapter 25.0, "Ball Assignments".
- For mechanical information on the package, see Chapter 26.0, "Mechanical Specifications"

3.1 Signal Groupings

Figure 4 shows a logical grouping of the IXF3204 framer signals.

Figure 4. Signal Groupings for Intel® IXF3204 Framer



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3.2 Ball Descriptions

This section includes the following ball descriptions for the IXF3204 framer:

- Section 3.2.1, “Ball Descriptions - Interface to Line Interface Unit”
- Section 3.2.2, “Ball Descriptions - Interface to System Backplane Bus”
- Section 3.2.3, “Ball Descriptions - Interface to Host Processor”
- Section 3.2.4, “Ball Descriptions - Clock and Clock References”
- Section 3.2.5, “Ball Descriptions - Test Interfaces”
- Section 3.2.6, “Ball Descriptions - Power and Grounds”
- Section 3.2.7, “Ball Descriptions - No Connects”

3.2.1 Ball Descriptions - Interface to Line Interface Unit

Table 2. Intel® IXF3204 Framer - Line Interface Unit Balls (Sheet 1 of 2)

Ball Name	Ball	I/O	Description
ALOS7 ALOS6 ALOS5 ALOS4	C4 B1 A16 B13	I	**Analog Loss Of Signal 7:4.** See Table 8, “Intel® IXF3204 Framer - Power and Ground Balls”.
ALOS3 ALOS2 ALOS1 ALOS0	R12 N11 T1 P4	I	**Analog Loss Of Signal 3:0.** ALOS is an indicator that can be provided by an external LIU to inform the user that a LOS condition has occurred. This indication is sampled and stored. Furthermore, an internal indicator can be set and propagated to the host processor.
RCLK7 RCLK6 RCLK5 RCLK4	C3 D2 B16 A14	I	**Receive Clock 7:4.** See Table 8, “Intel® IXF3204 Framer - Power and Ground Balls”.
RCLK3 RCLK2 RCLK1 RCLK0	R13 T16 N3 T3	I	**Receive Clock 3:0.** RCLK is used to clock data to the receive-side framer. Data can be clocked in on either edge. Each clock is independently controlled.
RNEG7 RNEG6 RNEG5 RNEG4	A2 C1 C15 C13	I	**Receive Data Negative 7:4.** See Table 8, “Intel® IXF3204 Framer - Power and Ground Balls”.
RNEG3 RNEG2 RNEG1 RNEG0	P12 T15 P2 R4	I	**Receive Data Negative 3:0.** RNEG is sampled on the selected edge of the RCLK to receive data for the receive-side framer. (The default is falling edge.) When operating in unipolar mode, RNEG carries other information. For details, see the description of the configuration bits in the memory map document for the IXF3204 framer.
RPOS7 RPOS6 RPOS5 RPOS4	B3 D3 C14 A13	I	**Receive Data Positive 7:4.** See Table 8, “Intel® IXF3204 Framer - Power and Ground Balls”.

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Table 2. Intel® IXF3204 Framer - Line Interface Unit Balls (Sheet 2 of 2)

Ball Name	Ball	I/O	Description
RPOS3 RPOS2 RPOS1 RPOS0	T13 R15 R1 T4	I	**Receive Data Positive 3:0.** RPOS is sampled on the selected edge of the RCLK to receive data for the receive-side framer. (The default is falling edge.) When operating in unipolar mode, RPOS carries the data to be received.
TCLK7 TCLK6 TCLK5 TCLK4	C2 E2 D15 B15	O	**Transmit Clock 7:4.** See Table 9, “Intel® IXF3204 Framer - No Connect Balls”.
TCLK3 TCLK2 TCLK1 TCLK0	R14 N14 N2 R2	O	**Transmit Clock 3:0.** TCLK is used to clock the data from the transmit-side framer. The edge on which data is delivered can be selected to either rising edge or falling edge.
TNEG7 TNEG6 TNEG5 TNEG4	B2 D1 C16 B14	O	**Transmit Data Negative 7:4.** See Table 9, “Intel® IXF3204 Framer - No Connect Balls”.
TNEG3 TNEG2 TNEG1 TNEG0	P13 P15 P1 R3	O	**Transmit Data Negative 3:0.** TNEG is updated on the selected edge of the TCLK to transmit negative bipolar data. (The default is rising edge.) When operating in unipolar mode, TNEG carries other information. For details, see the description of the configuration bits in the memory map document for the IXF3204 framer.
TPOS7 TPOS6 TPOS5 TPOS4	A1 E3 D14 A15	O	**Transmit Data Positive 7:4.** See Table 9, “Intel® IXF3204 Framer - No Connect Balls”.
TPOS3 TPOS2 TPOS1 TPOS0	T14 R16 P3 T2	O	**Transmit Data Positive 3:0.** TPOS is updated on the selected edge of the TCLK to transmit positive bipolar data. (The default is rising edge.) When operating in unipolar mode, TPOS carries the data to transmit.

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3.2.2 Ball Descriptions - Interface to System Backplane Bus

Table 3. Intel® IXF3204 Framer - System Backplane Bus Balls (Sheet 1 of 3)

Ball Name	Ball	I/O	Description
BRCLK7 BRCLK6 BRCLK5 BRCLK4	T12 K15 H12 F14	I/O	**Backplane Receive Clock 7:4.** See Table 9, “Intel® IXF3204 Framer - No Connect Balls”.
BRCLK3 BRCLK2 BRCLK1 BRCLK0	E10 C8 C6 D4	I/O	**Backplane Receive Clock 3:0.** BRCLK can be run at 1x, 2x, or 4x the base clock rate. These rates support replication and concentration modes as well as the H-MVIP and CHI modes. The allowed base clock rates are the following: • 1.536 MHz • 1.544 MHz • 2.048 MHz
BRDATA7 BRDATA6 BRDATA5 BRDATA4	R11 K14 H13 F13	O	**Backplane Receive Data. 7:4.** See Table 9, “Intel® IXF3204 Framer - No Connect Balls”.
BRDATA3 BRDATA2 BRDATA1 BRDATA0	B11 A8 A6 B4	O	**Backplane Receive Data. 3:0.** BRDATA normally carries data from the time slots. However, in a CHI mode, BRDATA can carry data and signaling information in an interleaved fashion. **NOTE:** The clock edge to deliver this data can be configured to either rising or falling.
BRFP7 BRFP6 BRFP5 BRFP4	P11 L16 H16 F15	I/O	**Backplane Receive Frame Pulse 7:4.** See Table 9, “Intel® IXF3204 Framer - No Connect Balls”.
BRFP3 BRFP2 BRFP1 BRFP0	D11 D8 C7 A3	I/O	**Backplane Receive Frame Pulse 3:0.** The clock edge to deliver or sample BRFP can be configured to either rising or falling. Additional parameters that can be configured include the delay from bit 0, the polarity, and the width of the active pulse.
BRMFP7 BRMFP6 BRMFP5 BRMFP4	T11 M16 J13 F16	O	**Backplane Receive Multiframe Pulse 7:4.** See Table 9, “Intel® IXF3204 Framer - No Connect Balls”.
BRMFP3 BRMFP2 BRMFP1 BRMFP0	A11 D9 B7 C5	O	**Backplane Receive Multiframe Pulse 3:0.** The parameters selected for BRFP are also used to sample BRMFP in terms of delay, width, and polarity.
BRSIG7 BRSIG6 BRSIG5 BRSIG4	P10 M13 J15 G15	O	**Backplane Receive Signaling 7:4.** See Table 9, “Intel® IXF3204 Framer - No Connect Balls”.

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Table 3. Intel® IXF3204 Framer - System Backplane Bus Balls (Sheet 2 of 3)

Ball Name	Ball	I/O	Description
BRSIG3 BRSIG2 BRSIG1 BRSIG0	C11 C9 D6 B5	O	**Backplane Receive Signaling 3:0.** BRSIG carries the signaling information of the receive T1/E1 data stream. **NOTE:** The clock edge and rate selected for BRDATA are used to deliver the signaling information.
BTCLK7 BTCLK6 BTCLK5 BTCLK4	R10 N13 J14 G16	I/O	**Backplane Transmit Clock 7:4.** See Table 9, “Intel® IXF3204 Framer - No Connect Balls”.
BTCLK3 BTCLK2 BTCLK1 BTCLK0	D13 B9 E7 A4	I/O	**Backplane Transmit Clock 3:0.** BTCLK can be run at 1x, 2x, or 4x the base clock rate. These rates support replication and concentration modes as well as the H-MVIP and CHI modes. The allowed base clock rates are the following: • 1.536 MHz • 1.544 MHz • 2.048 MHz
BTDATA7 BTDATA6 BTDATA5 BTDATA4	T10 M14 J16 G14	I	**Backplane Transmit Data 7:4.** See Table 8, “Intel® IXF3204 Framer - Power and Ground Balls”.
BTDATA3 BTDATA2 BTDATA1 BTDATA0	A12 A9 A7 A5	I	**Backplane Transmit Data 3:0.** BTDATA normally carries data from the timeslots. However, in a CHI mode, BTDATA can carry data and signaling information in an interleaved fashion. **NOTE:** The clock edge to sample this data can be configured to either rising or falling.
BTFP7 BTFP6 BTFP5 BTFP4	T9 L15 L13 G13	I/O	**Backplane Transmit Frame Pulse 7:4.** See Table 9, “Intel® IXF3204 Framer - No Connect Balls”.
BTFP3 BTFP2 BTFP1 BTFP0	B12 D10 D7 D5	I/O	**Backplane Transmit Frame Pulse 3:0.** The clock edge to deliver or sample the BTFP signals can be configured to either rising or falling. Additional parameters that can be configured are the delay from bit 0 and the polarity and the width of the active pulse.
BTMFP7 BTMFP6 BTMFP5 BTMFP4	P9 L14 K13 H14	I	**Backplane Transmit Multiframe Pulse 7:4.** See Table 8, “Intel® IXF3204 Framer - Power and Ground Balls”.
BTMFP3 BTMFP2 BTMFP1 BTMFP0	C12 C10 E8 E6	I	**Backplane Transmit Multiframe Pulse 3:0.** The parameters selected for BTFP are also used to sample BTMFP in terms of delay, width, and polarity.

Table 3. Intel® IXF3204 Framer - System Backplane Bus Balls (Sheet 3 of 3)

Ball Name	Ball	I/O	Description
BTSIG7 BTSIG6 BTSIG5 BTSIG4	R9 M15 K16 H15	I	**Backplane Transmit Signaling 7:4.** See Table 8, “Intel® IXF3204 Framer - Power and Ground Balls”.
BTSIG3 BTSIG2 BTSIG1 BTSIG0	D12 B10 B8 B6	I	**Backplane Transmit Signaling 3:0.** BTSIG carries the signaling bits for insertion into the outgoing T1/E1 data stream. **NOTE:** The clock edge and rate selected for BTDATA are also used to sample the signaling information.

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3.2.3 Ball Descriptions - Interface to Host Processor

Table 4. Intel® IXF3204 Framer - Interface to Host Processor Balls (Sheet 1 of 2)

Ball Name	Ball	I/O	Description
ADR15 ADR14 ADR13 ADR12 ADR11 ADR10 ADR9 ADR8 ADR7 ADR6 ADR5 ADR4 ADR3 ADR2 ADR1 ADR0	G2 G1 G3 H4 H1 H3 H2 J1 J3 K1 J2 J4 K4 K3 L1 K2	I	**Address.** The 16-bit ADR address lines are used to read or write any internal register or RAM region. For details, see the memory map document for the IXF3204 framer.
CSB	F3	I	**Chip Select. (Active Low.)** When CSB is low, it selects the IXF3204 framer, allowing it to perform read/write operations.
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0	N1 M3 M2 N4 M1 L3 M4 L2	I/O	**Data Bus.** The 8-bit DB signals are used to transfer data through read or write transactions. **NOTE:** A DB signal enters a tristate either when there is no data transfer or when the data transfer is a write process.
DSB	P14	I	**Data Strobe. (Active Low.)** Depending on the processor being used, DSB operates in a different way in the modes supported by the three processors. For details, see Section 20.0, “Host Processor Interface”.
I/M#	N12	I	**Intel® Processor / Motorola Processor.** I/M# selects a processor interface mode as follows: • I/M# = 0 selects a Motorola processor. • I/M# = 1 selects an Intel® processor.
INTB	P16	O	**Hardware Interrupt Output, Open Drain.** When INTB is not asserted, it is in a tristate. When the I/M# ball sets the processor mode for a: • Motorola processor, INTB is active in the ‘0’ state. • Intel® processor, INTB is active in the ‘1’ state.
MTYPE	F1	I	**Motorola Processor Types.** MTYPE selects a Motorola processor type as follows: • MTYPE = 0 selects from the family of Motorola Power PC processors (such as the Motorola MPC860 processor) • MTYPE = 1 selects from the family of Motorola 68K processors (such as the Motorola 68302 processor)

Table 4. Intel® IXF3204 Framer - Interface to Host Processor Balls (Sheet 2 of 2)

Ball Name	Ball	I/O	Description
RDYB	N15	O	**Ready Signal. (Active Low, Open Drain.)** • When a data transfer to the IXF3204 framer is selected, RDYB is set to '1'. • When the data transfer is complete, RDYB is set to '0'. • When the host processor removes CSB (CSB = '1'), then RDYB goes to a tristate.
RWB	N16	I	**Read / Write. (Active Low.)** RWB distinguishes between read and write operations. • 0 = Write • 1 = Read
WEB	F2	I	**Write Enable. (Active Low for Motorola MPC860 Processor.)** Depending on the processor being used, WEB indicates a write operation when CSB is active, and the IXF3204 framer loads the internal register with data provided on the data bus.
RESETB	R6	I	**Master Hardware Reset. (Active Low.)** When low, RESETB resets the IXF3204 framer hardware. RESETB has an internal pull-up resistor.

3.2.4 Ball Descriptions - Clock and Clock References

Table 5. Intel® IXF3204 Framer- Clocks and Clock Reference Balls

Ball Name	Ball	I/O	Description
E1x24	P5	I	**E1 x 24.** E1x24 is a clock input to be used to generate E1 rates locked to the reference, with jitter removed. E1x24 is required if the internal phase-locked loop is to be used to remove jitter from a reference line signal. E1x24 is also required if a divided-down frequency is to be used as a timing reference for the Tx line-side. Otherwise, when it is not in use, set it to '0'.
REFCLK	R5	O	**Reference Clock.** REFCLK is a reference clock that can be taken from any of the Rx lines.
SYSCLK	E1	I	**System Clock.** SYSCLK is the system clock used for the internal state machines. Typically, SYSCLK is a 33-MHz clock.
T1x24	T5	I	**T1 x 24.** T1x24 is a clock input to be used to generate T1 rates locked to the reference, with jitter removed. T1x24 is required if the internal phase-locked loop is to be used to remove jitter from a reference line signal. T1x24 is also required if a divided-down frequency is to be used as a timing reference for the Tx line-side. However, when it is not in use, set it to '0'.

3.2.5 Ball Descriptions - Test Interfaces

The IXF3204 framer has two types of test interfaces: (1) a test interface designed for the IXF3204 framer specifically and (2) the industry-standard test interface designed by the Joint Test Action Group (JTAG).

3.2.5.1 Test Interface 1 - Intel® IXF3204 Framer

Table 6. Intel® IXF3204 Framer - Test Interface 1 Balls

Ball Name	Ball	I/O	Description
SCANEN	P7	I	**Scan Enable.** SCANEN is set to '0' when in normal operation.
TESTENB	R7	I	**Test Enable. (Active Low.)** • 0 = Scan mode • 1 = Normal operation
TRISTB	T7	I	**Tristate. (Active Low.)** • 0 = Place all outputs into a tristate. • 1 = Normal operation TRISTB has an internal pull-up resistor.

3.2.5.2 Test Interface 2 - JTAG Test

Table 7. Intel® IXF3204 Framer - Test Interface 2 Balls

Ball Name	Ball	I/O	Description
TCK	E14	I	**Test Clock.** TCK provides timing for the JTAG test operations, which can be carried out using the IEEE P1149.1 test access port. TCK has an internal pull-down resistor.
TDI	D16	I	**Test Data Input.** TDI carries JTAG test data input through IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK, and it has an internal pull-up resistor.
TDO	E13	O	**Test Data Output.** TDO carries JTAG test data output through the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO has a tristate output, which is inactive except when scanning of data is in progress.
TMS	E15	I	**Test Mode Select.** TMS controls the JTAG test operation that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCLK, and it has an internal pull-up resistor.
TRSTB	E16	I	**Test Reset (Active Low).** TRSTB provides JTAG test access port reset through the IEEE P1149.1 test access port. TRST has a pull-up resistor and must be asserted during power-up sequence.

3.2.6 Ball Descriptions - Power and Grounds

Table 8. Intel® IXF3204 Framer - Power and Ground Balls

Ball Name	Ball	Power, Ground	Description
ALOS7 ALOS6 ALOS5 ALOS4	C4 B1 A16 B13	-	**Analog Loss Of Signal 7:4.** ALOS7:4 signals must be connected to VSS (ground).
BTDATA7 BTDATA6 BTDATA5 BTDATA4	T10 M14 J16 G14	-	**Backplane Transmit Data 7:4.** BTFP7:4 signals must be connected to VSS (ground).
BTMFP7 BTMFP6 BTMFP5 BTMFP4	P9 L14 K13 H14	-	**Backplane Transmit Multiframe Pulse 7:4.** BTMFP7:4 signals must be connected to VSS (ground).
BTSIG7 BTSIG6 BTSIG5 BTSIG4	R9 M15 K16 H15	-	**Backplane Transmit Signaling Input 7:4.** BTSIG7:4 signals must be connected to VSS (ground).
RCLK7 RCLK6 RCLK5 RCLK4	C3 D2 B16 A14	-	**Receive Clock 7:4.** RCLK7:4 signals must be connected to VSS (ground).
RNEG7 RNEG6 RNEG5 RNEG4	A2 C1 C15 C13	-	**Receive Negative 7:4.** RNEG7:4 signals must be connected to VSS (ground).
RPOS7 RPOS6 RPOS5 RPOS4	B3 D3 C14 A13	-	**Receive Positive 7:4.** RPOS7:4 signals must be connected to VSS (ground).
VDD_CORE	E9, E11, F6, G5, J5, L12, M6, M8, M10	Power	**Core Logic Supply Voltage.** VDD_CORE must be connected to a decoupled 1.8 V power supply.
VDD_IO	F5, F7, F10, G12, J12, K5, M7, M9	Power	**Interface Circuitry Supplied Voltage.** VDD_IO must be connected to a decoupled 3.3 V power supply.
VSS	A10, E4, E5, E12, F4, F8, F9, F11, F12, G4, G6, G7, G8, G9, G10, G11, H5, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, K12, L4, L5, L6, L7, L8, L9, L10, L11, M5, M11, M12, N5, N6, N7, N8, N9, N10	Ground	**Ground Return.** All VSS balls must be connected to ground.

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3.2.7 Ball Descriptions - No Connects

Table 9. Intel® IXF3204 Framer - No Connect Balls

Ball Name	Ball	Description
BRCLK7 BRCLK6 BRCLK5 BRCLK4	T12 K15 H12 F14	**Backplane Receive Clock 7:4.** BRCLK7:4 signals must be left as no connects.
BRDATA7 BRDATA6 BRDATA5 BRDATA4	R11 K14 H13 F13	**Backplane Receive Data. 7:4.** BRDATA7:4 signals must be left as no connects.
BRFP7 BRFP6 BRFP5 BRFP4	P11 L16 H16 F15	**Backplane Receive Frame Pulse 7:4.** BRFP7:4 signals must be left as no connects.
BRMFP7 BRMFP6 BRMFP5 BRMFP4	T11 M16 J13 F16	**Backplane Receive Multiframe Pulse 7:4.** BRMFP7:4 signals must be left as no connects.
BRSIG7 BRSIG6 BRSIG5 BRSIG4	P10 M13 J15 G15	**Backplane Rx Signaling 7:4.** BRSIG7:4 signals must be left as no connects.
BTCLK7 BTCLK6 BTCLK5 BTCLK4	R10 N13 J14 G16	**Backplane Transmit Clock 7:4.** BTCLK7:4 signals must be left as no connects.
BTFP7 BTFP6 BTFP5 BTFP4	T9 L15 L13 G13	**Backplane Transmit Frame Pulse 7:4.** BTFP7:4 signals must be left as no connects.
NC_6 NC_5 NC_4 NC_3 NC_2 NC_1	T6 P6 R8 P8 T8 H6	**No Connect 6 to No Connect 1.** Reserved. (These balls are No Connects).
TCLK7 TCLK6 TCLK5 TCLK4	C2 E2 D15 B15	**Transmit Clock - Output to LIU 7:4.** TCLK7:4 signals must be left as no connects.
TNEG7 TNEG6 TNEG5 TNEG4	B2 D1 C16 B14	**Transmit Negative - Data Output to LIU 7:4.** TNEG7:4 signals must be left as no connects.
TPOS7 TPOS6 TPOS5 TPOS4	A1 E3 D14 A15	**Transmit Positive - Data Output to LIU 7:4.** TPOS7:4 signals must be left as no connects.

4.0 Feature Set and Indicators

This chapter discusses the following topics:

- Section 4.1, "Feature Set"
- Section 4.2, "Indicators"

4.1 Feature Set

Table 10 lists the line and framing feature set for the IXF3204 framer.

Table 10. Line and Framing Features (Sheet 1 of 3)

Feature	Description
Interface	**Interfaces.** Bipolar: POS, NEG, CLK Unipolar: NRZ, CLK
Line Coding	**Selectable Line Coding.** **T1 Selectable.** AMI (per ANSI T1.102) B8ZS (per ANSI T1.102) Zero-code suppression ('ZCS', also known as 'Bit 7 coding'), Tx direction only **E1 Selectable.** AMI (per ITU G.703) HDB3 (per ITU G.703)
Line Monitoring	**Line Monitoring - Maskable Interrupt Generation.** **T1 – Maskable Interrupt Generated for All Conditions.** • AIS – Alarm Indication Signal. A ones' density of at least 99.9% in a window of 3 milliseconds to 75 milliseconds (per ANSI T1.231 and ITU G.775). • As an option, OOF condition can be used to validate AIS (per ANSI T1.403). • LOS - Loss of signal: 175 ± 75 clocks with no pulse transitions (per ANSI T1.231) • BPV - Bipolar violation • EXZ – Excess zeroes **E1 – Maskable Interrupt Generated for All Conditions.** • AIS – Alarm Indication Signal. Two or less zeroes in two consecutive double-frame windows (per ITU G.775) *-Or-* • OOF and less than three zeroes in a 512-bit period (per ETS 300 233) • LOS – Loss of signal: N consecutive intervals with no pulse transitions, where N is in the range of 10 to 255 (per ITU G.775) *-Or-* • A 1-millisecond window with no transitions causes LOS (per ITU I.431) • BPV – Bipolar Violation Detection. Two consecutive marks of the same polarity • HDB3 code violations – Two consecutive BPVs of the same polarity

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Table 10. Line and Framing Features (Sheet 2 of 3)

Feature	Description
Framing Modes	**Framing Modes.** **T1** D4-SF (per ANSI T1.107, T1.403) ESF (per ANSI T1.107, T1.403) SLC®96 (per Telcordia GR-303 and Telcordia TR-TSY-008) **E1** FAS/NFAS double-frame (per ITU G.704, G.706) CRC-4 multiframe (per ITU G.704, G.706) CAS multiframe (per ITU G.704, G.706, G.732) CRC-4 and CAS multiframe (per ITU G.704, G.706, G.732) **J1** J1 12-frame multiframe (per JT G.703, JT G.704, JT G.706, I.431) J1 24-frame multiframe (per JT G.703, JT G.704, JT G.706, I.431) **Transparent Framing Modes.** The IXF3204 framer can operate in either a T1 or E1 transparent mode. **T1 Transparent** The IXF3204 framer does not search or generate framing information. **E1 Transparent** The IXF3204 framer does not search or generate framing information. **NOTE:** In transparent modes, if a frame pulse is generated or received at the backplane, it must follow the T1 or E1 frame duration (193 or 256 bits).
Maximum Average Reframe Time	**Maximum Average Reframe Time.** The average reframe time for the IXF3204 framer is as follows: • 9 milliseconds in D4 SF mode • 14 milliseconds in ESF mode • 20 milliseconds in SLC®96 mode **T1** T1 – D4 SF 50 milliseconds (per G.704) T1 – ESF 15 milliseconds (per G.706) T1 – SLC®96 50 milliseconds (per G.706) **J1** J1 – 12 frames 50 milliseconds (using as reference G.704) J1 – ESF (24 frames) 15 milliseconds (using as reference G.706) **E1** E1 – FAS/NFAS: Average reframe time of the IXF3204 framer is 1 millisecond. E1 – CRC-4: Average reframe time of the IXF3204 framer is 7 milliseconds. E1 – CAS: Average reframe time of the IXF3204 framer is 7 milliseconds. E1 – CRC-4/CAS: Average reframe time of the IXF3204 framer is 7 milliseconds.

Table 10. Line and Framing Features (Sheet 3 of 3)

Feature	Description
False Framing Protection	**False Framing Protection.** **T1 - D4 SF** Ft coupled with Fs framing bits **T1- ESF** Fe framing bits coupled with CRC-6 error detection bits **T1- SLC®96** Ft framing bits coupled with Fs bits plus DDL spoiler bits **E1 - CRC-4** FAS/NFAS coupled with CRC-4 sync sequence. CRC calculation also checked.

Out Of Frame (OOF) Conditions	**Out Of Frame Detection (OOF).**
	Maskable interrupt generated.
	Reframing.
	Automatic or manual reframing upon detection of OOF condition.
	Change of Frame Alignment (COFA).
	Latest receiver synchronization results in a change of frame or multiframe alignment. After reset, the first time the port is synchronized, a COFA is always declared.
	T1
	• **T1 D4** - Out Of Frame is forced when there are M errors in a programmable window of N consecutive Ft or Fs bits. M = 1,2:7 and N = 1,2:7.
	• **T1 ESF** - Out Of Frame is forced when there are M errors in a programmable window of N consecutive Fe bits. M = 1,2:7 and N = 1,2:7.
	• **Forced Reframe** - As an option, a reframe can be forced when the number of CRC6 errors is equal to or exceeds 320 in a one-second interval.
	E1
	• **E1 Loss of Basic Frame Alignment (BFA)** - BFA occurs when there are either three consecutive errors in FAS or three consecutive errors in NFAS.
	• **E1 Loss of CRC Multiframe** - As a programmable option, a loss of CRC multiframe is declared if either of the following occur:
	  • There are 915 or more CRC errors detected in a one-second interval.
	  • N errors in a window of M bits occur in the CRC multiframe alignment signal.
	• **E1 Loss of CAS Multiframe** - Two consecutive CAS multiframe alignment words received in error cause a multiframe to be out of CAS. As an option, the user can declare a multiframe is out of CAS if, in a whole multiframe, all TS16 time slots are received in a '0' state.
	NOTE: For all E1 operations:
	• Whenever BFA is lost, CAS and CRC multiframes are lost.
	• Loss of CRC multiframe cause a loss of Basic Frame alignment.

CRC of T1 ESF and E1 CMF Disabling	**CRC6 of T1 ESF and E1 CRC-4 Disabling.** When the direction is: • Rx, CRC checking can be disabled. • Tx, CRC bits can be taken from the backplane data.

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Table 11 lists the slip buffer features for the IXF3204 framer.

Table 11. Slip Buffer Features

Feature	Description
Slip Buffers	**Slip Buffers.** • Separate slip buffers for both the receive and transmit paths. • Always engaged. As an option, slip buffers can be Minimum Delay or Two Frames. • Read and Write pointer can be accessed (read and write) from the host processor • Slip indication • Slip direction indication • Pointer separation indication (RdPtr – WrPtr) • Manual or automatic re-centering under COFA conditions • For details on slip buffers, see Chapter 13.0, "Slip Buffers".

Table 12 lists the signaling features for the IXF3204 framer.

Table 12. Signaling Features

Feature	Description
Signaling	**T1/J1-Robbed-Bit Signaling.** • D4 SF – Four states: AB bits • ESF – Sixteen states: ABCD bits • SLC®96 – Four (AB) or nine states (AB + toggling) **T1/E1/J1 Common Channel Signaling (CCS).** • Available using the HDLC section of FDL module • CCS available by selecting any TS in either T1 or E1 modes **E1 Channel Associated Signaling (CAS).** • On TS16 (per ITU G.704) **T1/E1/J1.** • Signaling Freeze per DS1/E1 - Triggered by loss of Frame conditions. (LOS, AIS, OOF, OOCAS) • Signaling Debounce - Disable or two multiframes • Signaling forced by the host processor - The host processor can define signaling to transmit in each direction (line and backplane). This value is kept until the host processor changes it or releases it. **Signaling Access.** • Signaling can be accessed through the host processor bus or on the signaling bus. • Signaling change indicators per DS0 **NOTE:** In T1 nomenclature, the term 'DS0' is the same as a time slot (TS).

Table 13 lists the T1 performance-monitoring features for the IXF3204 framer.

Table 13. T1 Performance Monitoring Features (Sheet 1 of 2)

Feature	Description
Compliance	**T1 Compliance.** ANSI T1.231, T1.403
PRM	**Performance Report Messaging.** Automatic generation and detection of one-second T1.403 PRM
Counters	**Counters.** • 15 minutes - Thirty-one bins, each containing the 15 minutes of accumulated data related to the parameter being measured. • 24 hours • Automatic integration and parameterization of primitives and alarms.

Performance Primitives	**Anomalies (per ANSI T1.231).**
	Line
	• EXZ – Excess zeroes
	• AMI/ZCS – Any string with greater than 15 consecutive zeroes
	• B8ZS – Any string with greater than 7 consecutive zeroes
	• BPV – Bipolar Violations
	• Pulse of the same polarity as previous pulse excluding those which are a part of the B8ZS Code
	Path
	• FE – Frame bit errors
	• SF – Any Ft or Ft and Fs bit error
	• ESF – Any Fe Bit error
	• CS – Controlled slips
	• Change of Frame Alignment (COFA) indication
	• CRC-6 – CRC errors
	• Any received CRC-6 code not identical to the corresponding locally calculated code
	
	Defects (per ANSI T.1231).
	Line
	• LOS – Loss Of Signal
	• OOF – Out Of Frame
	Path
	• AIS – Alarm Indication Signal
	• SEF – Severely Errored Frame
	  • In SF mode: 2 or more Ft bit errors in a 0.75-millisecond window (that is, 2 of 6 Ft bits in error)
	  • In ESF mode: 2 or more Fe bit errors in a 3-millisecond window (that is, 2 of 6 Fe bits in error)

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Table 13. T1 Performance Monitoring Features (Sheet 2 of 2)

Feature	Description
Performance Failures	**Detected Performance Failures (per ANSI T1.231).** • LOS – LOS defect for more than 2 seconds • AIS – AIS defect for more than 2 seconds • LOF – OOF defect for more than 2 seconds • RAI – Remote Alarm Indication. Indicated as soon as alarm is detected
Far-End Performance Reporting	**Far-End Performance Reporting (per ANSI T1.403).** • User-controllable automatic message assembly and transmission • FDL PRM support in both receive and transmit directions
Performance Parameters	**Performance Parameters.** The following performance parameters are collected, integrated, and stored (per ANSI T1.231). The parameters are accessible through the host processor interface. **Line Parameters – Near-end** • CV-L • ES-L • SES-L **Path parameters – Near-end** • CSS-P • CV-P • ES-P • SAS-P • SES-P • UAS-P **Line Parameters– Far-end** • ES-LFE **Path Parameters – Far-end** • CSS-PFE • CV-PFE • ES-LFE • ES-PFE • ESA-PFE • ESB-PFE • SEFS-PFE • SES-PFE • UAS-PFE

Table 14 lists the E1 performance-monitoring features for the IXF3204 framer.

Table 14. E1 Performance Monitoring Features

Feature	Description
Compliance	**E1 Compliance.** ITU G.821, G.826, O.150, ETS 300 011, ETS 300 233
Counters	**Counters.** Accumulative counters, 32 bits long
Line-Code Violations	**Line Code Violations (per ITU O.161).** • AMI - Two consecutive marks of the same polarity • HDB3 - Two consecutive marks of the same polarity
Performance Primitives	**Near-End Anomalies (per ITU G.826).** • a_1 - An errored frame-alignment signal • a_2 - An Errored Block (EB) as indicated by the CRC not matching the received CRC-4 **Near-End Defects** • d_1 - Loss of signal • d_2 - Alarm indication signal • d_3 - Loss Of Frame alignment **Far-End Parameters (as defined for the IXF3204 framer)** • FE-a1 - E bit received active (‘0’) • FE-d1 - AIS is received active (‘1’)
Performance Parameters	**Performance Parameters.** The following performance parameters are collected and stored (per ITU G.826). The parameters are accessible through the host processor interface. **Events** • BBE – Background Block Error • EB – Errored Block • ES – Errored Second • SES – Severely Errored Second **Parameters** • BBER – Background Block Error Ratio • ESR – Errored Seconds Ratio • SESR – Severely Errored Seconds Ratio

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Table 15 lists the data-link features for the IXF3204 framer.

Table 15. Data-Link Features

Feature	Description
Dedicated FDL Processors	**Dedicated Transmit and Receive Facility Data Link Processor Per-Port.** Includes MOP processing and BOPs
T1 Data Links	**Supported T1 Data Links.** • SLC®96 Derived Data Link (per Telcordia TR-TSY-008) • ESF Facility Data Link (per ANSI T1.403 and Telcordia TR-TSY-499) • ESF Facility Data Link (per AT&T TR 54016) • ISDN PRI D-Channel handler Support (per Telcordia TR-TSY-754) • The data link is accessed through the host processor interface.
E1 Data Links	**Supported E1 Data Links.** • TS0 Sa4 Bit Data Link - M Channel [per ITU I.431 and G.962 (ETS 300 233)]. • User can select any combination of any of the Sa(8:4) bits • TS16 Data Link • V5.2 DLC Data Link Support for time slots 15, 16, 31 (per ETS 300 347-1, ITU G.965) • The data link is accessed through the host processor interface.

Table 16 lists the embedded high-level data-link controller features for the IXF3204 framer.

Table 16. Embedded High-Level Data-Link Controller Features

Feature	Description
General	**General.** The IXF3204 framer has 24 full-duplex controller processors, each mappable from one payload bit on any line port, up to the entire payload.
Data Rates	**Data Rates.** • From 8 Kbps (one payload bit) up to the entire payload (minus framing and signaling bits). • Consecutive/non-consecutive channel concatenation for H0, H11, and H12 are also supported.
Control/Access	**Control/Access.** Control is through an 8-bit host processor interface and access is through FIFO registers. Maskable interrupts for each channel/source.
Applications/Protocols Supported	**ISDN LAPD/LAPB (HDLC) Protocol Messaging (per ITU Q.921).** • Integrated DLC (per Telcordia GR-303) • V5.1 and V5.2 Interfaces (per ITU G.964/ETS 300 324, ITU G.965/ETS 300 347)
Modes	**Non-Automatic.** • HDLC LAPB, LAPD, and LAPV5 protocols without procedure support and with address matching • Framed without address matching • Framed without CRC check/insertion • Fully transparent, clear channel, no processing is performed, and every byte is stored in the FIFO.
HDLC Features	**Non-Automatic Mode.** • Supports All LAPx protocols • Programmable rate per channel: Any combination of bits, including DS0 subrate, DS1, H0, H11, and H12 **Bit-Oriented Functions.** • Flag generation/recognition • Address recognition • Bit stuffing, zero insertion/deletion • CRC generation/check • Abort generation/recognition • Non-octet frame content recognition • Minimum frame-length check and maximum frame-length check and cut off • Interframe generation/support for 7Eh or FFh • Supports reception of shared opening/closing flag • Supports reception of shared 0 in flags • Framed Transparent mode • Starting and ending flag of 7Eh generation/recognition • Removal of starting and ending flag and interframe time fill at receive-side • Fully Transparent mode • Byte-aligned data transmission for transparent mode
FIFO Buffers	**FIFO Buffers.** • FIFO status through the host processor interface • Transmit FIFO depth of 128 bytes (128 x 1 bytes) • Receive FIFO depth of 128 bytes (128 x 1 bytes)

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Table 17 lists interface features for the IXF3204 framer.

Table 17. Interface Features (Sheet 1 of 2)

Feature	Detail
Host Processor Interface	**Host Processor Interface.** • 8-bit parallel data interface • Non-multiplexed mode • 16-bit address bus • Supports Motorola and Intel® buses • Supports Motorola processors such as the M68360, MPC860, and M68302 • Supports Intel® i486™ and i960® processors in synchronous bus interfaces • Asynchronous bus support • Wait states are inserted by using the RDYB signal • Internal wait-state generator • One open-drain interrupt output, INTB • Support for interrupt-driven, polled, or mixed-access architectures
Line Interface	**Types.** • Bipolar data (POS and NEG) and clock • NRZ data and clock • Independent clock and data inputs/outputs for each port
System Backplane - General Features	**System Backplane - General Features.** • Non-multiplexed or N-Port multiplexed operation (N = 4 or 8) • Byte replication in multiplexed mode • Clock source selection for each port • Programmable clock-rate selection (1x or 2x data rates) • Full user control of frame sync polarity, width, and position • Compatibility: TDM, MVIP/ST-BUS, H-MVIP, CHI (data and signaling on the same ball), and so on • Support for gapped-clock generation • Independent clock, data, signaling, frame pulse, and multiframe pulse signals per port.

System Backplane - Timing	**Independent Port Timing.**
	• Tx and Rx timing on each port is fully independent (Tx and Rx can work asynchronously) and uses independent clock/frame sync pairs.
	• Selectable internal clock source generated from a single reference (that is, either a line or external reference clock).
	Selectable Master or Slave Operation:
	• Tx and Rx Clock/Frame Sync signals can be inputs (Slave) or outputs (Master).
	• When the Tx or Rx timing signals are outputs (Master), their timing can be derived from the internal clock source or from a selected Rx Line Clock.
	• Slave Clock input can be any of the following (where N = 1, 2, 4, or 8):
	  • N x 1.536 MHz
	  • N x 1.544 MHz
	  • N x 2.048 MHz

Table 17. Interface Features (Sheet 2 of 2)

Feature	Detail
Overhead Information	**Signaling Data Accessibility.** Signaling data are accessible in the following ways: • In-band • Signaling TDM port • Host processor interface The method of access is independent of data direction. (For example, Tx and Rx for a particular port can use different means of access.) **NOTE:** FDL data are accessible through the host processor interface.

Table 18 lists the maintenance and diagnostics features for the IXF3204 framer.

Table 18. Maintenance/Diagnostics Features

Feature	Detail
Maintenance Loopbacks	**Supported T1 Line-Side Loopbacks.** • T1 line (per ANSI T1.403, AT&T TR 54016) • T1 payload (per ANSI T1.403, AT&T TR 54016) • T1 partial payload loopback. (Up to 24 DS0s simultaneously per port.) **Supported E1 Line-Side Loopbacks.** • E1 line • E1 payload • E1 partial payload loopback. (Up to 32 time slots simultaneously per port.) **Supported System-Side Loopbacks.** • T1 local loopback (data back from Tx line to system backplane) • E1 local loopback **NOTES:** • Line and local loopbacks can be active at the same time. • Selective manual or automatic loopback is supported. • Automatic AIS transmit upon loopback activation is selectively supported.
Error Insertion	**Selectable Bipolar Violation, F-bit (T1)/ FAS Word (E1), and CRC Error Injection.** • Single errors • Programmable rate from 1 to 10^{-6} The error insertion rate is associated with a related event, so that errors in Fe bits set to 10^{-1} indicate that for every 10 Fe bits there is one error inserted. In the case of BPVs, the same rate is applied to every ten marks.
External Indicators	**External Indicators.** • Multiframe signals per-line port reported to the system backplane • Frame sync polarity, width, and position are fully programmable • The polarity, width, and position of the multiframe signal follows that of the corresponding frame sync
Time-Slot Code Insertion	• T1: Digital reference signal (DRS) pattern • T1: Selectable digital milliwatt pattern insertion (per ITU G.711) • E1: DRS pattern • E1: Selectable digital milliwatt pattern insertion (per ITU G.711)

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Table 19 lists the pattern generator, pattern receiver, and BERT features for the IXF3204 framer.

Table 19. Pattern Generator/Receiver and BERT Features

Feature	Description
Compliance	**Pattern Generator/Receiver and BERT Compliance.** For both the pattern generator/receiver and BERT, compliance is as follows: • ANSI T1.231, AT&T TR 62411, Telcordia TR-TSY-820, and Telcordia TR-NWT-001219 • ITU O.150, ITU O.151, ITU O.152, and ITU O.153
Pattern Generation and Bit Error Rate Tester (BERT)	**Eight Programmable Pattern Generators and Receivers.** • Can be used for line and system-side testing. • Generator can insert selected fixed pattern, pseudo-random bit sequence (PRBS) pattern, or user-programmable patterns from 1 to 32 bits. • All patterns support subrate DS0 or multiple DS0 up to the full bandwidth. • Receiver counts mismatches between received stream and expected pattern. • BERT can be performed on entire payload or on individual DS0s. • Subrate support by selecting any combination of bits in the time slot **Selectable Fixed Patterns: (per: AT&T TR 62411, Telcordia TR-NWT-001219, ITU O.150, O.151, and O.152)** • All ones (marks) • All zeroes (spaces) • Alternating ones and zeroes (1:1) • 1 in 3 (in-band loop-down code) • 1 in 4 (in-band loop-up code) • 1 in 5 • 1 in 7 • 1 in 8 • 1 in 16 • 3 in 24 **Selectable PRBS patterns (per: AT&T TR 62411, Telcordia R-NWT-001219, ITU O.150, O.151, and O.152)** • 2^{6-1} • 2^{7-1} • 2^{8-1} • 2^{9-1} • 2^{11-1} • 2^{15-1} • 2^{20-1} • QRSS (2^{20-1}, with no more than 14 consecutive zeroes) • 2^{23-1}
Pattern Receiver	**User-Programmable Pattern with Programmable Length Up to 32 Bits.** Can detect either a pattern match or an inverse pattern match and integrates the pattern match for the number of bits specified.
Counters	**24-Bit Counter and 24-Bit Error Counter.** The contents of the counters are copied to registers accessible by a host processor in one of the following ways: • The IXF3204 framer is programmed to copy the contents automatically every second. • The host processor sends a load command to the IXF3204 framer.

4.2 Indicators

'Indicators' are IXF3204 framer responses to events such as alarms. Indicators include interrupts, status indicators, and counters that are available to the host processor to convey the state of the IXF3204 framer.

Table 20 lists the main T1 indicators for the IXF3204 framer.

Table 20. Main T1 Indicators (Sheet 1 of 2)

Feature	Description
Out Of Frame (OOF)	**Indicator and Status.** **T1 D4:** An Out Of Frame is forced when there are M errors in a programmable window of N consecutive Ft or Fs bits. M = 1, 2:7 and N = 1, 2:7. Default values are 2 errors in a window of 4. **T1 ESF:** An Out Of Frame is forced when there are M errors in a programmable window of N consecutive Fe bits. M = 1, 2:7 and N = 1, 2:7. Default values are 2 errors in a window of 4. As an option, the user can program the IXF3204 framer so that if the number of CRC6 errors is equal to or exceeds 320 in a one-second interval, an Out of Frame condition is forced. **NOTE:** Synchronization is achieved when either 24 (the default) or 10 (optional) Fe for ESF or Ft/Fs for D4 consecutive bits match the synchronization pattern.
Loss Of Signal (LOS)	**Indicator and Status - Loss Of Signal (LOS).** 175 ± 75 clocks with no pulse transitions (per ANSI T1.231). The user can define the number of consecutive zeroes to declare LOS. The default value is 128. The LOS state is removed if there are at least N ones in a window of M bits. The default value for N is 16 and the default value for M is 128, so that 16/128 results in a 12.5% density being required to remove LOS.
Alarm Indication Signal (AIS)	**Indicator and Status - Alarm Indication Signal (AIS).** A ones' density of at least 99.9% in a window of from 3 milliseconds to 75 milliseconds (per ANSI T1.231 and ITU G.775). As an option, the Out Of Frame (OOF) condition can be used to validate AIS (per ANSI T1.403). The default value is 3 milliseconds. The user can program the window to use to declare AIS. The AIS indication is cleared when the 99.9% density is not met in the 3-ms window.
Remote Alarm Indication (RAI or 'Yellow Alarm')	**Indicator and Status - Remote Alarm Indication (RAI).** **SF and SLC®96. Normal Mode:** • Clears when the set condition is not present. • Sets when bit 2 is '0' in every channel (per ANSI T1.231). • A yellow alarm is declared when the 24 TS have bit 2 set to '0'. **SF Alternate mode (J1 D4 SF):** • Clears when framing bit 12 = '0' for two consecutive superframes • Sets when framing bit 12 = '1' for two consecutive superframes **ESF:** • Clears when the pattern below does not occur in 2 consecutive intervals. • Sets when FDL BOM = 1111 1111 0000 0000 occurs in 16 contiguous pattern intervals.

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Table 20. Main T1 Indicators (Sheet 2 of 2)

Feature	Description
LOF Failure (Red Alarm)	**Loss of Frame (LOF) Failure (Red Alarm).** • Clears when OOF has been removed for a period of 20 seconds or less (per ANSI T1.231). • Sets when an OOF defect persists for a period of 2.5 ± 0.5 seconds. The user can change the clear and set thresholds from 125 microseconds to 8.19 seconds.
LOS Failure	**Loss of Signal (LOS) Failure.** • Clears when LOS has been removed for a period of 20 seconds or less (per ANSI T1.231). • Sets when an LOS defect persists for a period of 2.5 ± 0.5 seconds. The user can change the clear and set thresholds from 125 microseconds to 8.19 seconds.
AIS Failure (Blue Alarm)	**AIS Failure (Blue Alarm).** • Clears when AIS has been removed for a period of 20 seconds or less (per ANSI T1.231). • Sets when an AIS defect persists for a period of 2.5 ± 0.5 seconds. The user can change the clear and set thresholds from 125 microseconds to 8.19 seconds.
COFA	**Change of Frame Alignment (COFA).** COFA is declared when the new frame location is different from the previous one.
CRC6 Errors Indicator and Count	**CRC Errors Latched Indicator.** CRC errors counter
Ft/Fe Bit Errors Indicator and Count	**Framing Error Indication.** Ft (D4) or Fe (ESF) counters
Fs Bit Errors Indicator and Count	**Fs Error Counter and Indicator.** Fs (D4) counters count any Fs bit errors when in the SF mode.
Ft and Fs Errors Indicator and Count	**Counter of Ft Plus Fs Errors and Indicator.** This counter is the counter of the Ft and FS errors and indicator.
Slip Indicator and Count	**Slip Indicator and Counter.** The Slip Indicator and Counter counts either frame deletions or skips.
PRM Detected	**Performance Report Messaging Detected.** PRM Detected is the PRM reception indicator and PRM data.
MOP Detected Indication Plus Other Status Info	**Message-Oriented Protocol Detected.** Message-oriented protocol (MOP)-detected indicators. However, the MOP indicator does not include PRM.
BOP Indication and Count	**Bit-Oriented Protocol Detected Indicator and Value.** The bit-oriented protocol (BOP) is declared detected when it is continuously detected a number of times indicated by the threshold. (Default = 10.)
Japanese Application Support	**Compliance with JT-G.704.** • Yellow Alarm generation and detection • CRC checking and transmission.

Table 21 lists the main E1 indicators for the IXF3204 framer.

Table 21. Main E1 Indicators (Sheet 1 of 2)

Feature	Description
Out Of Frame (OOF), Out of CRC Multiframe, Out of CAS Multiframe	**Out of Frame Conditions.** Out of Frame conditions include the following. • **Out of (Basic) Frame:** Three consecutive errors in FAS or three consecutive errors in NFAS generate an OOF condition. • **Out of CRC Multiframe:** • An Out of CRC Multiframe event occurs if two consecutive errors are received in the CRC multiframe alignment signal. • As an option, if 915 or more CRC errors are detected in a one-second interval, then the reframe process is started (per ITU G.706.) • **Out of CAS Multiframe:** An Out of CAS Multiframe event occurs either when: • Two consecutive CAS multiframe alignment words are received in error. • All TS16 in a multiframe are '0' (optional). **NOTE:** The IXF3204 framer gets basic frame alignment (BFA) first and then starts checking for CRC or CAS multiframes, depending on the selected mode. Whenever an OOF condition exists, CAS and CRC multiframes are also lost.
Loss Of Signal (LOS)	**Loss of Signal (per ITU G.775).** • Clears when there is at least one transition in a window of 10 to 255 bits. The windows are user programmable. • Sets when there are no transitions in a window of from 10-bit to 255-bit periods. *-Or-* **(per ITU I.431, ETS 300 233):** • Clears when the programmable ones' density is met. • Sets when there are no transitions in a window of 1-ms (2048 bits). As an option, the user can program both the number of consecutive zeroes to declare a LOS state and the ones' density to remove the LOS state. **NOTE:** • The default value to clear LOS is 16 transitions in a window of 128-bit periods (12.5% ones' density). • The default value to set LOS is a 128 consecutive zeroes.
Blue Alarm (AIS)	**Blue Alarm (per ITU G.775).** • Clears when each of two consecutive double-frame periods have three or more zeroes or when the Frame Alignment Signal (FAS) is found. • Sets when less than three zeroes are detected in each of two consecutive double-frame periods. (Each double-frame period is 512 bits.) **NOTE:** As an option, if OOF is set and there are less than three zeroes in a 512-bit period (per ETS 300 233), the blue alarm can be set.
Remote Alarm Indication (RAI)	**Remote Alarm Indication (per ITU G.775).** • Clears when bit 3 of time slot 0 in NFAS frames = '0' for three consecutive times. • Sets when bit 3 in time slot 0 of NFAS frames = '1' for three consecutive times.

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Table 21. Main E1 Indicators (Sheet 2 of 2)

Feature	Description
Remote Multiframe Alarm (TS16 RAI)	**Remote Multiframe Alarm (per ITU G.704).** • Clears when bit 6 of time slot 16 of frame 0 = '0' for two consecutive multiframes. • Sets when bit 6 of time slot 16 of frame 0 = '1' for two consecutive multiframes.
TS 16 AIS	**TS 16 AIS (per ITU G.775).** • Clears when each of two consecutive multiframe periods contain four or more zeroes or when the Multiframe Alignment Signal (MFAS) is found. • Sets when there are less than 4 zeroes in TS16 in each of two consecutive multiframes.
COFA	**Change of Frame Alignment (COFA).** COFA is declared when a new frame location is different from a previous one.
AUX-P	**AUX-P.** • Clears when two or more errors in the pattern '10' are detected in a 512-bit window. • Sets when the sequence '10' is detected in a 512-bit window with no error or only one error.
LOF Failure (Red Alarm)	**LOF Failure (Red Alarm).** • Clears when OOF has been removed for 20 seconds or less. • Sets when an OOF defect persists for 2.5 ± 0.5 seconds. **NOTE:** The user can define the clear and set thresholds in the range 125 microseconds to 8.19 seconds.
LOS Failure	**LOS Failure.** • Clears when LOS has been removed for 20 seconds or less. • Sets when an LOS defect persists for 2.5 ± 0.5 seconds. **NOTE:** The user can define the clear and set thresholds in the range 125 microseconds to 8.19 seconds.
AIS Failure (Blue Alarm)	**AIS Failure (Blue Alarm).** • Clears when AIS has been removed for 20 seconds or less. • Sets when an AIS defect persists for 2.5 ± 0.5 seconds. **NOTE:** The user can define the clear and set thresholds in the range 125 microseconds to 8.19 seconds.
CRC Errors Indicator and Counter	**CRC Errors Indicator and Counter.** The CRC Errors Indicator and Counter counts CRC errors.
FAS Errors Indicator and Counter	**FAS Error Indicator and Counter.** The FAS Errors Indicator and Counter counts FAS errors.
FAS and NFAS Errors Indicator and Counter	**FAS and NFAS Errors Indicator and Counter.** The FAS and NFAS Errors Indicator and Counter counts FAS and NFAS errors.
Slip Indicator and Counter	**Slip Indicator and Counter.** The Slip Indicator and Counter counts slips.

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5.0 Initialization, Reset, and Interrupts

5.1 Initialization

The following process initializes the IXF3204 framer:

1. Perform a reset by using either a hardware reset or a software reset. (See Section 5.2, “Reset”.)
2. Remove the IXF3204 framer from the reset state.
3. Load the firmware into the IXF3204 framer address range 8000h to BFFFh.
4. Enable the internal processor by writing value 00h to the CPUREG register at address 0003h.
   After loading and enabling the firmware, the value the IXF3204 framer internal processor writes in register 1D0Fh is the revision ID of the firmware just loaded. The value for the revision ID is any number other than 0x00h.
5. Wait for the internal processor to indicate it is ready, which is done by reading register 1D0Fh. The value after reset is ‘0’.

At this point, the host processor can start configuring each of the IXF3204 framer modules.

5.2 Reset

Register 0000h is the reset register, RST. This register is set to 00h by the hardware reset.

Once the hardware reset is removed, the IXF3204 framer can be set into the reset state by writing A1h to the register 00h. The reset state is maintained as long as the value is maintained. The IXF3204 framer can be removed from the reset state by writing a 00h to RST.

There is also a software reset signal that affects only the IXF3204 framer internal processor. Register CPURST at address 03h can be used to control this operation. After hardware or software reset, this register is set to 01h. If the host processor requires only to reset the IXF3204 internal CPU, it must write 01h to CPURST, which is held in the reset state as long as CPURST = 01h.

5.3 Interrupt Handling

The host processor interacts with the IXF3204 framer with configuration, control, and status operations performed through direct read and write transfers. The IXF3204 framer requests servicing by asserting the interrupt line. The host processor enables generation of interrupts by programming interrupt masks. Both the interrupts and the masks are hierarchical.

The host processor works in:

- Polling mode by masking the interrupt ball INTB and monitoring the indicators.
- Interrupt mode by allowing the propagation of selected interrupts to interrupt ball INTB.

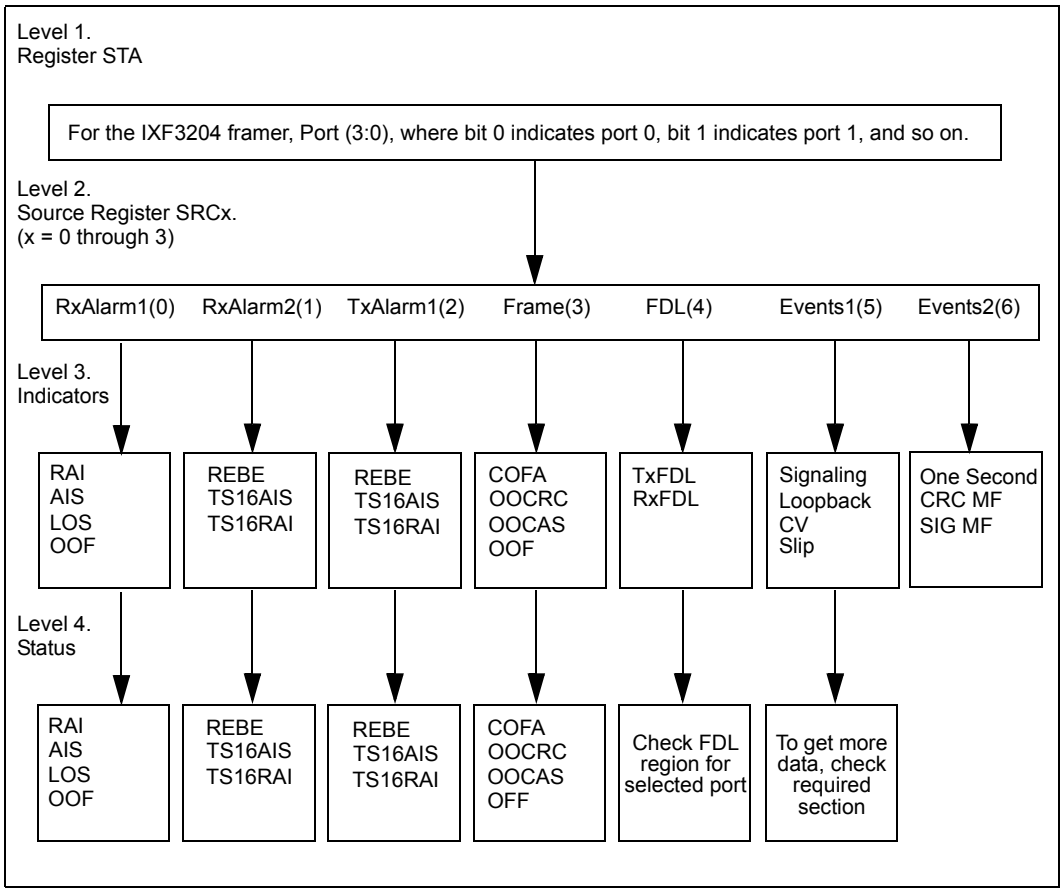
5.3.1 Interrupt Handling - Events Related to Framer Ports

Figure 5 shows how interrupt handling is performed by Register STA, which is used for events related to IXF3204 framer ports.

- Level 1- Indicates the port that is generating the interrupt.
- Level 2 - Indicates the module that is generating the interrupt: RxAlarm1, RxAlarm2, TxAlarm1, Frame, FDL, Events1, or Events2. [The numbers in parentheses indicate the bit position in the SRC register. For example, RxAlarm1(0) indicates that RxAlarm is bit 0 in the SRC register.]
- Level 3 - Indicates the associated indicator register bit (such as RAI or AIS) that is generating the interrupt.
- Level 4 - Indicates the associated status register bit (such as RAI or AIS) that is used to indicate the interrupt status.

Note: Certain registers, such as Events2, do not have an associated status register because an interrupt provides all required information. Once this interrupt is generated, it shows a sequence to follow to see which event caused the interrupt. This situation applies to one-second, CAS, or CRC multiframe period interrupts.

Figure 5. Intel® IXF3204 Framer Interrupt Handling - Register STA



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5.3.2 Interrupt Handling - Events Related to HDLC and BERT

Figure 6 shows how interrupt handling is performed by Register STB, which is used for events related to HDLC and BERT functional units.

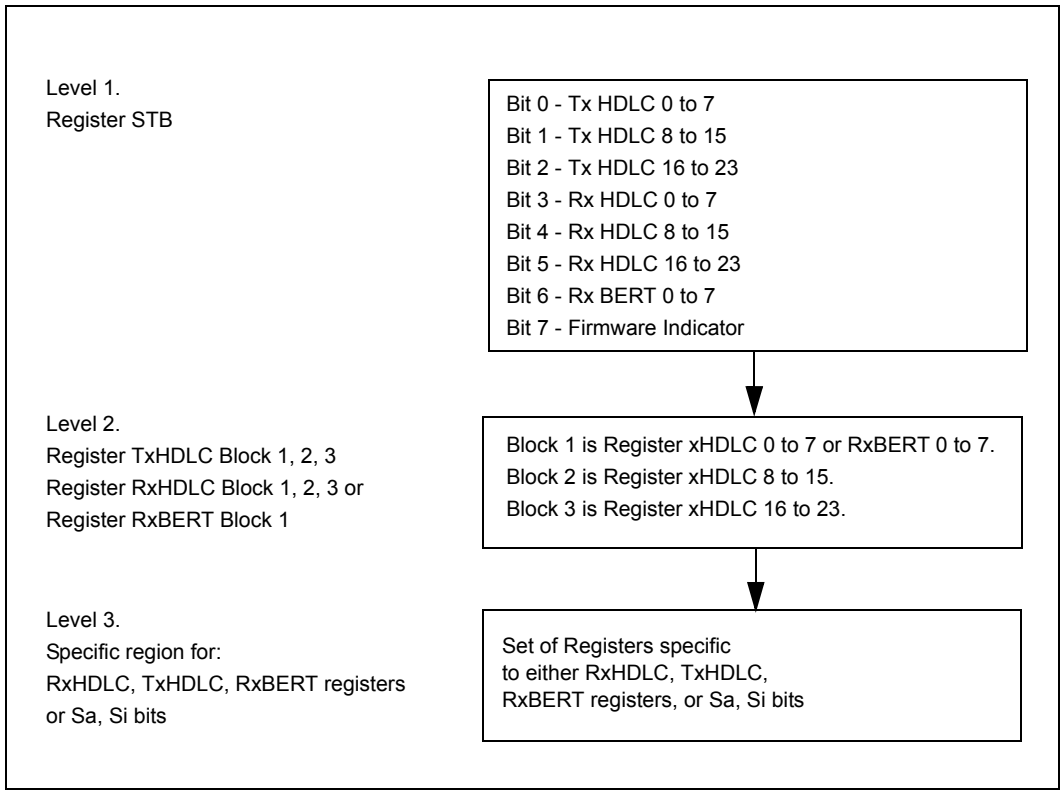
There are masks for the HDLC and BERT functional units, and these masks are hierarchical. Since the HDLC and BERT functional units can be associated with any port, a set of registers provides to the host processor information of where the event occurred within either HDLC or BERT unit. The host processor then must go to the respective memory region to obtain the correct status.

- Level 1 - Indicates the register group that is generating the interrupt.
- Level 2 - Indicates the associated register block in which the event occurred.
- Level 3 - Indicates the respective memory region the host processor goes to obtain the correct status regarding the event.

Note: The IXF3204 framer firmware has two bytes of indicators, each with its respective mask byte that reports new values for all of the following:

- Sa bits (8:4) and Si bits of the received stream
- An interworking state
- An indicator that shows when the processing for the database is complete.

Figure 6. Intel® IXF3204 Framer Interrupt Handling - Register STB



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6.0 T1 Framers

This chapter discusses the following T1 framer topics:

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6.1 T1 Line Coding

The IXF3204 framer provides T1 line coding and decoding functions to support non-coding line-interfaces and to facilitate performance monitoring.

The following sections detail the supported T1 line coding formats and associated functions. Unless stated, coding is separately selectable in both the receive- and transmit-sides of each port through the port-configuration registers.

- Section 6.1.1, "T1 Alternate Mark Inversion"
- Section 6.1.2, "T1 Zero Code Suppression"
- Section 6.1.3, "T1 Binary Eight Zero Substitution"

6.1.1 T1 Alternate Mark Inversion

Alternative Mark Inversion (AMI) is a Return-to-Zero (RZ) format per ITU G.703. In this format:

- A binary zero (or 'space') is represented by the absence of a pulse.
- A binary one (or 'mark') is represented by either a positive- or negative-going pulse.

Each consecutive pulse alternates in polarity (for example, a positive pulse must always be followed by a negative pulse, and a negative pulse must always be followed by a positive pulse) regardless of the number of intervening spaces between the two pulses. As a result, alternating marks are inverted.

Two consecutive pulses of the same polarity are known as a Bipolar Violation (BPV). To monitor performance, the IXF3204 framer actively monitors the line signal and provides a count of detected BPVs. By definition, all T1 line signals use basic AMI line coding. However, because T1 receivers rely on the presence of marks in the signal to recover clocking, various standards specify maximum-space and minimum-mark density requirements.

AMI coding alone does not provide a method to ensure compliance to mark/space requirements. However, the IXF3204 framer does provide a means of enforcing the ones' density requirement, as described in Section 6.1.2, "T1 Zero Code Suppression" and Section 6.1.3, "T1 Binary Eight Zero Substitution".

Note: The term 'AMI coding' indicates no specific methods are used to suppress excess zeroes in a signal.

6.1.2 T1 Zero Code Suppression

Zero Code Suppression (ZCS), also referred to as ‘Bit 7’ (B7) coding, is used to ensure the T1 mark density requirement is met per Telcordia TR-TSY-510. When the 8-bit word (bits 0 to 7) of any T1 channel consists of all zeroes (0000 0000), the bit in position 7 is forced to a ‘1’ (0000 0010).

ZCS is performed on transmitted data only. There is no ZCS decoding function defined since the receiver cannot differentiate between a ZCS-coded ‘0000 0010’ word, and an actual ‘0000 0010’ word. In SF and SLC®96 mode, the RAI (or ‘Yellow Alarm’) insertion occurs before ZCS coding.

(For information on how to enable use of ZCS, see the memory map document for the IXF3204 framer.)

6.1.3 T1 Binary Eight Zero Substitution

Zero Code Suppression works well for voice-band data but it has limitations with digital data. T1 binary Eight Zero Substitution (B8ZS), per ANSI T1.102, overcomes these limitations. B8ZS supports clear-channel (64 kbps) data and is compatible with all standard T1 framing formats. In B8ZS coding, eight consecutive zeroes in the T1 data stream are replaced by the B8ZS substitution pattern of ‘000V B0VB’, in which ‘V’ is an intentional bipolar violation (BPV) and ‘B’ is a valid bipolar mark.

The polarity of the BPVs and marks depends upon the polarity of the last mark before the ‘eight zero’ occurrence. The B8ZS substitution pattern is made regardless of where the eight consecutive zeroes occur in the datastream, including framing, signaling, and alarm bits.

In contrast to ZCS, which operates on data within a DS0 channel, B8ZS coding can occur across frame boundaries. The IXF3204 framer performs both B8ZS coding (on the T1 transmitted signal) and B8ZS decoding (on the T1 received signal). Received BPVs that are part of the B8ZS pattern are not counted as BPVs in the coding error counter of the port status register.

(For information on how to select B8ZS coding and decoding, see the memory map document for the IXF3204 framer.)

6.2 T1 Line Monitoring

Before framing occurs, the T1 line signal is monitored for the following alarms and impediments:

- Section 6.2.1, "T1 Alarm Indication Signal"
- Section 6.2.2, "T1 Bipolar Violations"
- Section 6.2.3, "T1 Excess Zeroes"
- Section 6.2.4, "T1 Loss of Signal"

6.2.1 T1 Alarm Indication Signal

A T1 Alarm Indication Signal (also known as 'Blue Alarm' or AIS) is declared when less than five spaces are detected in a 3-ms window of data, per ANSI T1.231, ITU G.775, and ANSI T1.403. This condition must be detected in the presence of a 1.0^{-03} Bit Error Rate (BER). When the IXF3204 framer detects AIS, the appropriate bit in a status register is set and a host processor interrupt is generated, unless the interrupt is masked. The window to declare AIS can be set from 3 to 42 milliseconds, and the default value is 3 milliseconds. The user can select AIS to be validated with OOF (ANSI T1.403). As an option, OOF can be used to validate the AIS condition. (For more information, see Section 6.14, "T1 Blue Alarm".)

6.2.2 T1 Bipolar Violations

A Bipolar Violation (BPV) is defined as two consecutive pulses (or 'marks') of the same polarity. To monitor performance, the IXF3204 framer actively monitors the line signal and provides a status register count of detected BPVs. Every second, the contents of the IXF3204 framer internal counter are copied to a register accessible by the host processor.

6.2.3 T1 Excess Zeroes

When an occurrence of Excess Zeroes (EXZ) is declared is dependent on the line-coding format, per ANSI T1.231. When the line-coding format is:

- HDB3, an EXZ occurs when 4 or more consecutive zeroes are detected.
- B8ZS, an EXZ occurs when 8 or more consecutive zeroes are detected.
- AMI, an EXZ occurs when 16 or more consecutive zeroes are detected.

Note: To monitor performance, the IXF3204 framer monitors the line signal for any violations of the maximum space rule and provides a count of EXZ occurrences.

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6.2.4 T1 Loss of Signal

A T1 Loss of Signal (LOS) is defined as any period of 175 +/- 75 clock cycles in which no pulse transitions occur, per AT&T TR 62411, ANSI T1.231, and ITU G.775. The IXF3204 framer monitors the line signal for LOS occurrences. When the IXF3204 framer detects LOS, the appropriate bit in the port status register is set and a host processor interrupt is generated (unless masked).

The LOS condition is not cleared until the mark density is at least 12.5% for the interval defined in the appropriate specification. The alarm threshold is programmable by modifying the window of measurement and the density of zeroes in that window to clear the condition as well as the number of consecutive zeroes to declare LOS.

6.3 T1 Insertion of Line Errors

For T1 testing, the IXF3204 framer supports the controlled insertion of the following types of line errors.

- Framing errors (See Section 6.10.1, “T1 Frame Bit Error Insertion”.)
- CRC errors, at rates from continuous to one in a million (See Section 6.10.2, “T1 CRC Error Insertion”.)
- Bipolar Violation (BPV) errors (discussed in the following text)

For B8ZS, ZCS, or AMI modes, the IXF3204 framer transmitter can be programmed to insert BPV errors. The IXF3204 framer error insertion register allows insertion of either single BPVs or insertions at a rate of from 100% (that is, insert continuous BPVs) up to 10^{-6} (that is, insert a BPV once every million of marks).

For T1, BPV insertions are subject to the following conditions:

- B8ZS zero-suppression coding is not violated.
- During Line Loopback, BPV insertion is not performed even if it is enabled.
- If the IXF3204 framer detects a DS1 in-band network loopback code, the IXF3204 framer enters a line loopback. As a result, any BPV insertions that are enabled are then disabled.
- If the IXF3204 framer has a full or partial payload loopback code (DS0s) and if BPV insertion is not desired during this loopback BPV, then insertion must be manually disabled.
- BPV insertion does not violate data integrity.

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6.4 T1 Framing

Table 22 lists the structure of a basic T1 frame.

Table 22. T1 Basic Frame Structure

Parameter	Value
Bit rate	1.544 Mbps
Frame length	193 bits, consisting of: • 1 overhead framing bit (known as the 'F bit') per frame • 192 payload bits
Frame period	125 microseconds
Frame rate	8 kHz
Payload (or 'Channelization')	24 channels (also known as 'time slots') with 8 bits/channel
Channel rate	64 Kbps

In the transmit direction, the IXF3204 framer can do one of the following:

- Internally generate the Framing (F) bits for the various multi-framing modes using the system backplane synchronization frame pulses selected through the TxFramer registers, bits B4:2.
- Provide F bits from the system backplane and pass them transparently to the line interface by selecting the transparent mode in the TxFramer register.

In the receive direction, the IXF3204 framer can do one of the following:

- Transport the F bit in a totally dedicated time slot into the system backplane data stream (backplane rate at 2.048 Mbps).
- Integrate the F bits for the various multi-framing modes into the system backplane data stream (backplane rate at 1.544 Mbps).
- Strip the F bits, providing only the channelized payload data with the appropriate frame synchronization pulse outputs (backplane rate at 1.536 Mbps).

The basic frame format is combined into various T1 multiframe formats, described in the following sections: Section 6.5, "T1 Superframe" through Section 6.7, "T1 Extended SuperFrame".

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6.5 T1 Superframe

To select the T1 Superframe (SF) mode per ANSI T1.107 and T1.403, program the appropriate configuration register bits associated with the Rx and Tx direction.

6.5.1 T1 SF Mode Description

The T1 SF mode (also known as 'D4 framing') consists of 12 consecutive basic T1 frames, with 1 F bit and 192 payload bits per frame. Table 23 lists the two groups of F bits:

- Six terminal-framing (Ft) bits, used to identify frame boundaries
- Six signaling-framing (Fs) bits, used to identify robbed-bit signaling frames and superframe boundaries

Table 23. T1 SF Frame Structure

Frame Number	Framing (F) Bits			Time Slot Bit Usage			
	Bit Number	Terminal Framing (Ft) Bit	Signaling Framing (Fs) Bit	Pulse-Code Modulation Format	Signaling, If Used	Signaling Bit Definition	
						2-State	4-State
1	1	1	-	1-8	-	-	-
2	194	-	0	1-8	-	-	-
3	387	0	-	1-8	-	-	-
4	580	-	0	1-8	-	-	-
5	773	1	-	1-8	-	-	-
6	966	-	1	1-7	8	A	A
7	1159	0	-	1-8	-	-	-
8	1352	-	1	1-8	-	-	-
9	1545	1	-	1-8	-	-	-
10	1738	-	1	1-8	-	-	-
11	1931	0	-	1-8	-	-	-
12	2124	-	0	1-7	8	A	B

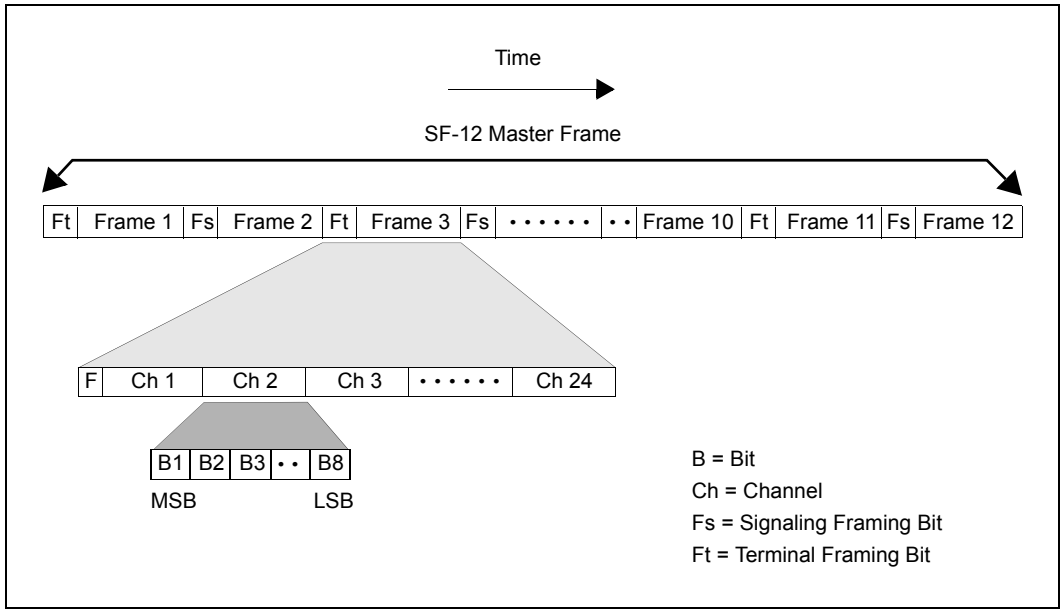
6.5.2 T1 SF Framing Algorithm

The IXF3204 framer receive framer declares SF/D4 frame synchronization when it detects a pre-determined number of consecutive correct framing bits Ft and Fs. The detection threshold can be set either to 24 Ft bits and 24 Fs bits (the default) or to 10 Ft bits and 10 Fs bits. If the IXF3204 framer does not find valid frame synchronization, then it restarts the framing algorithm. The framing search can be set either to look for both the Ft and Fs patterns (to achieve frame synchronization) or to look only for Ft bits.

- Ft Bits alone can be used to validate framing, or Ft bits qualified with Fs bits can be used to validate framing.
- While in frame, the IXF3204 framer monitors both Ft and Fs bits for F bit and Loss of Frame errors.

Figure 7 shows the IXF3204 framer T1 SF frame structure.

Figure 7. T1 SF Frame Structure



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6.6 T1 SLC®96 Mode

To select the SLC®96 mode per Telcordia TR-TSY-008 and GR-303, program the IXF3204 framer configuration register framer bits for either the Rx and Tx direction, as appropriate.

6.6.1 T1 SLC®96 Description

The SLC®96 system is a digital subscriber loop carrier system that utilizes a modified SF framing format on one or more of four T1 lines serving 96 subscribers. The Fs bit represented in the SF framing pattern is periodically replaced with a low-speed data link called the Derived Data Link (DDL). The SLC®96 master frames are 9 milliseconds long and have six SF superframes (72 frames total).

In this format, Ft bits are located in odd-numbered frames and consist of the standard 101010... repeating pattern. The pattern for Fs bits consists of a 0001 1100 0111 binary sequence in the F-bit position of even frames from 2 through 22 and frame 72 (12 bits total). The Fs bit position in the even frames from 24 through 70 contain the 24 bits that make up the SLC®96 DDL.

Table 24 lists the entire SLC®96 multiframe structure. DDL operation requires bits to be sourced and interpreted by a host processor. For signaling information, see Section 10.2.1, "T1 Channel-Associated (Robbed-Bit) Signaling".

Note: In Table 24, the letters C, M, A, and S represent respectively: Concentrator, Maintenance, Alarm, and Line-Switched Field bits. The Spoiler Bits ('S = n') are used to prevent spurious superframe synchronization.

Table 24. T1 SLC®96 Multiframe Structure (Sheet 1 of 3)

Frame Number	Bit Number	Framing (F) Bits			Bit Use In Each Time Slot	
		Terminal Framing Big (Ft)	Signaling Framing Bit (Fs)	Derived Data Link	Pulse-Code Modulation Format	Signaling Bit Definition
1	1	1	-	-	B1-B8	-
2	194	-	0	-	B1-B8	-
3	387	0	-	-	B1-B8	-
4	580	-	0	-	B1-B8	-
5	773	1	-	-	B1-B8	-
6	966	-	1	-	B1-B7	B8(A)
7	1159	0	-	-	B1-B8	-
8	1352	-	1	-	B1-B8	-
9	1545	1	-	-	B1-B8	-
10	1738	-	1	-	B1-B8	-
11	1931	0	-	-	B1-B8	-
12	2124	-	0	-	B1-B7	B8(B)
13	2317	1	-	-	B1-B8	-
14	2510	-	0	-	B1-B8	-
15	2703	0	-	-	B1-B8	-

Table 24. T1 SLC®96 Multiframe Structure (Sheet 2 of 3)

Frame Number	Bit Number	Framing (F) Bits			Bit Use In Each Time Slot	
		Terminal Framing Big (Ft)	Signaling Framing Bit (Fs)	Derived Data Link	Pulse-Code Modulation Format	Signaling Bit Definition
16	2896	-	0	-	B1-B8	-
17	3089	1	-	-	B1-B8	-
18	3282	-	1	-	B1-B7	B8(A)
19	3475	0	-	-	B1-B8	-
20	3668	-	1	-	B1-B8	-
21	3861	1	-	-	B1-B8	-
22	4054	-	1	-	B1-B8	-
23	4247	0	-	-	B1-B8	-
24	4440	-	-	C1	B1-B7	B8(B)
25	4633	1	-	-	B1-B8	-
26	4826	-	-	C2	B1-B8	-
27	5019	0	-	-	B1-B8	-
28	5212	-	-	C3	B1-B8	-
29	5405	1	-	-	B1-B8	-
30	5598	-	-	C4	B1-B7	B8(A)
31	5791	0	-	-	B1-B8	-
32	6984	-	-	C5	B1-B8	-
33	6177	1	-	-	B1-B8	-
34	6370	-	-	C6	B1-B8	-
35	6563	0	-	-	B1-B8	-
36	6756	-	-	C7	B1-B7	B8(B)
37	6949	1	-	-	B1-B8	-
38	7142	-	-	C8	B1-B8	-
39	7335	0	-	-	B1-B8	-
40	7528	-	-	C9	B1-B8	-
41	7721	1	-	-	B1-B8	-
42	7914	-	-	C10	B1-B7	B8(A)
43	8107	0	-	-	B1-B8	-
44	8300	-	-	C11	B1-B8	-
45	8493	1	-	-	B1-B8	-
46	8686	-	-	S = 0	B1-B8	-
47	8879	0	-	-	B1-B8	-
48	9072	-	-	S = 1	B1-B7	B8(B)
49	9265	1	-	-	B1-B8	-
50	9458	-	-	S = 0	B1-B8	-

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Table 24. T1 SLC®96 Multiframe Structure (Sheet 3 of 3)

Frame Number	Bit Number	Framing (F) Bits			Bit Use In Each Time Slot	
		Terminal Framing Big (Ft)	Signaling Framing Bit (Fs)	Derived Data Link	Pulse-Code Modulation Format	Signaling Bit Definition
51	9651	0	-	-	B1-B8	-
52	9844	-	-	M1	B1-B8	-
53	10037	1	-	-	B1-B8	-
54	10230	-	-	M2	B1-B7	B8(A)
55	10423	0	-	-	B1-B8	-
56	10626	-	-	M3	B1-B8	-
57	10809	1	-	-	B1-B8	-
58	11002	-	-	A1	B1-B8	-
59	11195	0	-	-	B1-B8	-
60	11388	-	-	A2	B1-B7	B8(B)
61	11581	1	-	-	B1-B8	-
62	11774	-	-	S1	B1-B8	-
63	11967	0	-	-	B1-B8	-
64	12160	-	-	S2	B1-B8	-
65	12353	1	-	-	B1-B8	-
66	12546	-	-	S3	B1-B7	B8(A)
67	12739	0	-	-	B1-B8	-
68	12932	-	-	S4	B1-B8	-
69	13125	1	-	-	B1-B8	-
70	13318	-	-	S = 1	B1-B8	-
71	13511	0	-	-	B1-B8	-
72	13704	-	0	-	B1-B7	B8(B)

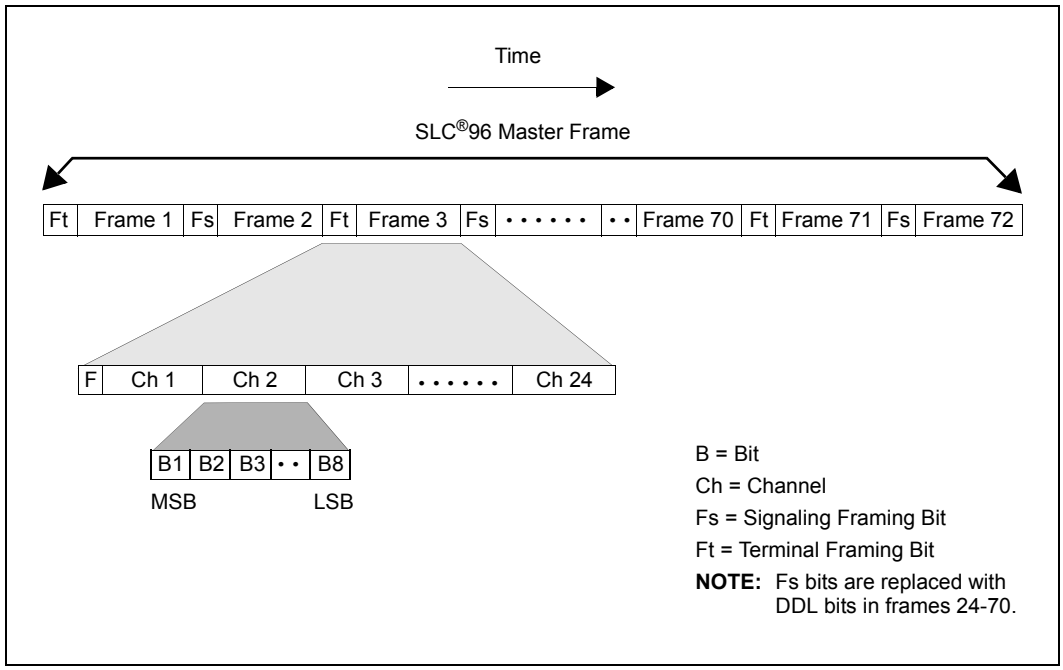
6.6.2 T1 SLC®96 Framing Algorithm

The IXF3204 framer receive framer declares SLC®96 frame synchronization when a complete frame sequence is detected, including the spoiler bits. If valid frame synchronization is not found, then the framing algorithm is restarted. To prevent spurious Fs synchronization, four spoiler bits are incorporated into the DDL block.

- Ft, Fs, and spoiler bits are used to validate framing. A complete frame must be detected before declaring synchronization.
- While in frame, Ft and (non-DDL) Fs bits are monitored for frame errors.

Figure 8 shows the IXF3204 framer T1 SLC®96 frame structure.

Figure 8. T1 SLC®96 Frame Structure



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6.7 T1 Extended SuperFrame

To select the T1 Extended SuperFrame (‘ESF’) mode per ANSI T1.107 and T1.403, program the IXF3204 framer configuration register framer bits for either the Rx and Tx direction, as appropriate.

6.7.1 T1 ESF Description

The T1 ESF format consists of 24 consecutive basic T1 frames. The corresponding 24 F bits are used for a variety of functions, described as follows:

- Framing, a 2 kbit pattern. — This function relates to the terminal synchronization channel, in which frame and superframe alignment is provided by the F-bit of frames 4, 8, 12, 16, 20, and 24. This sequence is referred to as the Framing Pattern Sequence (FPS). The bits included in this sequence are called ‘Fe’ bits. The repeating pattern is 001011 binary, and it uses 6 F bits per extended superframe.
- Facility Data Link (FDL), a 4 kbps pattern. — The FDL function is carried by the odd F bits, using 12 F bits per extended superframe. The FDL is described in Section 12.0, “Facility Data Link”.
- Error detection, a 2 kbps pattern. — This function relates to the Cyclic Redundancy Check (CRC) bits that carry the CRC-6 code of the preceding superframe is located in F bit of frames 2, 6, 10, 14, 18, 22. (Error detection uses 6 F bits per extended superframe.) CRC-6 procedures are discussed in the following section, Section 6.7.2, “T1 ESF CRC-6 Procedures”.

6.7.2 T1 ESF CRC-6 Procedures

The CRC-6 is a method of performance monitoring per ITU G.706 that is carried in the F bit position of frames 2, 6, 10, 14, 18, and 22. The CRC-6 bits computed on the 4,632 bits of ESF (n) are transmitted in ESF (n+l) as per CCITT G.704. At the receiver, the CRC-6 bits are computed again based on the received superframe and compared with the CRC-6 check bits received in the subsequent superframe. The compared check bits are identical in the absence of transmission errors.

In calculating CRC-6 bits, the F bits are replaced by binary ones. All information in other bit positions is identical to the information in the corresponding multiframe bit positions.

Note: An alternate method of calculating the CRC-6 bits is used for J1 1.544 Mbps 24-frame Multiframe mode only. The algorithm is similar to that described in Section 6.6.2, “T1 SLC®96 Framing Algorithm” and the actual F bits are used in the calculation (instead of being replaced by ones).

A programmable option that ensures against false framing confirms Fe candidates by CRC-6 verification. Other T1 CRC options are available as follows:

- Section 6.7.2.1, “T1 ESF CRC-6 Options on the Transmit Side”
- Section 6.7.2.2, “T1 ESF CRC-6 Options on the Receive Side”

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6.7.2.1 T1 ESF CRC-6 Options on the Transmit Side

T1 ESF CRC-6 options on the transmit side include the following:

- The CRC-6 bits are computed by the IXF3204 framer internally on the output data sent to the LIU for transmission in the default mode.
- The CRC-6 bit positions in the transparent input transmit serial data stream are sent to the line when the transparent mode of CRC-6 is selected.

The CRC is calculated before ones-density enforcement (if selected) is performed. When an ESF frame is sent, the CRC-6 bits are computed and transmitted in the bit positions listed in Table 25. The CRC-6 bits computed on the 4,632 bits of ESF(N) are transmitted in ESF(N+1). The check bits Cl through C6 contained in ESF(N+1) are always to be those associated with the contents of ESF(N), immediately preceding ESF. When there is no ESF immediately preceding, the check bits may be assigned any value.

6.7.2.2 T1 ESF CRC-6 Options on the Receive Side

T1 ESF CRC-6 options on the receive side include the following:

- The IXF3204 framer can be set either to perform no verification or to check CRC-6 before declaring a valid frame alignment.

Error verification is performed by recomputing the CRC bits and comparing the result to the received CRC-6 bits of the previous superframe. In case of an error, the CRC error counter is incremented.

6.7.3 T1 ESF Framing Algorithm

Multiframe alignment in ESF mode requires that the proper ordering of Fe bits be found before multiframe alignment is declared. The user can program 24 bits (the default) or 10 bits to be validated before declaring synchronization. Multiframe alignment can be further qualified with a programmable option to validate the alignment by CRC-6 verification. When the programming option is enabled, framing is declared only if the Fe bits sequence is correct for 24 consecutive bits and the CRC-6 calculation matches the expected one. If both conditions are not met, a new search starts.

Table 25 lists the T1 ESF frame structure, where ‘m’ is the bit that carries the FDL information, ‘A’ and ‘B’ are signaling bits, and ‘e1’ to ‘e6’ are the CRC calculation bits.

Table 25. T1 ESF Frame Structure

Frame Number	F Bits				Time Slot Bit Usage		Signaling Bit Definition		
	Bit Number	Framing Bit (Fe)	Facility Data Link	CRC-6	Pulse-Code Modulation Format	Signaling (If Used)	2-State	4-State	16-State
1	1	-	m	-	1-8	-	-	-	-
2	194	-	-	e1	1-8	-	-	-	-
3	387	-	m	-	1-8	-	-	-	-
4	580	0	-	-	1-8	-	-	-	-
5	773	-	m	-	1-8	-	-	-	-
6	966	-	-	e2	1-7	8	A	A	A
7	1159	-	m	-	1-8	-	-	-	-
8	1352	0	-	-	1-8	-	-	-	-
9	1545	-	m	-	1-8	-	-	-	-
10	1738	-	-	e3	1-8	-	-	-	-
11	1931	-	m	-	1-8	-	-	-	-
12	2124	1	-	-	1-7	8	A	B	B
13	2317	-	m	-	1-8	-	-	-	-
14	2510	-	-	e4	1-8	-	-	-	-
15	2703	-	m	-	1-8	-	-	-	-
16	2896	0	-	-	1-8	-	-	-	-
17	3089	-	m	-	1-8	-	-	-	-
18	3282	-	-	e5	1-7	8	A	A	C
19	3475	-	m	-	1-8	-	-	-	-
20	3668	1	-	-	1-8	-	-	-	-
21	3861	-	m	-	1-8	-	-	-	-
22	4054	-	-	e6	1-8	-	-	-	-
23	4247	-	m	-	1-8	-	-	-	-
24	4440	1	-	-	1-7	8	A	B	D

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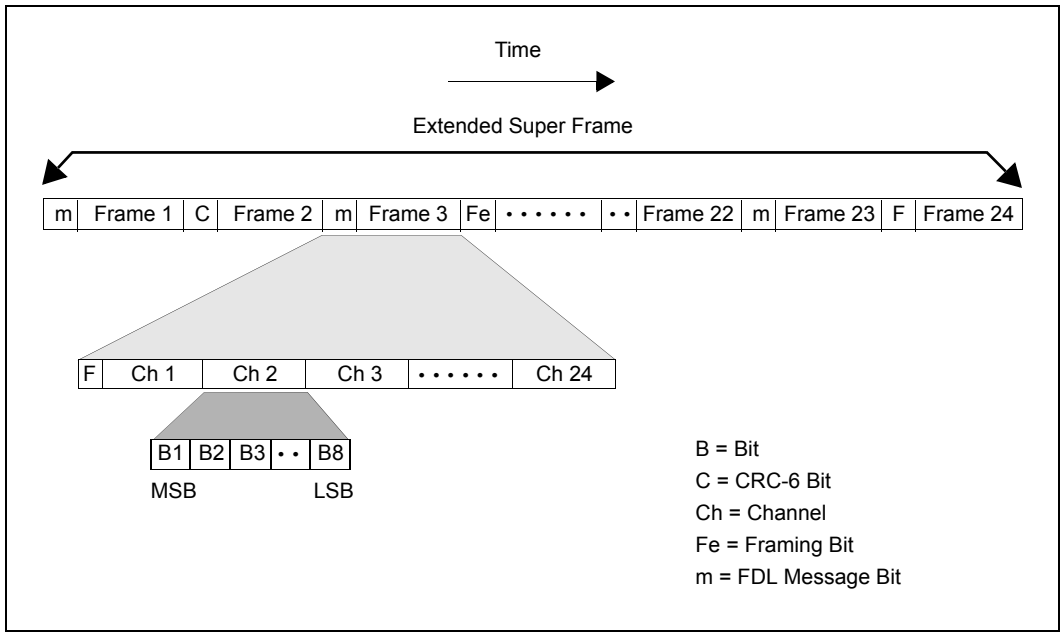
Figure 9 shows the T1 ESF frame structure.

Figure 9. T1 ESF Frame Structure



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6.8 T1 General Framing Properties

This section details T1 general framing properties not covered elsewhere.

6.8.1 T1 False Framing Protection

Table 26 lists for each T1 framing mode a corresponding method for preventing false framing per Telcordia TR-TSY-000507.

Table 26. T1 False Framing Prevention

Framing Mode	False Framing Prevention Method
SF/D4	Ft framing bits coupled with Fs framing bits
SLC®96	Ft framing bits coupled with Fs framing bits and spoiler bits
ESF	Fe framing bits coupled with CRC-6 error detection bits

6.8.2 T1 Maximum Average Reframe Time

The maximum average reframe time is defined as the difference between (1) the instance a known good pseudo-random DS-1 framed signal is applied to the receiver and (2) a valid framed and channelized signal is observed at the output of the receiver when the maximum number of frame positions are examined. The maximum average reframe time applies to a signal with no errors and assumes all bits besides the framing bits have an equal probability of being a zero or one.

Table 27 lists for each T1 framing mode the maximum average reframe time and the corresponding specification.

Table 27. T1 Maximum Average Reframe Time

Framing Mode	Maximum Average Reframe Time (ms)	Specification
SF/D4	50	ITU G.704
SLC®96	50	Telcordia TR-TSY-8
ESF	15	ITU G.706

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6.9 T1 Framing Indicators

6.9.1 T1 Frame Bit Error

The IXF3204 framer monitors individual frame bits (that is, Ft or Fs for SF) for errors. Every second, the IXF3204 framer provides an indication of individual bit errors, along with a maskable interrupt when an error occurs and a count of individual errors.

6.9.2 T1 Out-of-Frame Detection

An Out of Frame (OOF) condition is declared when a particular ratio of framing bits is determined to be in error. The user can select the OOF ratio by setting the appropriate bits in the configuration register. The user can select any window from 1 to 7 and any error threshold from 1 to 7.

Table 28 lists the most common selectable combination of bits and ratios. When a receive OOF event occurs, IXF3204 framer declares a maskable OOF interrupt to the host processor.

Table 28. T1 Out-Of-Frame Criteria Options

Format	Ratio	Fe	Ft	Fs	Ft and Fs
ESF	2/4 2/5 2/6 3/5	X X X X	-	-	-
D4 SF	2/4 2/5 2/6	-	X X X	X X X	X X X
SLC®96	2/4 2/5	-	X X	X X	X X

NOTES:
1. This table includes possible configurations for the IXF3204 framer.
2. 2/n refers to any two framing bits in error in a sliding window of n framing bits (including 2 consecutive frame bit errors). An Ft bit window, an Fs bit window, and a combined Ft and Fs window can all be monitored simultaneously by user selection.
3. In SLC®96 mode, once DDL alignment is determined, only Fs bits that do not carry DDL information are used in OOF detection. DDL bits can be considered unerrored Fs bits.

6.9.3 T1 Resynchronization

The IXF3204 framer can be configured to resynchronize either manually upon detection of an OOF condition or automatically (the default). If the IXF3204 framer is enabled for automatic detection and an OOF condition is present, the IXF3204 framer automatically searches for frame sync.

6.9.4 T1 Change Of Frame Alignment

The IXF3204 framer reports a Change of Frame Alignment (COFA) condition when the last receiver resynchronization results in a change of frame alignment. COFAs indicate that a new bit position has been selected as the valid framing bit location. In contrast, OOFs indicate that only some percentage of the framing bits are in error. COFAs are always associated with an OOF.

Note: The IXF3204 framer provides a COFA indication bit in the port status register.

6.10 T1 Frame and Cyclic Redundancy Check Error Insertion

The IXF3204 framer supports the controlled insertion of various classes of errors for testing. Insertion of errors is controlled by setting the appropriate bits.

6.10.1 T1 Frame Bit Error Insertion

The IXF3204 framer transmit framer can be programmed to insert either single frame-bit errors or F-bit errors at several rates up to one in a million. The errors can be inserted in Ft, Fs, or Fe bits by inverting the value generated by the framer.

6.10.2 T1 CRC Error Insertion

When the IXF3204 framer sources Cyclic Redundancy Check (CRC) bits, an additional feature allows the IXF3204 framer to command deliberate inversion (and thereby corruption) of outgoing CRC code words.

The IXF3204 framer can insert CRC errors at a rate of either one per multiframe (continuous) or at a rate of up to one every 10^{-6} frames. CRC error insertion is available only in ESF mode and affects only the framing bits that carry the CRC.

6.11 T1 Alarm Overview

The next sections provide details for detecting and transmitting the following alarms:

- Section 6.12, “T1 Red Alarm”
- Section 6.13, “T1 Yellow Alarm”
- Section 6.14, “T1 Blue Alarm”

6.12 T1 Red Alarm

The T1 red alarm indicates loss of receive-side framing per ANSI T1.231. The Loss Of Frame (also known as ‘OOF’) condition is integrated for N time (with N from 125 microseconds to 8.19 seconds) before the Red alarm status bit (RED) goes active and a maskable interrupt is generated. Intermittent OOF conditions are integrated so that if the density of OOF conditions is equal to or above the set value, the alarm is declared.

The Red alarm flag is cleared if no OOF occurs for M time after re-acquisition of frame synchronization (with M any number up to 8.19 seconds). The clear condition is also integrated so that if the OOF state is not present for a density above the clear value, the alarm is removed. The default values are 2.5 seconds to set and 8.19 seconds to clear.

The Loss Of Frame (OOF) condition, as well as the failure (red alarm), are reported in separate bits with change indicator and real time status.

Note: For T1, there is no transmitted red alarm.

6.13 T1 Yellow Alarm

The T1 yellow alarm signal (also known as a Remote Alarm Indication or 'RAI') indicates a receive-side fault on the far-end and is therefore an indication of local-side transmit path performance. Detection of either a blue alarm or a red alarm can generate the transmission of a yellow alarm.

6.13.1 T1 Yellow Alarm Detection

Detection of a T1 yellow alarm is dependent upon the framing mode.

- T1 SF and SLC®96 Yellow Alarm Detection

  In the T1 SF and SLC®96 framing modes, yellow alarm detection is based on bit 2 being equal to '0' in all TS of a frame, per ANSI T1.403. When this condition is detected, the Receive Yellow Alarm flag bit is set, and a maskable interrupt is generated. Further integration of the yellow alarm can be done using the programmable thresholds available for the integrated version of this alarm.

- T1 ESF Yellow Alarm Detection

  In the T1 ESF mode, an additional yellow alarm is detectable based upon the FDL, per ANSI T1.403. In this mode, the yellow alarm is declared if an FDL pattern (1111 1111 0000 0000) occurs in 16 contiguous 16-bit pattern intervals on the ESF datalink. The yellow alarm is cleared if the pattern does not match the alarm pattern in two contiguous patterns.

6.13.2 T1 Yellow Alarm Transmission

A T1 yellow alarm transmission is initiated when a configuration bit is set or as a result of a consequent action. (For details, see Section 11.3, "Alarm Handling and Consequent Actions".) The alarm can be sent automatically if the IXF3204 framer receiver automatic consequent action feature is enabled and the IXF3204 framer receives a triggering event. The triggering event is controlled by the automatic alarm control register. The alarm is sent as long as the receive event is present. Depending on the framing mode selected, the IXF3204 framer performs yellow alarm transmission differently.

- T1 SF and SLC®96 Yellow Alarm Transmission

  In T1 SF framing modes (SF and SLC®96), yellow alarm transmission is accomplished by forcing the second most-significant bit of all the PCM channels to a '0', per ANSI T1.403. If the ZCS coding option is enabled, the force function occurs before ZCS processing

- T1 ESF Yellow Alarm Transmission

  In T1 ESF, the Yellow Alarm can be transmitted in the FDL, which complies with ANSI T1.403. In this mode, the FDL yellow alarm pattern (1111 1111 0000 0000) is transmitted on the FDL. When the yellow alarm transmit bit is cleared, the IXF3204 framer sends the idle code and waits for the next message from the selected FDL data source.

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6.14 T1 Blue Alarm

The T1 blue alarm signal (also known at the Alarm Indication Signal or 'AIS') indicates that the remote terminal is either off-line, or undergoing maintenance, or both. Also known as the 'Keep-Alive' signal, it is generated to allow proper clock recovery on lines undergoing maintenance, therefore preventing excess jitter transmission, and so on. (For more information on the T1 blue alarm, see Section 6.2.1, "T1 Alarm Indication Signal".)

6.14.1 T1 Blue Alarm Detection

In the T1 framing mode, an Alarm Indication Signal (AIS) is declared when less than 5 zeroes exist in a 3-ms window of received data, per ANSI T1.231. The indicator associated with the RAIS reports the AIS and causes a maskable processor interrupt. This indicator is cleared if the received signal has 6 or more zeroes in a 3-ms window. The blue alarm is reliably detected in the presence of a 1×10^{-3} BER. The AIS condition, as well as the failure (blue alarm), are reported in separate bits with change indicator and real-time status.

6.14.2 T1 Blue Alarm Transmission

By setting the appropriate bits, an AIS can be sent as an unframed all-ones from TPOS and TNEG, per ANSI T1.231.

AIS also can be sent automatically if both of the following occur: the IXF3204 framer receiver automatic alarm response feature is enabled and the IXF3204 framer receives a triggering event (controlled by the automatic alarm control register). The alarm is sent as long as the receive event is present.

AIS can be generated as part of a consequent action if both of the following occur: (1) there is a triggering event and (2) the consequent action is enabled.

6.15 Fractional T1

In Fractional T1 mode, the system side can be programmed to source gapped clock outputs for both the receive and transmit directions. Gapping is possible at a DS0 level and is programmable. Fractional T1 is enabled by programming the appropriate receive and transmit gap selections.

As an option, the F bit can be gapped when in gap clock mode. The clock must be output from the IXF3204 framer in both the Rx and Tx backplane directions.

Note:

- Gapping must be used in 1x streams only.
- Gapped clocks are generated only when the IXF3204 framer is the clock source. When the IXF3204 framer is a clock sink, it requires a continuous, non-gapped clock for correct operation. In this case, clock gapping for fractional T1 must be handled externally.

7.0 J1 Framers

This chapter discusses the following J1 framer topics:

- Section 7.1, “J1 Frame Operations”
- Section 7.2, “J1 Alarm Overview”
- Section 7.3, “J1 Yellow Alarm”

7.1 J1 Frame Operations

Operation of J1 frames (per TTC JT-G703, JT-G704, JT-G706, and JT-I431) is very similar to that of T1 frames. This chapter describes only the differences between J1 and T1. The rest of the functions, such as line coding, AIS, OOF, and so on are the same for J1 as for T1. (For details of J1 operations that are the same as T1 operations, see Chapter 6.0, “T1 Framers”.)

Table 29 lists and cross references the primary differences between J1 and T1 frame operations.

Table 29. Primary Differences between J1 and T1 Frame Operations

J1 and T1 Frame Operation Differences	Cross Reference to Section Discussing the Difference
12-frame multiframe structure (SF)	Section 7.1.1, “J1 Frame Operation - Modified 12-Frame Multiframe”
24-frame multiframe structure (ESF)	Section 7.1.2, “J1 Frame Operation - Modified 24-Frame Multiframe”
CRC-6 procedure, 24-frame multiframe	Section 7.1.2, “J1 Frame Operation - Modified 24-Frame Multiframe”
Yellow alarm definition	Section 7.3, “J1 Yellow Alarm”

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7.1.1 J1 Frame Operation - Modified 12-Frame Multiframe

Table 30 lists the modified J1 12-frame multiframe structure, which operates at 1.544 Mbps. In contrasting the format of the J1 12-multiframe and the T1 SF, the major difference is the (re)definition of the F bit in frame 12 of the multiframe structure. With J1, this bit is defined to be a far-end receive failure alarm (also known as 'Japanese Yellow Alarm').

Use of Japanese Yellow Alarm, in which an Fs bit is lost to RAI use, requires a modified framing algorithm (from the T1 SF framing algorithm) to manage the modified framing structure. This alarm is valid only when J1 12-Frame multiframe mode is selected. The Japanese Yellow Alarm is described in Section 7.3, "J1 Yellow Alarm".

To select the J1 12-frame multiframe (1) use the application programming interface manual for the IXF3204 framer to enable J1 operation and select J1-12 frame multiframe and (2) use Table 30 to select the J1 yellow alarm bit.

Table 30. J1 12-Frame Multiframe Structure

Frame	F Bits			Time Slot Bit Usage			
	Bit	Terminal Framing Bit Ft	Signaling Framing Bit Fs	Pulse-Code Modulation Format	Signaling (If Used)	Signaling Bit Definition	
						2-State	4-State
1	1	1	-	1-8	-	-	-
2	194	-	0	1-8	-	-	-
3	387	0	-	1-8	-	-	-
4	580	-	0	1-8	-	-	-
5	773	1	-	1-8	-	-	-
6	966	-	1	1-7	8	A	A
7	1159	0	-	1-8	-	-	-
8	1352	-	1	1-8	-	-	-
9	1545	1	-	1-8	-	-	-
10	1738	-	1	1-8	-	-	-
11	1931	0	-	1-8	-	-	-
12	2124	-	Japanese Yellow Alarm	1-7	8	A	B

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7.1.2 J1 Frame Operation - Modified 24-Frame Multiframe

Table 31 lists the modified J1 24-frame multiframe structure, which also operates at 1.544 Mbps. In contrasting the format of the J1 24-multiframe and the T1 ESF, the major difference is the (re)definition of the CRC-6 calculation procedures.

- With J1 ESF, the CRC-6 calculation is based upon the values of all 4,632 bits in the J1 24-multiframe structure, including the actual Fe bit values.
- With T1 ESF, the CRC-6 calculation is based on the assumption that all Fe bits have a value of '1' for calculation purposes. For details, see Section 6.7.2, "T1 ESF CRC-6 Procedures".

To select the J1 24-frame multiframe (1) use the application programming interface manual for the IXF3204 framer to enable J1 operation and to select J1-24 frame multiframe and (2) use Table 31 to select the J1 yellow alarm bit.

Table 31. J1 24-Frame Multiframe Structure

Frame Number	F-Bits				Time Slot Bit Usage		Signaling Bit Definition		
	Bit Number	Framing Bit Fe	Facility Data Link	CRC-6	Pulse-Code Modulation Format	Signaling (If used)	2-State	4-State	16-State
1	1	-	m	-	1-8	-	-	-	-
2	194	-	-	e1	1-8	-	-	-	-
3	387	-	m	-	1-8	-	-	-	-
4	580	0	-	-	1-8	-	-	-	-
5	773	-	m	-	1-8	-	-	-	-
6	966	-	-	e2	1-7	8	A	A	A
7	1159	-	m	-	1-8	-	-	-	-
8	1352	0	-	-	1-8	-	-	-	-
9	1545	-	m	-	1-8	-	-	-	-
10	1738	-	-	e3	1-8	-	-	-	-
11	1931	-	m	-	1-8	-	-	-	-
12	2124	1	-	-	1-7	8	A	B	B
13	2317	-	m	-	1-8	-	-	-	-
14	2510	-	-	e4	1-8	-	-	-	-
15	2703	-	m	-	1-8	-	-	-	-
16	2896	0	-	-	1-8	-	-	-	-
17	3089	-	m	-	1-8	-	-	-	-
18	3282	-	-	e5	1-7	8	A	A	C
19	3475	-	m	-	1-8	-	-	-	-
20	3668	1	-	-	1-8	-	-	-	-
21	3861	-	m	-	1-8	-	-	-	-
22	4054	-	-	e6	1-8	-	-	-	-
23	4247	-	m	-	1-8	-	-	-	-
24	4440	1	-	-	1-7	8	A	B	D

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7.2 J1 Alarm Overview

The next sections provide details for detecting and transmitting the following alarms:

- Red. The J1 red alarm is the same as the T1 red alarm. (See Section 6.12, “T1 Red Alarm”.)
- Blue. The J1 blue alarm is the same as the T1 blue alarm. (See Section 6.14, “T1 Blue Alarm”.)
- Yellow. The following text describes J1 yellow alarm detection and transmission.

7.3 J1 Yellow Alarm

The J1 yellow alarm is also known as Remote Alarm Indication (RAI). It indicates a receive-side fault on the far-end and is therefore an indication of local-side transmit path performance. Detection of either a blue alarm or a red alarm can generate the transmission of a yellow alarm.

7.3.1 J1 Yellow Alarm Detection

J1 yellow alarm detection is dependent upon framing mode, as described in the following sections.

- J1 SF Yellow Alarm Detection

  In J1 SF (12-frame multiframe) structure, an alternate yellow alarm (the ‘Japanese yellow alarm’) is defined per TTC JT-G704. A Japanese yellow alarm is detected if the Fs bit in frame 12 of the superframe is equal to ‘1’ for two consecutive superframes, and it clears when F bit 12 is not equal to ‘1’ for 2 consecutive superframes.

- J1 ESF FDL Yellow Alarm Detection

  In J1 24-frame multiframe structure, the yellow alarm is detected when 16 consecutive ones are detected in the DL bit, per TTC JT-G704.

7.3.2 J1 Yellow Alarm Transmission

A J1 yellow alarm transmission is initiated when the configuration bit is set or as a result of a consequent action. (For details, see Section 11.3, “Alarm Handling and Consequent Actions”.) The alarm can be sent automatically if the IXF3204 framer receiver automatic consequent action feature is enabled and the IXF3204 framer receives a triggering event. The triggering event is controlled by the automatic alarm control register. The alarm is sent as long as the receive event is present. Depending on the selected framing mode, the yellow alarm transmission is performed differently.

- J1 SF Yellow Alarm Transmission

  In J1 12-frame multiframe (SF) mode an alternate yellow alarm transmission (the Japanese yellow alarm) is enabled, which inverts the frame 12 bit to ‘1’, per TTC JT-G704.

- J1 ESF FDL Yellow Alarm Transmission

  In J1 24-frame multiframe mode, the FDL yellow alarm is detected when there are 16 consecutive ones in the data link bits, per TTC JT-G704.

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8.0 E1 Framers

This chapter discusses the following E1 Framer topics:

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8.1 E1 Line Coding

The IXF3204 framer provides E1 line coding and decoding functions to support non-coding line interfaces and to facilitate performance monitoring.

The following sections detail the supported E1 coding formats.

- Section 8.1.1, "E1 Alternate Mark Inversion"
- Section 8.1.2, "E1 High-Density Bipolar Three"

8.1.1 E1 Alternate Mark Inversion

As with T1 line coding, Alternative Mark Inversion (AMI) is a Return-to-Zero (RZ) format, per ITU G.701. In this format:

- A binary 'one' (a 'mark') is represented by either a positive- or negative-going pulse.
- A binary 'zero' (a 'space') is represented by the absence of a pulse.

As with T1 line coding, each consecutive pulse alternates in polarity (for example, a positive pulse must always be followed by a negative pulse and a negative pulse must always be followed by a positive pulse) regardless of the number of intervening spaces between the two pulses.

For E1 line coding, as described in Section 8.1.2, "E1 High-Density Bipolar Three", HDB3 line coding method is used to prevent excess zeroes from occurring.

8.1.2 E1 High-Density Bipolar Three

In High-Density Bipolar Three (HDB3) coding, four consecutive zeroes in the E1 data stream are replaced by the HDB3 substitution pattern of either '000V' or 'B00V', in which 'V' is an intentional bipolar violation (BPV) and 'B' is a valid bipolar mark. This substitution pattern, per ITU G.703, limits the maximum number of consecutive spaces to three.

The choice of substitution pattern is made so that the number of B pulses between consecutive V pulses is odd (that is, successive V pulses are of alternate polarity). This substitution is made regardless of where the four consecutive zeroes occur in the datastream, including framing, signaling, and alarm bits.

The IXF3204 framer performs both HDB3 coding on the E1 transmitted signal and HDB3 decoding on the E1 received signal. The user must select the proper registers, defined in the memory map document for the IXF3204 framer.

Note:

- Select HDB3 encoding/decoding by programming appropriate bits in the associated register.
- Received BPVs that are part of the HDB3 pattern are not counted as BPVs in the coding violation error counter.

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8.2 E1 Line Monitoring

Before framing activity occurs, the E1 line signal is monitored for the following alarms and impediments:

- Section 8.2.1, “E1 Alarm Indication Signal”
- Section 8.2.2, “E1 Auxiliary Pattern”
- Section 8.2.3, “E1 Coding Violations”
- Section 8.2.4, “E1 Loss of Signal”

8.2.1 E1 Alarm Indication Signal

An E1 Alarm Indication Signal (‘AIS’), per ITU G.775 is declared when less than three spaces (that is, two or less zeroes) are detected in a 250-microsecond period of data in a 512-bit window on each of two consecutive periods. This condition must be detected in the presence of a 1.0E-03 Bit Error Rate (BER) so that a framed all-ones pattern is not mistaken as an AIS.

Alternatively, the AIS indicator can be coupled with the Loss of Frame Detector, per ETS 300 233. In this case, detection of both AIS and LOF is used to set the received AIS indicator bit. After AIS is detected, the port status flag is set, and a maskable processor interrupt is generated. The AIS is cleared when the set conditions are not met. The IXF3204 framer can also send the AIS signal toward the line side when programmed by the user or as a consequent action. (For details, see Section 11.3, “Alarm Handling and Consequent Actions”.)

8.2.2 E1 Auxiliary Pattern

ETS 300 233 defines an alternative signal to AIS for E1 lines, per ETSI 300 233. This signal, the Auxiliary Pattern (AUXP) is an unframed continuous pattern of marks and spaces (101010...).

AUXP is declared when a continuous alternating mark/space pattern is detected over a 512-bit period (that is, over 250 microseconds, or two frames) in the presence of a 10^{-3} Bit Error Rate (BER) so that a framed 1:1 pattern is not mistaken as an AUXP. Once AUXP is detected, the alarm status flag is set, and a maskable processor interrupt is generated. The AUXP is cleared when the pattern is not detected in any subsequent 512-bit period after the detection of AUXP.

When the user programs the IXF3204 framer to send AUXP, an unframed 1:1 pattern is transmitted on the line. AIS and AUXP transmission should not be set at the same time. However, if they are, AIS takes precedence.

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8.2.3 E1 Coding Violations

For E1, two basic types of line coding violations are defined:

- A Bipolar Violation ('BPV') coding violation, per ITU G.703 is defined as two consecutive pulses (marks) of the same polarity.
- A High-Density Bipolar 3 ('HDB3') coding violation, per ITU O.161 is defined as the occurrence of two consecutive BPVs of the same polarity.

The IXF3204 framer actively monitors the line signal for coding violations and provides a status register count of detected violations for performance monitoring purposes. The information can be read from the LIV and LICV registers.

8.2.4 E1 Loss of Signal

An E1 Loss of Signal ('LOS') is defined as any period of 175+/- 75 clock cycles in which no pulse transitions occurred. The IXF3204 framer continually monitors the line signal for LOS occurrences. The LOS indication is set when no pulse transitions are detected for a period that exceeds the programmed threshold limit. The LOS indication is cleared if there are N transitions detected in a window of duration M. Receive signal losses set a maskable interrupt flag.

8.3 E1 Insertion of Line Errors

For E1 testing, the IXF3204 framer supports controlled insertion of the following line error types.

- Framing errors (not discussed here)
- CRC errors, at rates from continuous to one in a million (Section 8.6.7, "E1 CRC-4 Error Insertion")
- Bipolar Violation (BPV) errors (discussed in the following text)

For HDB3 or AMI modes, the IXF3204 framer transmitter can be programmed to insert BPV errors. The IXF3204 framer error insertion register allows insertion of either single BPVs or insertions at a rate of from 100% (that is, insert continuous BPVs) up to 10^{-6} (that is, insert one BPV every million of marks).

For E1, BPV insertions are subject to the following conditions:

- HDB3 zero-suppression coding is not violated.
- During Line Loopback, BPV insertion is not performed even if it is enabled.
- If the IXF3204 framer detects a DS1 in-band Network Loop back code, the IXF3204 framer enters a line loopback. As a result, any BPV insertions that are enabled are then disabled.
- If the IXF3204 framer has a full or partial (DS0s) payload loopback code and if BPV insertion is not desired during this loopback BPV, then insertion must be manually disabled.

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8.4 E1 Framing

Table 32 lists the structure of a basic E1 frame, per ITU G.704, G.706, and G.732. The E1 basic frame format can be combined into the multiframe formats as described in the following sections: Section 8.5, "E1 FAS/NFAS Framing" to Section 8.8, "E1 Channel-Associated Signaling Multiframe".

Table 32. E1 Basic Frame Structure

Parameter	Value
Bit rate	2.048 Mbps
Frame length	256 bits, consisting of: • 8 overhead framing bits per frame • 248 payload bits
Frame period	125 microseconds
Frame rate	8 kHz
Payload (or 'Channelization')	30 channels (also known as 'time slots') with 8 bits/channel
Channel rate	64 Kbps

8.5 E1 FAS/NFAS Framing

Basic G.704 FAS/NFAS framing is selected by enabling E1 framing mode and disabling CAS and CRC-4 multiframing, per ITU G.704, G.706.

8.5.1 E1 FAS/NFAS Framing Description

Two distinct basic frame types are defined, one with the Frame Alignment Signal (FAS) word in Time Slot 0 (TS0) and one with the Not FAS (NFAS) word in TS0. These two different frame types are alternately transmitted and are used to determine frame synchronization and provide bandwidth for maintenance and overhead functions.

Table 33 lists the definitions for the TS0 bits.

Table 33. E1 Time Slot 0 Bit Allocation

FAS/ NFAS	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
FAS	International Bit (Si)[1]	0	0	1	1	0	1	1
NFAS	International Bit (Si)	1	Remote Alarm Indication (A)[2]	Spare Bit (Sa4)[3]	Spare Bit (Sa5)	Spare Bit (Sa6)	Spare Bit (Sa7)	Spare Bit (Sa8)

NOTES:
1. Reserved for international use. Usage is defined in ITU G.704.
2. 0 = No Alarm. 1 = Alarm Condition.
3. Spare Bits Sa4 to Sa8. Usage is defined in ITU G.704. Possible uses include point-to-point applications (Sa4-Sa8), message-based data link (Sa4), national bit usage, or synchronization status messages. User must set these bits to '1' on links that cross an international border.

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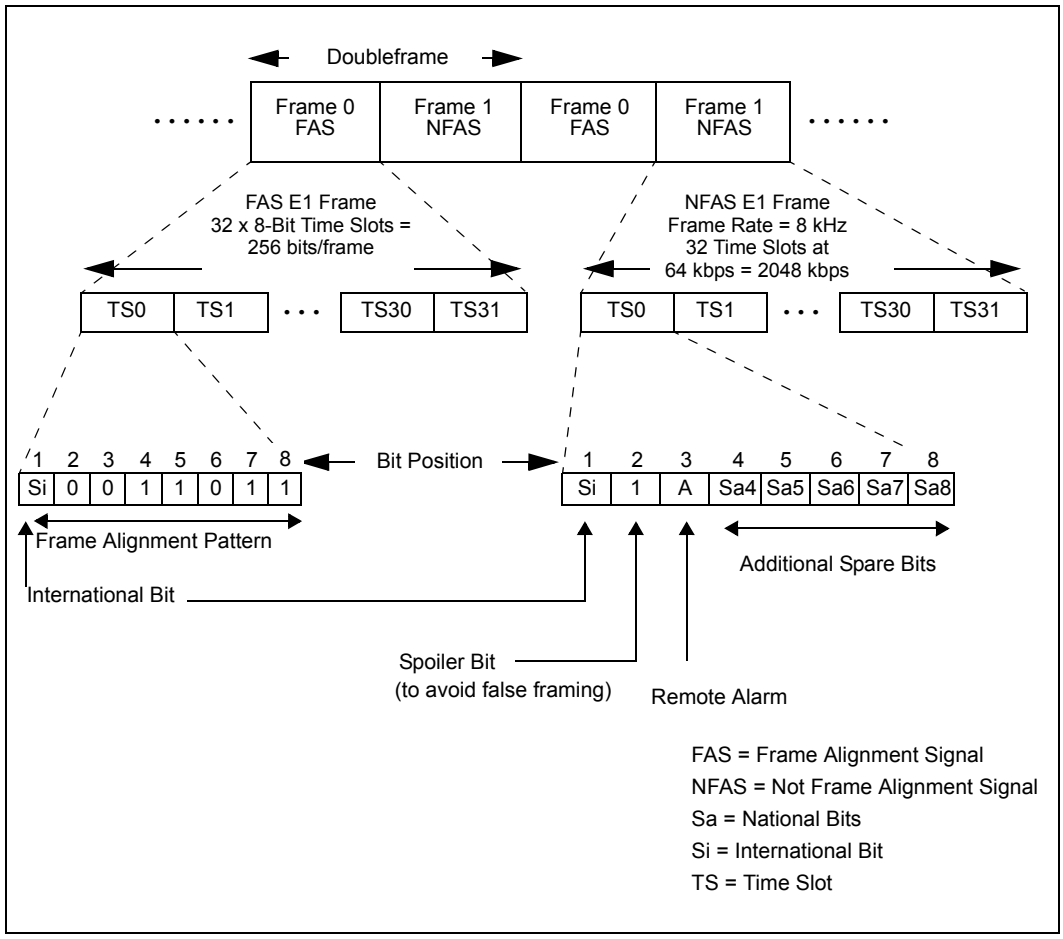
Figure 10 shows the entire FAS/NFAS ‘doubleframe’ structure.

Figure 10. FAS/NFAS Doubleframe



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8.5.2 E1 FAS/NFAS Framing Operation

To achieve synchronization, the following detection sequence is required:

- Reception of a FAS word (0011011 binary) with no errors.
- Reception of a NFAS word with bit 2 = '1' precisely one frame period later.
- Reception of a FAS word with no errors precisely one frame period later.

The OOF flag bit is set when frame sync is lost and cleared when frame alignment is established. It generates a maskable interrupt for the host processor. If frame sync is lost and then regained at a different position (as marked by the off-line framer circuit), the Change Of Frame Alignment (COFA) bit is set.

In the receive direction:

In a FAS frame, the Si bit is extracted and stored in a byte register. The byte is updated on multiframe boundaries.

In an NFAS frame, the Si bit and the Sa4 to Sa8 bits are also extracted and stored on multiframe boundaries in byte registers, and all the bytes in the registers are accessible to the host processor. When the framer is not in CRC-4 mode, the byte is updated every 16 frames without any specific alignment to a frame number, FAS and eight NFAS. The Sa bits are also accessible to the data link module. For configuration details and a description of Sa-bit handling, see Section 8.18, "E1 Sa/Si Bit Access and Handling". For TS0 bit usage, see Figure 10.

In the transmit direction:

The FAS/NFAS frame time slot 0 information can be either or both of the following:

- Generated internally, assembled from the provided Sa, Si, and RAI bits in the appropriate registers.
- Sourced transparently from the system backplane to the line.

The Si bits in both the FAS (Sif) and NFAS (Sinf) frames may be passed through transparently from the system backplane. This configuration results in the IXF3204 framer sourcing the FAS and NFAS words from the respective internal sources with the exception of the Si bits, which are now furnished by the external source. Similarly, the Sa bits in the NFAS frame may be passed through transparently from the serial interface.

8.5.3 E1 FAS/NFAS Error Generation

The IXF3204 framer allows insertion of single FAS or NFAS bit errors or bit error insertions at several rates from continuous to one in a million frames.

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8.6 E1 CRC-4 Multiframe

This mode is selected when CRC-4 mode is set in the configuration registers in Rx or Tx mode, per ITU G.704.

8.6.1 E1 CRC-4 Multiframe Description

Four-bit Cyclic Redundancy Check (CRC-4) Multiframing is used for immunity against false framing and also provides non-intrusive error monitoring capabilities for the E1 payload data. The implementation consists of redefinition of Bit 1 of the FAS/NFAS frames and definition of a larger multiframe structure.

The CRC-4 Multiframe has 16 alternating FAS/NFAS frames, consecutively numbered from 0 to 15. The CRC-4 Multiframe is in turn divided into two 8-frame 'sub-multiframes': SMF I and SMF II. When CRC-4 multiframing is enabled, a CRC is calculated for each 'sub-multiframe' and is reported in the next multiframe.

- In FAS frames, bit 1 is used to send the four CRC-4 bits, designated C1 - C4, in each SMF.
- In NFAS frames, bit 1 is used to send the four-bit CRC-4 multiframe alignment pattern (001011) and two CRC-4 error indication bits (E).

Table 34 lists the CRC-4 Multiframe structure.

Table 34. CRC-4 Multiframe Structure

SMF	Frame Number	Time Slot 0 Bit Number							
		1	2	3	4	5	6	7	8
I	0	C1	0	0	1	1	0	1	1
	1	0	1	A	Sa4	Sa5	$Sa6_1$	Sa7	Sa8
	2	C2	0	0	1	1	0	1	1
	3	0	1	A	Sa4	Sa5	$Sa6_2$	Sa7	Sa8
	4	C3	0	0	1	1	0	1	1
	5	1	1	A	Sa4	Sa5	$Sa6_3$	Sa7	Sa8
	6	C4	0	0	1	1	0	1	1
	7	0	1	A	Sa4	Sa5	$Sa6_4$	Sa7	Sa8
II	8	C1	0	0	1	1	0	1	1
	9	1	1	A	Sa4	Sa5	$Sa6_1$	Sa7	Sa8
	10	C2	0	0	1	1	0	1	1
	11	1	1	A	Sa4	Sa5	$Sa6_2$	Sa7	Sa8
	12	C3	0	0	1	1	0	1	1
	13	E1	1	A	Sa4	Sa5	$Sa6_3$	Sa7	Sa8
	14	C4	0	0	1	1	0	1	1
	15	E2	1	A	Sa4	Sa5	$Sa6_4$	Sa7	Sa8

NOTE:
1. A: Remote Alarm Indication; C1 - C4: CRC-4 Bits; En: Remote End CRC-4 Block Error Indicator Bits; Sa4 - Sa8: Additional Spare Bits; $Sa6_N$: Sa6 Bit Numbering per ETS 300 233 Codeword Definition.

8.6.2 E1 CRC-4 Multiframe Operation

When CRC-4 is selected as the receive framing option and after FAS/NFAS frame sync is present, the receiver attempts to synchronize to the 16-frame CRC multiframe, per ITU G.706. CRC-4 multiframe alignment is attained when at least two correct CRC-4 Multiframe Alignment Signals (‘MFAS’) 001011 binary are detected within 8 milliseconds and the time between each correct MFAS is either 2 milliseconds or multiples of 2 milliseconds.

The pulse generated every 16 frames at the appropriate backplane multi-frame pulse ball corresponds to the CRC-4 multiframe boundary or to the CAS multiframe boundary, depending on the selection by the user. As a check for spurious frame synchronization, if CRC-4 alignment is not achieved within 8 milliseconds after FAS/NFAS sync, a new search is initiated for valid FAS/ NFAS frame alignment.

8.6.3 E1 CRC-4 Multiframe Interworking

If ITU G.706 Annex B CRC Interworking functionality is enabled (which allows the interworking of CRC-4 with non-CRC-4 equipment), the following procedure is used if CRC-4 multiframe alignment is not achieved within 100 to 500 milliseconds:

1. Set the ‘Loss of CRC Multiframe Alignment’ indicator.
2. Inhibit receive CRC processing.
3. Continue to transmit CRC-4 data with both of the ‘E’ Bits (that is, the REBE bits) set to ‘0’.

The IXF3204 framer firmware manages the interworking function after the user enables this function. (For register and implementation details, see the memory map document for the IXF3204 framer.)

8.6.4 E1 CRC-4 Multiframe Error Checking

After CRC-4 multiframe alignment is achieved, CRC-4 error checking can start and frame-alignment monitoring continues. If there is:

- No mismatch between the calculated remainder and the received CRC-4 bits, no CRC error is registered for the checked SMF.
- A mismatch between the calculated remainder and the received CRC-4 bits, then a CRC-4 error has occurred, the event is flagged, and a maskable interrupt is driven and recorded in the receiver CRC-4 error counter. The error counter register available to the host processor is updated every second.

8.6.5 E1 Loss of CRC-4 Multiframe Alignment

If basic frame alignment is lost, then the CRC multiframe is lost. As a user-enabled option, CRC-4 Multiframe alignment is lost if two consecutive CRC MF alignment signals are received with errors. Loss of CRC multiframe is indicated and causes the generation of a maskable interrupt per ITU G.706 as well as both ETSI 300 01 and 300 233. (The default state is ‘disabled’.)

If a minimum of 915 errored CRC blocks are detected out of a window of 1000, a false frame alignment is indicated (loss of frame) and a new search for frame alignment is started at a point just after the location of the assumed spurious frame alignment signal.

8.6.6 E1 CRC-4 Multiframe Transmission

The CRC multiframe signal is generated by the Tx framer when that mode is enabled. The CRC-4 bits can be sent from the ones calculated in the Tx framer or from the bits received from the backplane side.

In general, the time slot 0 information related to CRC, Sa/Si, RAI, and REBE bits can be:

- Generated from any of the following:
  - The calculated CRC
  - The provided Sa, Si registers
  - The provided RAI and REBE bits from the appropriate register
  - The consequent actions module, if it is enabled. (For details, see Section 11.3, “Alarm Handling and Consequent Actions”.)
- Sourced transparently from the system backplane to the line.
- A combination of the two above

Multiframe boundary alignment can come from an external source or from a free-running internal multiframe counter.

8.6.7 E1 CRC-4 Error Insertion

The CRC-4 encoder may be set to insert single or continuous CRC-4 errors by inverting the C1-C4 bits. The Error Injection register allows insertion of either a single CRC error or error insertion at a rate from one to one in a million.

8.7 E1 Remote End Block Error Operation

Detection:

The Remote End Block Error bits (also known as ‘REBE’ or ‘E’ bits) are indications from the downstream data source that it detected a CRC-4 error in an SMF sent to it by the near end. Normally, the E bits are set to ‘1’, but when there is a remote-end SMF block error (and the remote end is equipped for REBE operation), the error REBE is reported by clearing to ‘0’ the E bit sent back to the near end. Upon receipt of an E bit = ‘0’, the event is recorded in the receive 12-bit REBE counter.

Transmission:

If the automatic REBE response feature is:

- Not enabled, the transmit REBE bits (bit 1 of frames 13 and 15) are set to ‘1’.
- Enabled and a CRC-4 error is detected in the receive:
  - SMF I, then the transmit E bit in frame 13 of the next multiframe is set to ‘0’.
  - SMF II, then the transmit E bit in frame 15 of the next multiframe is set to ‘0’.

Note: The REBE value can be forced by the user or programmed to follow some consequent actions. (For details, see Section 11.3, “Alarm Handling and Consequent Actions”.)

8.8 E1 Channel-Associated Signaling Multiframe

This section discusses the E1 Channel-Associated Signaling (CAS) multiframe.

8.8.1 E1 CAS Multiframe Description

E1 CAS Multiframing, per ITU G.704, uses time slot 16 both to define signaling multiframe boundaries and to contain individual channel signaling bits. Time slot 0 usage is identical to FAS/NFAS Doubleframe usage. The CAS multiframe can be aligned to either the FAS or NFAS frames.

The CAS multiframe is made up of 16 consecutive basic E1 frames (eight doubleframes) numbered from 0 to 15. Time slot 16 of frame 0 has a multiframe alignment signal ('MFAS') 0000 binary in the first 4-bit positions of the time slot. The remaining 4 bits have spare bits and an alarm indication. Time slot 16 in the remaining frames (1 to 15) has signaling information for TS 1 to 15 and TS 17 to 31.

Table 35 lists how sixteen state words are imbedded in TS16. No signaling is associated with TS0 or TS16, as these time slots are overhead time slots and not payload channels. (This table is repeated as a convenience to the reader in Section 10.2.3, "E1 Channel-Associated Signaling: Time Slot 16".)

Table 35. Time Slot 16 CAS Multiframe Structure

Frame Number	Time Slot 16	
	Bits 1 - 4	Bits 5-8
0	0000 MFAS[1]	XYXX[2]
1	ABCD TS1 Signaling ITU Channel 1	ABCD TS17 Signaling ITU Channel 16
2	ABCD TS2 Signaling ITU Channel 2	ABCD TS18 Signaling ITU Channel 17
n	ABCD TSn Signaling ITU Channel n	ABCD TS (n + 16) Signaling ITU Channel (n + 15)
14	ABCD TS14 Signaling ITU Channel 14	ABCD TS30 Signaling ITU Channel 29
15	ABCD TS15 Signaling ITU Channel 15	ABCD TS31 Signaling ITU Channel 30

NOTES:
1. MultiFrame Alignment Signal.
2. X: Spare Bits; Y: Remote Alarm Indication; 0: No Alarm; 1: Alarm.

8.8.2 E1 CAS Multiframe Operation

The search for the TS16 CAS structure is started when the option is enabled and after basic frame alignment is obtained. CAS alignment is declared when the '0000' pattern is found following a non-zero time slot. The receiver can detect if the CAS multiframe is aligned to the FAS or NFAS frame. The state of the 'Y' bit is used to check for the TS16RAI signal.

8.8.3 E1 Loss of CAS Multiframe

Loss of CAS multiframe is indicated by a maskable indicator. Multiframe alignment loss is reported if two consecutive CAS Multiframe Alignment Signals (MFAS) are received with errors.

As an option, multiframe alignment loss is reported if all the bits in TS16 are zeroes for the period of an entire multiframe. The all-zeroes option disallows the reception of all zeroes used in the signaling-bit positions. If alignment is lost due to the all-zeroes condition, realignment takes place after a valid CAS MultiFrame (MF) is received in TS-16 following a frame in which the TS16 has at least one non-zero bit.

8.8.4 E1 CAS Multiframe Transmission

CAS multiframe boundary alignment can come from either an external source or from an internal multiframe counter. An external sync signal aligns data on the TX serial interface for insertion into frame 0 of the 16-frame CAS TX multiframe.

The normal multiframe alignment signal consists of all zeroes in the first 4 bits of TS16 in frame 0 of the CAS multiframe. More than two consecutive erroneous MFAS signals cause the far end to lose CAS-MF sync.

As listed in Table 35, the X bits are spare bits that accompany the MFAS and the TS 16 remote alarm (Y bit) in TS16 of frame 0. The X bits occupy positions 5, 7, and 8 in TS16. If the IXF3204 framer supplies TS16, the X bits can be individually set in the transmit signaling register. The default value for each of the X bits is binary 1.

8.8.5 E1 CAS Multiframe Alignment to FAS/NFAS

Frame 0 of the transmitted CAS Multiframe [containing the MultiFrame Alignment Signal (MFAS) in time slot 16] can be aligned to either a FAS or NFAS basic E1 frame.

8.9 E1 Simultaneous CAS and CRC Multiframes

In this mode, both CAS and CRC multiframes are present simultaneously, per ITU G.704. The CAS multiframes are not necessarily synchronized to the CRC-4 multiframes. This mode is enabled by simultaneously enabling CAS and CRC multiframing.

This mode of operation allows the concurrent use of both CAS and CRC-4 multiframing. The alignment of the CAS multiframe is independent of the CRC-4 multiframe. Even though the CRC-4 multiframe has a specific sequence (that is, the C1 bits are in frame 0 and frame 8), frame 0 of the CAS multiframe needs to be aligned only with either the FAS or NFAS frame word. Therefore, for both FAS and NFAS alignments, frame 0 of the CAS multiframe can be in any of 8 different positions relative to frame 0 of the CRC-4 multiframe. CAS and CRC-4 alignment search start after basic frame alignment is accomplished.

In the Rx path, the multiframe pulse delivered to the backplane can be sourced by either the CAS or CRC multiframes and can be programmed by the user. Both CAS (TS16) and CRC-4 multiframing can be employed simultaneously. The transmit multiframe signal can correspond to either the CAS or CRC-4 multiframe sync pulse. If a transmit multiframe is assigned to the CRC-4 multiframe pulse, the CAS multiframe can be aligned to either a FAS or NFAS basic frame. The user can select FAS or NFAS alignment for CAS.

8.10 E1 Alarm Overview

The next sections provide details for the following alarms:

- Section 8.11, “E1 Alarm: Red Alarm”
- Section 8.12, “E1 Alarm: Remote Alarm Indication”
- Section 8.13, “E1 Alarm: TS16 RAI”
- Section 8.14, “E1 Alarm: TS16 AIS”
- Section 8.15, “E1 Alarm: AIS”

8.11 E1 Alarm: Red Alarm

As with a T1 red alarm, an E1 red alarm indicates a loss of receive-side framing. Also, as with T1, for E1 there is no transmitted red alarm.

If an OOF condition persists for a period N or more, the OOF Alarm status bit (RED) goes active and a maskable processor interrupt is generated per ITU Q.516. The status register flag clears if no OOF occurrences are detected for a period M. The user can program the value of N and M from 125 microseconds to 8.19 seconds. The Loss Of The Frame (OOF) condition as well as the failure (red alarm) are reported in separate bits with change indicator and real-time status.

8.12 E1 Alarm: Remote Alarm Indication

An E1 Remote Alarm Indication (RAI) is declared if bit 3 of three consecutive NFAS words equals ‘1’, per ITU G.704. The alarm is cleared if three consecutive NFAS words have bit 3 equal to ‘0’. The receipt of remote alarm sets the status flag RAI and generates a maskable processor interrupt.

In the transmit side, RAI can be generated by a user command or as part of a consequent action upon a triggering receive condition. The triggering receive conditions are defined in the consequent actions section. The remote alarm is sent as long as the triggering receive event is present. (For details, see Section 11.3, “Alarm Handling and Consequent Actions”.)

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8.13 E1 Alarm: TS16 RAI

An E1 TS16 RAI alarm indicates a receive-side fault on the far-end and is therefore an indicator of local-side transmit path performance. Typically, a RAI is transmitted by a terminal in response to the detection of a red alarm.

In CAS multiframe mode, the TS16 remote alarm is transported in bit position 6 in TS16 of frame 0 per ITU G.704. A binary:

- '0' indicates a normal condition (the default)
- '1' indicates TS16 remote alarm

A TS16 RAI is declared when the TS16 RAI bit is set to '1' for two consecutive CAS multiframes. An alarm bit and maskable interrupt are generated upon detection. The alarm clears when the same bit is equal to '0' for two consecutive multiframes.

In the transmit direction, in CAS multiframe mode, the TS16 remote alarm is in bit position 6 in TS16 frame 0. Transmitting a binary:

- '0' indicates a normal condition (default)
- '1' denotes TS16 remote alarm

The bit can be set manually by writing to the frame 0 TS16 register in the transmit signaling array.

TS16 RAI also can be sent automatically if the receiver automatic alarm response feature is enabled and the IXF3204 framer receives a triggering event. The triggering event is defined in the consequent actions section. (For details, see Section 11.3, "Alarm Handling and Consequent Actions".)

8.14 E1 Alarm: TS16 AIS

When the IXF3204 framer is set to receive CAS multiframe and if all ones are received in TS16 for a period of 1 multiframe, then time slot 16 AIS is declared per ITU G.775. This condition sets the flag bit and generates a maskable interrupt to the host processor.

The alarm clears when each of two consecutive multiframe periods contain four or more zeroes or when the MFAS signal is found.

In the transmit direction in CAS multiframe mode, TS16 AIS is a continuous transmission of all ones in time slot 16 for a period of at least 1 multiframe. Furthermore, the IXF3204 framer can be programmed to send TS16 AIS.

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8.15 E1 Alarm: AIS

An E1 Alarm Indication Signal (‘AIS’) indicates that the remote terminal is either off-line, or undergoing maintenance, or both. Also known as the “Keep-Alive” signal, it is generated to allow proper clock recovery on lines undergoing maintenance (therefore preventing excess jitter transmission and so on.).

The AIS condition is declared when the incoming signal has two or less zeroes in each of two consecutive doubleframe periods (521 bits total) per ITU G.775. The condition is cleared when each of two consecutive double-frame periods contains three or more zeroes or when the frame alignment signal is found.

The AIS condition as well as the failure (integration of the AIS condition) are reported in separate bits with change indicator and real time status.

In the transmit direction, the IXF3204 framer can send AIS as commanded by the user or as a consequent action to the reception of an incoming condition. (For details, see Section 11.3, “Alarm Handling and Consequent Actions”.)

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8.16 E1 Main Indicators

Table 36 lists the framing indicators the IXF3204 framer supports. The indicator function is listed along with a cross reference to the description of the function operation.

Table 36. E1 Main Indicators

Indicator	Cross Reference
Loss of CRC Multiframe (CRC mode only)	Section 8.6.5, "E1 Loss of CRC-4 Multiframe Alignment"
Far-End Block Error (CRC mode only)	Section 8.7, "E1 Remote End Block Error Operation"
Loss of Frame	Section 8.16.1, "E1 Loss of Basic Frame Alignment - FAS/NFAS"
Loss of Signaling (CAS) Multiframe (CAS mode only)	Section 8.16.3, "E1 Loss of CAS Multiframe Alignment"

8.16.1 E1 Loss of Basic Frame Alignment - FAS/NFAS

Per ITU G.706, loss of FAS/NFAS frame synchronization can be caused by several events, including:

- Three or more consecutive FAS words with either single or multiple bit errors
- Three or more consecutive NFAS words with bit 2 = '0'

The FAS, or the FAS and NFAS criteria can be used as the basis for loss of synchronization. A maskable interrupt is provided to indicate a Loss Of Frame synchronization. After frame synchronization is lost, the receiver immediately begins a search for a valid framing pattern, unless automatic resynchronization is disabled.

Loss Of Frame synchronization can also be detected by the reception of excess CRC errors. For details, see Section 8.6.5, "E1 Loss of CRC-4 Multiframe Alignment"

8.16.2 E1 Loss of CRC Alignment

CRC-4 Multiframe alignment is lost if two consecutive CRC MF alignment signals are received with errors. Loss of CRC multiframe is indicated and causes the generation of a maskable interrupt. This option can be enabled by the user. The default state is disabled.

If a minimum of 915 errored CRC blocks are detected out of a window of 1000, false frame alignment is indicated (Loss Of Frame) and a new search for frame alignment is started at a point just after the location of the assumed spurious frame alignment signal.

8.16.3 E1 Loss of CAS Multiframe Alignment

A maskable indicator indicates a Loss of CAS multiframe alignment. Multiframe alignment loss is reported if two consecutive CAS Multiframe Alignment Signals (MFAS) are received with errors.

As an option, multiframe alignment loss is reported if all the bits in TS16 are zeroes for the period of an entire multiframe. The all-zeroes option disallows the reception of all zeroes used in the signaling bit positions. If alignment is lost due to the all-zeroes condition, realignment takes place after a valid CAS multiframe is received in TS-16 following a frame in which the TS16 has at least one non-zero bit.

8.16.4 E1 Change of Frame Alignment

An E1 Change of Frame Alignment (COFA) condition is reported when the last receiver resynchronization results in a change of frame alignment. COFAs indicate that a new bit position is selected as the valid framing bit location, whereas OOFs indicate that only some percentage of the framing bits are in error. COFAs are always associated with an OOF. The IXF3204 framer provides a COFA indication bit in the port status register.

8.16.5 E1 FAS and NFAS Error Counting

In a one-second interval, there are 8000 E1 frames. One half of the frames have FAS words, and the other half of the frames have NFAS words.

- FAS errors occur when bits 2 to 8 do not match the binary pattern 0011011.
- NFAS errors occur when bit 2 of the NFAS byte is 0.

Error counters available include both (1) FAS error counters and (2) FAS + NFAS error counters. The error counters do not count errors when the IXF3204 framer either loses or is searching for basic FAS/NFAS frame synchronization.

8.16.6 E1 CRC Error Counting

When there is a discrepancy between the expected CRC-4 value and the received one, the CRC error counter is updated. Every second, the value of this counter is loaded to a register accessible by the host processor. The counters are active only when the framer is synchronized to the CRC structure.

8.17 E1 Receiver Resynchronization Control

When an Out Of Frame (OOF) condition is present, the IXF3204 framer can be programmed to resynchronize automatically (the default) or manually. Automatic resynchronization is qualified by an OOF. If automatic resynchronization is disabled, then when the framer gets into OOF, it stays there until it is able to synchronize.

The receive framer can be manually forced to resynchronize by writing a 0,1 sequence to a bit defined for that purpose. This sequence causes the framer to go out of frame and search for a new frame synchronization position.

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8.18 E1 Sa/Si Bit Access and Handling

The IXF3204 framer supports full access to all spare Sa bits (also known as the ‘National’ bits) and Si bits (also known as the ‘International’ bits). In the Tx direction, the Sa/Si bits can be generated from one of the following:

- Sa/Si registers
- The internal FDL controller (only Sa bits)
- The system backplane

8.18.1 E1 Sa/Si Bit Reception and Codewords

The user must program the Sa/Si change indicator to be generated either when (1) there is any change in the Sa/Si bits or (2) a check for stability in the nibbles (codewords) is required.

- If reporting of Sa/Si bits is required, the IXF3204 framer firmware uses the Rx HDLC modules 16 to 23 (one for each port) to store the TS0 data and extract the Sa/Si bits. [When requesting Rx national bit (Sa) reporting, the host processor cannot use Rx HDLC 16 to 23.]
- When the framing mode:
  - — Is CRC-4, then the Sa/Si bytes are aligned to the multiframe structure.
  - — Is not CRC-4, then no particular alignment is followed.
- The IXF3204 framer stores four bytes of Sa/Si information. Once these four bytes are ready and a change of value is detected, then an indication is set to inform the host processor. The four bytes of information that are stored are available until another four bytes of Sa/Si are received and updated. The IXF3204 framer provides specific registers for the host processor to access those four bytes of Sa/Si information.
- Any or all of the Sa bits can be selected and passed to the on-chip FDL controller to be configured as a data-link bit. The message data are accessible through a FIFO in the host processor bus.
- If enabled to do so, the IXF3204 framer detects for code stability.
  - — A codeword is defined as a 4-bit sequence in the Sa bits that is aligned to the CRC multiframe. The IXF3204 framer can check the stability of a codeword in any Sa bit.
  - — Codeword stability is defined as three consecutive codewords (that is, nibbles) with the same value. When a new, stable codeword is received, the indication is asserted. When there is not a sequence of three nibbles of the same value in a four-multiframe period, the IXF3204 framer firmware indicates this ‘instability’ to the host processor.

8.18.2 E1 Sa/Si Transmission and Codewords

Host processor-accessible registers hold a byte value for the Sa bits. The user can select the bits to be sourced from the internal registers (the default) or from the backplane in any combination.

The Sa4 to Sa6 bytes are aligned to the CRC-4 multiframe structure.

- If the CRC-4 multiframe structure is not defined in the Tx direction but CAS is defined, then the Sa4 to Sa6 bytes are aligned to the CAS multiframe structure.
- If neither CAS nor CRC-4 structures are defined, then the bits are sent in sequence from bit 0 to bit 7 without any further alignment.

Note: Si-bit servicing is not applicable when using CRC-4 multiframe structures.

8.19 Fractional E1 Mode

In Fractional E1 mode, the system side can be programed to source gapped-clock outputs for both the receive and transmit directions. As with T1, gapping is possible at a DS0 level and is programmed by using the number of DS0s to gap.

Gapped clocks are generated when the IXF3204 framer is the clock source. When the IXF3204 framer is a clock sink, it requires a continuous, non-gapped clock for correct operation. In this case clock gapping for fractional E1 must be handled externally.

Note: As with T1, for the fractional E1 mode:

- Gapping must be used in 1x streams only.
- Gapped clocks are generated only when the IXF3204 framer is the clock source. When the IXF3204 framer is a clock sink, it requires a continuous, non-gapped clock for correct operation. In this case, clock gapping for fractional E1 must be handled externally.

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9.0 Unframed Mode

The IXF3204 framer provides support for an unframed mode by selecting the transparent mode in either the Rx or Tx direction. In the unframed mode, for T1 or E1 signals the IXF3204 framer performs only the following:

- Line coding/decoding
- Rate adaptation. Supports different rates and phases on the line side and the backplane by using elastic stores (that is, slip buffers). Rate adaptation is sometimes called ‘rate adaption’.
- System backplane formatting

On the system backplane framing-pulse and time-slot information is maintained, but there is no alignment of the stream to the time slots. To properly transport the streams from the line side to the system side and the reverse, the same rates must be used.

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10.0 Signaling

This chapter outlines the methods by which signaling information is conveyed on T1/E1 links. (Signaling on J1 links is the same as for signaling on T1 links.) The following topics are discussed:

10.1 Signaling Overview

The IXF3204 framer provides direct support for the following types of signaling methods:

- Channel-Associated Signaling (CAS).

  As described in Section 10.2, "Channel-Associated Signaling", with CAS, each channel has its own signaling information. CAS is implemented differently between T1 and E1.

- Common Channel Signaling (CCS).

  As described in Section 10.3, "Common Channel Signaling", a dedicated channel can be used to convey signaling information. Applications that use this signaling method include ISDN-PRI (D-Channel), Telcordia GR-303, and V5.2 Digital Loop Carriers.

- Transparent.

  With this signaling method, signaling information is passed transparently (unaltered) through the IXF3204 framer. External means are required to insert and extract signaling information. Applications that use this signal method include SS7 and MF trunk signaling.

The type of signaling method used and the means of accessing this signaling information is fully user-configurable in the IXF3204 framer through the port configuration registers.

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10.2 Channel-Associated Signaling

Methods of Channel-Associated Signaling are the following:

- Section 10.2.1, “T1 Channel-Associated (Robbed-Bit) Signaling”
- Section 10.2.2, “T1 Channel-Associated Signaling: Per Time-Slot Enable”
- Section 10.2.3, “E1 Channel-Associated Signaling: Time Slot 16”
- Section 10.2.4, “E1 Channel-Associated Signaling: Per Time-Slot Enable”

10.2.1 T1 Channel-Associated (Robbed-Bit) Signaling

The SF/D4 T1 Channel-Associated Signaling is also known as ‘Robbed-Bit signaling’. It ‘borrows’ the LSB in each time slot of frames 6 and 12 to transport signaling information such as on-hook/off-hook and ringing/no-ringing for an associated time slot. Signaling bits borrowed from time slot N transport signaling information for time slot N (where N = 1 to 24). The naming and meaning of each bit both depend on the signaling type being used.

Table 37 lists:

- The signaling types (SF, SLC®96, or ESF)
- The four signaling bits that carry the signaling information (A, B, C, D). All signaling bits represent binary information, except when 9-state signaling is selected. (For 9-state signaling, see Table 38.)
- The resulting signaling modes (either ‘none’, or 4-state, 9-state, or 16-state)

The IXF3204 framer both encodes and decodes this type of signaling information. Four bits [A, B, A prime (A’), and B prime (B’)] represent the signaling information on the dedicated backplane signaling ports and through the host processor interface bus. [If the A bit is toggled, it is shown as A prime (A’) and it the B bit is toggled, it is shown as B prime (B’).]

Note: Robbed-bit signaling can be disabled on a per-time-slot basis, which allows for both transparent signaling and clear-channel applications.

Table 37. T1 Robbed-Bit Signaling Use

Signaling Types			Signaling Bits				Signaling Modes
SF	SLC®96	ESF	A	B	C	D	
X	X	X					None
X	X		X	X			4-State
	X		X	X			9-State
		X	X	X	X	X	16-State

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Table 38 lists the bit mapping for the SLC®96 nine-state signaling mode. In this mode, the two signaling bits provide a maximum of nine states by using a three-level logic system that allows for the A and B bits to take the values of either all ones, all zeroes, or alternating ones and zeroes.

Table 38. SLC®96 Nine-State Signaling Mode Bit Mapping

Signaling Bit Pattern	Mapped Code ABA'B'
A = 0, B = 0	0000
A = 0, B = 1	0101
A = 1, B = 0	1010
A = 1, B = 1	1111
A = 0, B = T	0100 or 0001
A = 1, B = T	1011 or 1110
A = T, B = 0	0010 or 1000
A = T, B = 1	0111 or 1101
A = T, B = T	0011 or 0110 or 1100 or 1001

10.2.2 T1 Channel-Associated Signaling: Per Time-Slot Enable

With Channel-Associated Signaling, when in CAS mode and an application is T1 the user can select per time-slot enable. In this case, the IXF3204 framer allows the user to mark any time slot for transparent signaling or equivalently as a clear channel.

A register allows the marking of time slots that do not carry robbed-bit signaling. When any of the register bits is set to '1' then:

- On the transmit side, the corresponding time slot is marked as transparent/clear and robbed-bit signaling is not inserted.
- On the receive side, disabling a bit removes the 'signaling change' indication for each of the time slots marked.

10.2.3 E1 Channel-Associated Signaling: Time Slot 16

E1 Channel-Associated Signaling uses time slot 16 to transport signaling information in frames 1 through 15 of the CAS multiframe. The CAS multiframe structure supports channel- associated signaling for 30 of the 32 64-kbps channels in the E1 frame. In E1, all signaling bits represent binary information and the signaling mode is always 16-state signaling.

Table 39, from Section 8.8, "E1 Channel-Associated Signaling Multiframe", is repeated here as a convenience to the reader. Table 39 lists how sixteen state words are imbedded in TS16. No signaling is associated with TS0 or TS16, as these time slots are overhead time slots and not payload channels.

Table 39. Time Slot 16 CAS Multiframe Structure

Frame Number	Time Slot 16	
	Bits 1 - 4	Bits 5-8
0	0000 MFAS[1]	XYXX[2]
1	ABCD TS1 Signaling ITU Channel 1	ABCD TS17 Signaling ITU Channel 16
2	ABCD TS2 Signaling ITU Channel 2	ABCD TS18 Signaling ITU Channel 17
n	ABCD TSn Signaling ITU Channel n	ABCD TS (n + 16) Signaling ITU Channel (n + 15)
14	ABCD TS14 Signaling ITU Channel 14	ABCD TS30 Signaling ITU Channel 29
15	ABCD TS15 Signaling ITU Channel 15	ABCD TS31 Signaling ITU Channel 30

NOTES:
1. MultiFrame Alignment Signal.
2. X: Spare Bits; Y: Remote Alarm Indication; 0: No Alarm; 1: Alarm.

10.2.4 E1 Channel-Associated Signaling: Per Time-Slot Enable

With Per Time-Slot Enable E1 Channel-Associated Signaling, when in CAS mode and an application is E1:

- On the transmit side, signaling for 30 channels is transmitted.
- On the receive side, the user can mark a time slot so that the 'signaling change' indication for each of the time slots marked is disabled.

10.3 Common Channel Signaling

Common Channel Signaling (CCS) is available in all framing modes for both T1 and E1. With this signaling mode, one or more time slots are selected to carry signaling data for all other time slots in the form of an HDLC message.

The IXF3204 framer has 8 independent HDLC controllers associated with the FDL module. Alternatively the 24 independent HDCL controllers can be configured for any data rate from 8 Kbps to the entire payload stream. If CCS is desired, then one of these controllers must be assigned to the associated line port and configured to the CCS time slot(s). The CCS data can then be accessed through the HDLC controller FIFO through the host processor interface.

10.4 Signaling Access

The IXF3204 framer provides the following methods to access signaling data.

- Through signaling registers accessible through the host processor interface bus (not discussed here)
- Transparently in the backplane data streams (also not discussed here)
- Through dedicated backplane signaling ports (discussed in the following text)

When signaling access occurs through dedicated backplane signaling ports, each backplane port can support independent transmit and receive streams. Each stream has associated data and signaling balls, as well as associated frame and multiframe pulses.

The format of the signaling bits presented to the backplane signaling ports vary according to the signaling mode selected. The IXF3204 framer adds a 4-bit stuff nibble to pad the 4-bit signaling nibble to fill an 8-bit byte.

As listed in Table 40, the format options for the signaling bits presented to the backplane are defined by configuring the two Signaling Byte Format Bits (SBFB). The value of the stuffing nibble can be defined either at the port level or at the DS0 (or time slot) level. When defined at the:

- Port level, all DS0s use the same stuffing nibble.
- DS0 level, each DS0 can carry a different value for stuffing.

Table 40. Signaling Byte Format Options

SBFB[1:0]	Signaling Byte[1]
00	SSSS SSSS
01	SSSS ABCD
10	ABCD SSSS
11	ABCD ABCD

NOTES:
1. SSSS is defined by the contents of the Stuff Nibble Definition Register (SNDR). ABCD represents the extracted signaling data.

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10.5 Signaling Processing Options

The IXF3204 framer supports the following options for processing signal information from the line side:

- Section 10.5.1, “Signaling Freeze”
- Section 10.5.2, “Signaling Debounce”

Note: Signaling can be forced at the DS0 level toward either the line or the backplane. To force signaling, the user must select the time slot and set the value, which is then sent continuously to the selected time slot and direction (either Tx line or Rx backplane).

10.5.1 Signaling Freeze

The IXF3204 framer provides a user-selectable signaling freeze capability, which allows call states to be maintained during brief Out Of Frame (OOF) periods.

This function operates as follows:

1. The signaling bits from two consecutive superframes are collected and buffered internally.
2. Two frames of bits are held in the signaling buffer so signaling integration can be implemented and one frame of bits is held in the output inserters.
3. After the correct signaling is determined, it is updated in the ‘stable’ section of the debouncing FIFO.
4. From the ‘stable’ section, the signaling values are sent to the backplane.
5. When the IXF3204 framer detects OOF, AIS, or LOS, and if a signaling freeze is enabled, then the ‘stable’ section remains unchanged so the same signaling value continues to be inserted into its corresponding stream.
6. This condition continues until the IXF3204 framer achieves frame synchronization and new values are received at least two frames, which updates the stable values.

10.5.2 Signaling Debounce

Signaling debounce can be activated in any signaling mode, which causes the receive signaling buffer to be updated for any channel only if all signaling bits do not change for two consecutive multiframes. In SLC®96 mode, the integration period is four 12-frame multiframes (48 frames).

When signaling debounce is not selected, the operation mode defaults to ‘FIFO mode’. In this case, a three- multiframe FIFO is used so signaling starts to be output to the backplane only after two full multiframes are received. The remaining functions such as ‘signaling freeze’ and ‘signaling change’ (discussed in Section 10.2.4, “E1 Channel-Associated Signaling: Per Time-Slot Enable”) are still available.

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11.0 Alarm Processing

This chapter discusses the following aspects of the IXF3204 framer alarm processes:

- Section 11.1, “Alarm Detection and Reporting”
- Section 11.2, “Alarm Integration”
- Section 11.3, “Alarm Handling and Consequent Actions”

11.1 Alarm Detection and Reporting

The IXF3204 framer detects alarms and reports them through interrupts and status bits. Some defect conditions are integrated in time and the result is designated a failure, which is also reported through interrupts.

For both defect and failure conditions, the main interrupts provided for alarms are the following:

- LOS - Loss Of Signal (Red Alarm)
- OOF - Out Of Frame (also known as a ‘Red Alarm’)
- AIS - Alarm Indication Signal (Blue Alarm)
- RAI - Remote Alarm Indication (Yellow Alarm)

In the case of any failure, an integration period is defined to set or clear the condition. The defect indication is set as soon as the event is received.

Other interrupts are provided that reflect detection of anomalies or other events. For details, see the memory map document for the IXF3204 framer.

For certain detected events, the user can program consequent actions based on the event. (For details, see Section 11.3, “Alarm Handling and Consequent Actions”.)

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11.2 Alarm Integration

The IXF3204 framer integrates the following alarms: LOS, AIS, OOF, and RAI.

The algorithms used to declare the alarms are related to the operation mode as defined by the user. In addition, the user can define the amount of time that it takes to detect either the presence or absence of a failure.

After reset, the default settings for T1, E1, and J1 are the following:

- Clear = 8.19 seconds
- Set = 2.5 seconds

The user can modify four values: (1) set E1, (2) clear E1, (3) set T1/J1, and (4) clear T1/J1. Each of these values can be from 125 microseconds up to 8.19 seconds.

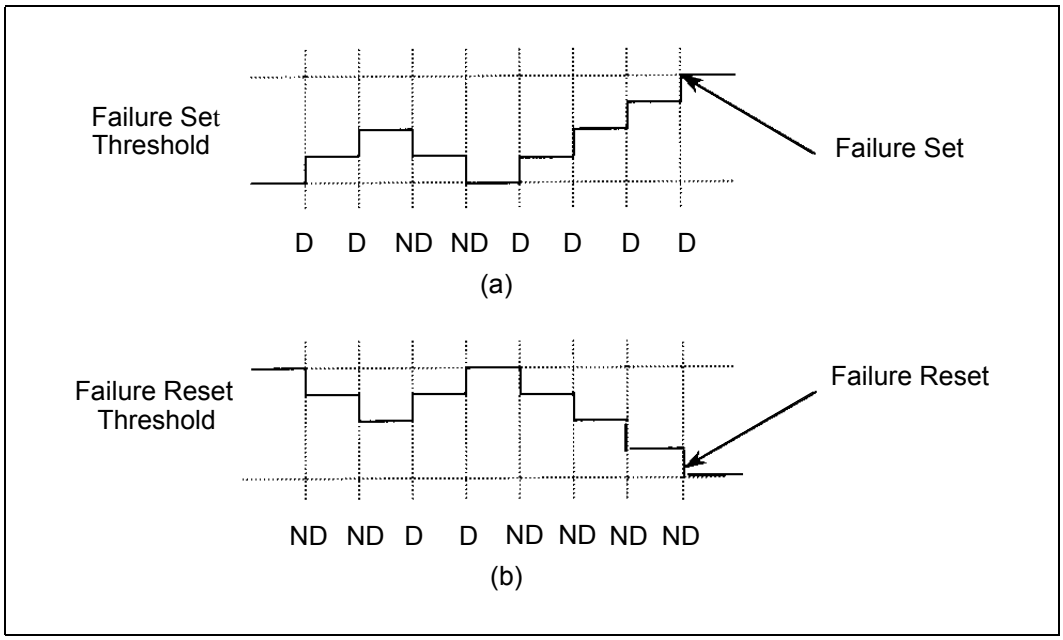
The alarm is evaluated in windows of 125 microseconds. When the current state of the failure is 'clear' and the defect is found inside of the 125-microsecond window, a counter is incremented.

Figure 11 shows the threshold for both failure set and reset.

- **Failure Set.** If the counter reaches the failure set threshold, then the 'failure set' condition is declared. If before reaching the 'set' condition, a window is found with the defect not set, then the counter is decremented by one. In this way, some gaps are allowed in the defects.
- **Failure Reset.** If there are sufficient intervals that pass without a defect being present, then the 'failure reset' condition is declared.

Note: In Figure 11, ND = No Defect and D = Defect.

Figure 11. Set and Clear Processes for Failure Detection



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11.3 Alarm Handling and Consequent Actions

When an event triggers an alarm, the alarm generates a consequent action if the user has programmed one. Defects and anomalies that are detected in the receive stream trigger actions that affect a signal going toward the transmit line stream and the receive backplane stream. In addition, detection of loop codes can be used to trigger actions such as setting or removing loopbacks.

Table 41 lists the consequent actions on the Tx line and Rx backplane sides. Both the actions to be performed and the priority are programmable. For example, AIS and RAI cannot be sent at the same time as a consequent action of LOS. The user must program only one of them. However, RAI and a codeword can be sent as a consequent action in E1 streams.

- Under OOF, LOS, or AIS conditions, the alarm module sends to the backplane module either an 'AIS/AUXP send' indication or a user-defined pattern indication. The user can select an RAI, AIS, or codeword (E1 format) transmission to the line side. When transmission of E bits under OOF is enabled, CRC error information is transmitted. For details on how to enable the transmission of E bits under OOF, see the memory map document for the IXF3204 framer.
- Under interworking conditions, the user can select a RAI, AIS, or codeword (E1 format) transmission to the line side. Under this condition, E bits can be set.
- Under a loss of CAS multiframe condition, the user can select an RAI, AIS, or codeword (E1 format) transmission to the line side.
- Under a LOS condition and if LOF has not yet occurred, CRC error information is transmitted.
- If an in-band loop code is detected, the module enable/disable loop indication signal enables or disables the local or payload loopback in the loop module. This signal can be set by hardware (an internal in-band loop module).
- At any time, the host processor can program any alarm transmission by the IXF3204 framer by writing the proper values to the module that sends the alarm.

Table 41. Consequent Actions (Sheet 1 of 2)

State on Rx Line	Consequent Actions on Tx Line	Consequent Actions on Rx Backplane
OOF Out Of Frame detected in the Rx Framer	Transmit RAI or AIS or AUXP or codeword (E1 mode). E bits can be set to value '0'. The user can define the value of the Sa5-bit when sending a codeword as a consequent action. (This operation relates only to the E1 mode.) Multiframe AIS can be set (E1 mode).	Send AIS or AUXP or user-defined code
LOS Loss Of Signal detected in the line module	Transmit RAI or AIS or AUXP or codeword (E1 mode). E bits can be set to value '0'. The user can define the value of the Sa5-bit when sending a codeword as a consequent action. (This operation relates only to the E1 mode.) Multiframe AIS or multiframe RAI can be set (E1 mode).	Send AIS or AUXP or user-defined code

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Table 41. Consequent Actions (Sheet 2 of 2)

State on Rx Line	Consequent Actions on Tx Line	Consequent Actions on Rx Backplane
AIS Alarm Indication Signal detected by the line module	Transmit RAI or AIS or AUXP or codeword (E1 mode). E bits can be set to value '0'. The user can define the value of the Sa5 bit when sending a codeword as a consequent action. (This operation relates only to the E1 mode.)	Send AIS or AUXP or user-defined code
Loss of CRC Multiframe	Transmit RAI or AIS or AUXP. E bits can be set to '0'. **NOTE:** Loss of CRC multiframe can occur due to the following: • The 8-millisecond timer expired. • CRC errors >= 915. • The 400-millisecond timer expired (CRC interworking).	
Loss of CAS multiframe	• Transmit RAI • Transmit multiframe RAI • Transmit multiframe AIS	
Reception of multiframe RAI	Transmit multiframe RAI	

Loop up/down codes	• In T1/D4 interrupt mode, the loop-up applies to line loopback operations per PUB 54016.
	  • Activation occurs when the in-band pattern '00001' is received for 5 ± 0.5 seconds.
	  • Deactivation occurs when the in-band pattern is '001' for 5 ± 0.5 seconds.
	• In T1 ESF mode, depending on the BOP sequence detected, either line loopbacks or payload loopbacks occur.	

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12.0 Facility Data Link

This chapter discusses the following Facility Data Link (FDL) topics:

12.1 FDL Features

FDL features include the following:

- Support for T1, J1, and E1 data-link communication
- Per-port enable/disable
- HDLC engine that can be mapped to support Common Channel Signaling (CCS)
- E1-specific functions:
  - Support for FAS/NFAS, CRC-4, and CAS E1 superframe formats
  - Configurable E1 Sa data-link bits
- T1-specific functions:
  - Detection/generation of Bit-Oriented Codes (BOPs) for T1 ESF and J1-24 streams.
  - Detection/generation of Derived Data Link (DDL) bits for T1 SLC®96 modes
  - Detection and transmission of T1 ESF PRM

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12.2 FDL Module Messages

The FDL module has several sections that manage the following types of messages:

- PRM (Section 12.3, “FDL Performance Report Messaging”)
- DDL (Section 12.4, “FDL Derived Data Link Message”)
- MOP (Section 12.5, “FDL Message-Oriented Protocol for HDLC Messages”)
- BOP (Section 12.6, “FDL Bit-Oriented Protocol Module for Messages”)
- CCS (Section 12.7, “FDL Common Channel Signaling Messages”)

The HDLC section of the FDL module is used to detect both MOP messages and PRM (which is a subset of MOP messages). BOP, PRM, and a user-defined MOP can all be received in the same data link.

12.3 FDL Performance Report Messaging

In a T1 ESF frame, the format for the IXF3204 framer PRM is a subset of the complete HDLC LAPD protocol specified in ITU-T Q.921. The frame format is the same, but it uses specific address values. The first three bytes of the PRM must be one of the following (from MSB to LSB):

- 00111000 / 00000001 / 00000011 - a message from the network interface (NI)
- 00111010 / 00000001 / 00000011 - a message from the customer interface (CI)

The PRM message-information field has 8 bytes and the CRC check-sequence field has 2 bytes. The PRM detector uses the first three bytes of a message to compare with the bytes for the NI and CI case. If the PRM detector bytes match those for either the NI case or the CI case (that is, whatever the user programmed), then the 8 information-field bytes are stored in a register section and an indication is generated.

The IXF3204 framer on-chip processor reads the PRM every second and generates a performance-related database. The PRM is also available for the host processor to read.

In the transmission direction, the IXF3204 framer on-chip processor generates every second a message that is sent even if the bit-oriented protocol (BOP) is currently being used. (PRM has priority over any message currently sent that uses BOP.) After the IXF3204 framer sends PRM, the BOP re-starts.

In some cases, the host processor uses the HDLC FIFO to send an HDLC message that uses the message-oriented protocol (MOP). In these cases, the IXF3204 framer sends PRM only after the HDLC message is completely sent. The host processor can control the generation of PRM by disabling the internal generation of the PRM.

12.4 FDL Derived Data Link Message

A Derived Data Link (‘DDL’) message is used to transmit control and alarm information. DDL bits are carried by the Fs bits of the SLC®96 superframe format for T1. They conform to the format specified in the Telcordia TR-TSY-000008 recommendation.

The DDL groups 24 bits into the following six fields:

- Concentrator fields (‘C’ bits C1 to C11)
- First spoiler field (bits fixed to ‘010’) For details on the first spoiler field, see Table 24.
- Second spoiler field (a bit fixed to ‘1’) For details on the second spoiler field, see Table 24.
- Maintenance field (‘M’ bits M1 to M3)
- Alarm field (‘A’ bits A1 and A2)
- Protection line switching field (‘S’ bits S1 to S4)

DDL bits are always received when the FDL module is in T1 SLC®96 mode. Information fields are stored in a register section, and no further processing is performed.

DDL bits are transmitted in a fashion similar to how DDL bits are received. There are three bytes available for the host processor to write the DDL bits. The FDL module generates an indication of ‘new DDL required’. The host processor then has one SLC®96 multiframe (that is, 9 milliseconds) to set the values. Once the new DDL is set, it is sent in the next frame. If the host processor does not change the value of the DDL registers, the same value is sent in every frame.

DDL bits are stored in three bytes. Once the three bytes are completely received, they are output to registers available to the host processor in the format listed in Table 42. Then status flags are updated to report that a new DDL message is received.

Table 42. Storage Format for DDL Bits

Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	C6	C5	C4	C3	C2	C1
2	M3	M2	M1	C11	C10	C9	C8	C7
3	0	0	S4	S3	S2	S1	A2	A1

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12.5 FDL Message-Oriented Protocol for HDLC Messages

The Message-Oriented Protocol (MOP) is used to detect both of the following:

- HDLC opening/closing flags (01111110)
- HDLC aborting sequences (1111111)

An HDLC message is declared to:

- Start (open) when the following occurs:
  - First, an HDLC opening flag is detected (01111110).
  - Second, a byte is detected that is different from either an aborting sequence or the HDLC flag (which is the same for both opening and closing an HDLC message).
- Close when an HDLC closing flag (01111110) is detected. At that moment, the received Frame Check Sequence (FCS) fields are compared with the calculated field.

In the transmit direction, the IXF3204 framer performs the flag insertion, stuffing, and CRC generation for data the user stores in the HDLC Data FIFO.

12.6 FDL Bit-Oriented Protocol Module for Messages

A bit-oriented protocol (BOP) module is a sequence of 16 bits (‘111111110xxxxxx0’):

- Eight ones
- One zero
- Six bits (xxxxxx) that are a BOP code
- Another zero

The sequence for the BOP module is as follows:

1. The BOP module detects sequences of eight consecutive ones and a ‘0’ (111111110).
2. The BOP module stores the next 6 bits and checks that the last bit is a ‘0’, in which case a BOP has been received. The BOP is not declared until it has been received N consecutive times, where N is by default 10. The user can program this number N to be from 1 to 15.

The IXF3204 framer provides ‘BOP received’ indicators. The RAI alarm BOP (00_H) can either be managed as a normal BOP or it can be enabled to be declared when 16 consecutive BOP = 00h are received.

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12.7 FDL Common Channel Signaling Messages

Support for Common Channel Signaling (CCS) messages is managed in one of the following ways:

- One of the HDLC controllers available manages the CCS. In this case, the user can support CCS by selecting and mapping one of the HDLC controllers to any time slot in the HDLC module.
- The internal HDLC section of the FDL module manages the CCS. In this case, CCS support is performed by mapping the HDLC section of the FDL module to any time slot in the data stream. When the operation mode is:
  - T1 ESF mode, the IXF3204 framer supports concurrent reception of BOP and CCS messages.
  - T1 SLC®96 mode, the IXF3204 framer supports concurrent reception of DDL and CCS messages.

12.8 FDL Module Interactions

The IXF3204 framer defines a handshake to interact with the FDL module. To ensure reliable operation of each section of the FDL module, the host processor must follow the handshake.

There are independent procedures to send PRM, and MOP and BOP messages. (The priority for PRM, MOP, and BOP messages is given in Section 12.3, “FDL Performance Report Messaging”.)

The following sections describe various IXF3204 framer interactions with the FDL module:

- Section 12.8.1, “Interactions with Performance Report Monitoring”
- Section 12.8.2, “Interactions with Message-Oriented Protocol Module”
- Section 12.8.3, “Interactions with Bit-Oriented Protocol”

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12.8.1 Interactions with Performance Report Monitoring

Figure 12 shows how the IXF3204 framer receives PRM.

The user must enable detection of PRM and select the required three bytes to compare for the message to be recognized as PRM. The default values of those registers are 38h, 01h, and 03h. When the IXF3204 framer detects PRM, an indication is given. The IXF3204 framer internal processor manages the PRM module unless the user disables it.

Figure 12. Reception of PRM

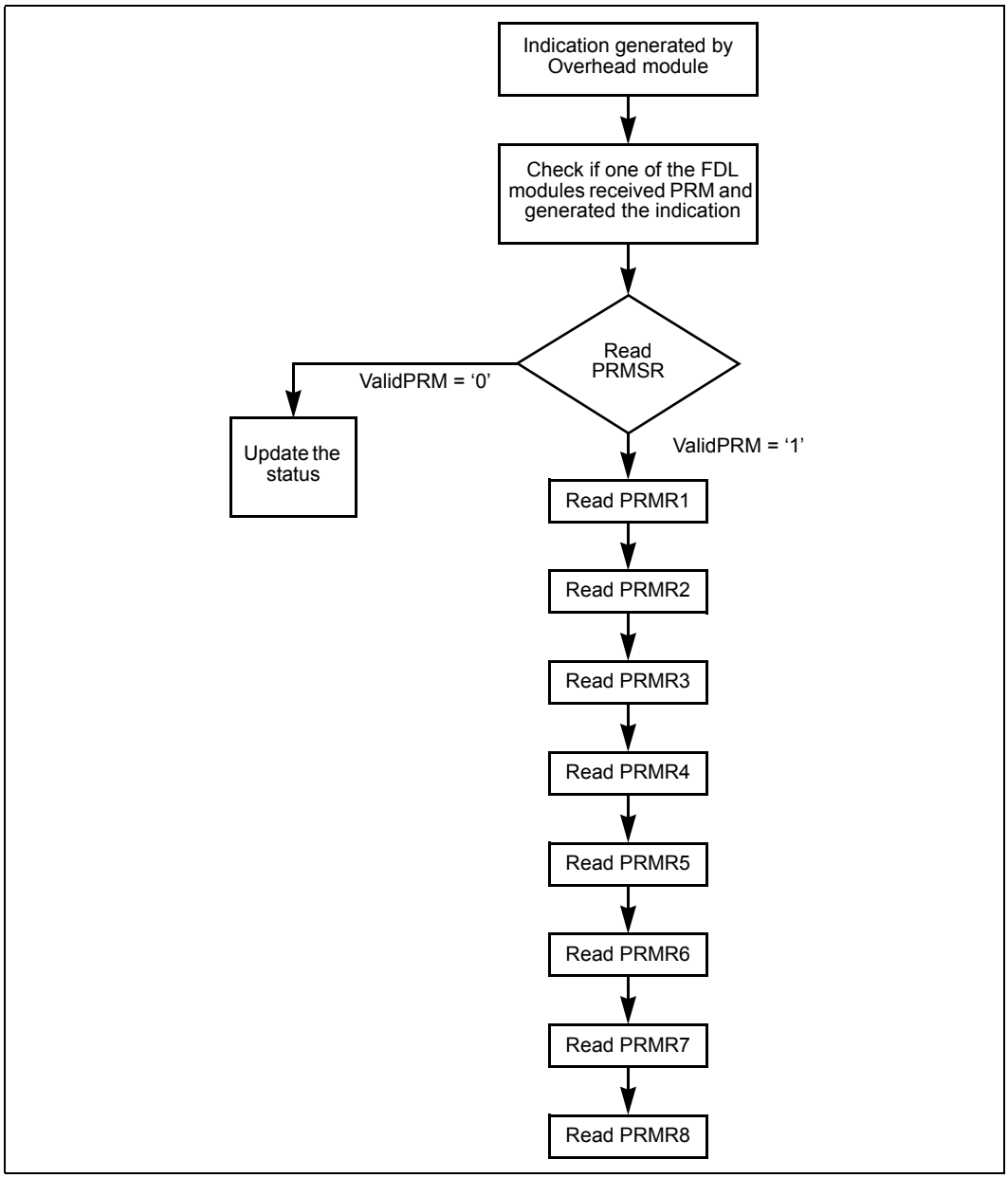

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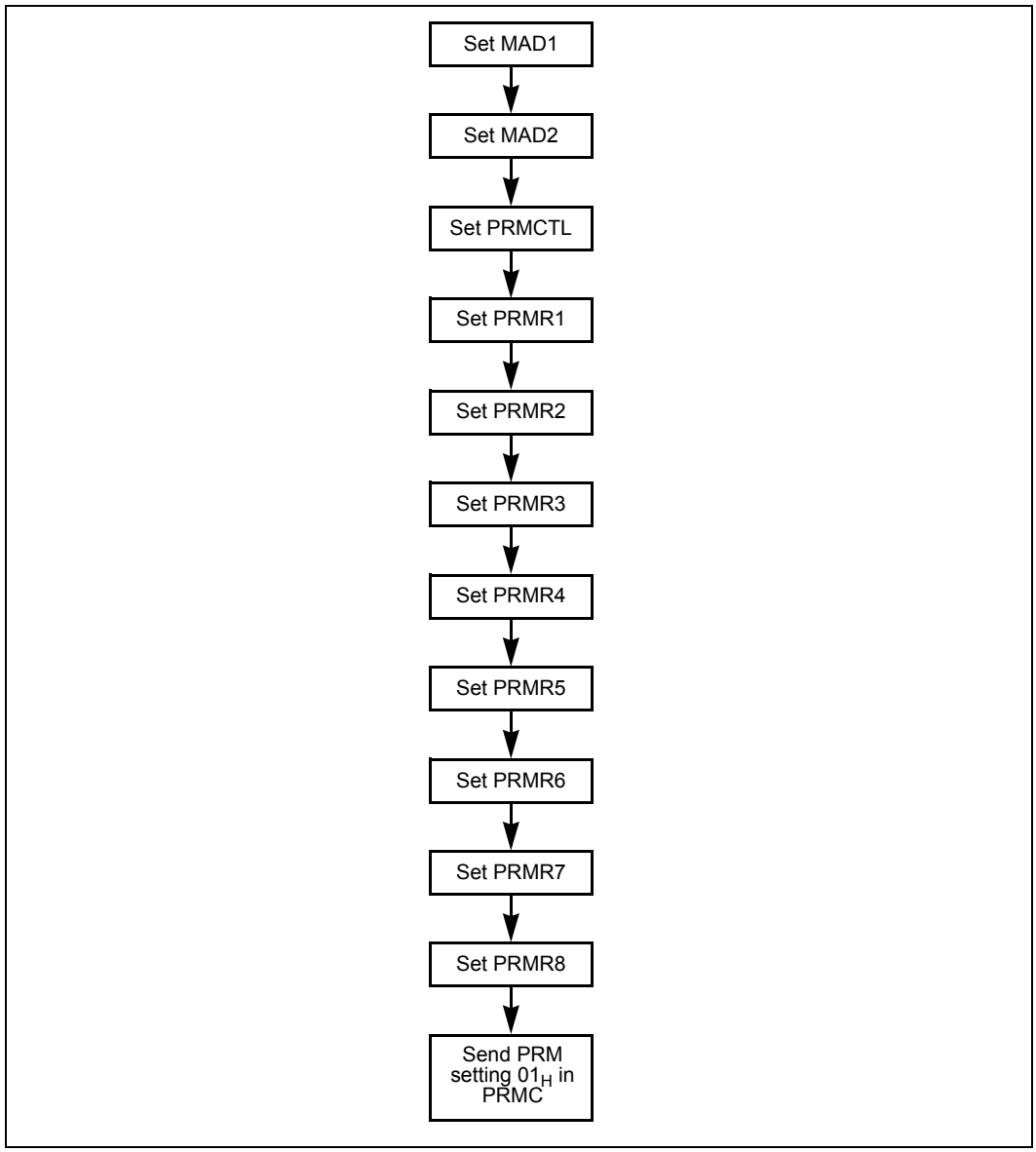
Figure 13 shows how the IXF3204 framer transmits PRM.

The IXF3204 framer internal processor generates PRM every second. Once the data are generated, the data are stored in the transmit section and then sent to the line automatically.

However, if the user elects to transmit PRM from the host processor, the user must first set the three address bytes, then set the eight data registers, and then set the 'send PRM' bit. The IXF3204 framer internal processor must be commanded not to send PRM so that the host processor can control the data registers.

Note: For details on PRM registers, see the memory map document for the IXF3204 framer.

Figure 13. Transmission of PRM



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12.8.2 Interactions with Message-Oriented Protocol Module

Reception and transmission of MOP HDLC messages follows the same procedure as the one described for HDLC modules in Section 12.5, "FDL Message-Oriented Protocol for HDLC Messages".

12.8.3 Interactions with Bit-Oriented Protocol

Figure 14 shows how the IXF3204 framer receives bit-oriented protocol (BOP) messages.

Once the IXF3204 framer detects that a BOP message is received at least N times (that is, 1 to 15 as specified by the user), it generates an indication. The user must check the valid BOP indication and the BOP code. Reception of a BOP code can be checked in either with a continuous mode or with a gap mode.

- In continuous mode, only when N continuous BOP codes are received can the BOP code be deemed valid.
- In the gap mode, if two consecutive BOP codes are detected, then starting at that point a gap of one code is allowed until the counter reaches a count of N. This mode allows for bit errors in the BOP code reception to be supported with a limit of one BOP in error between two good BOP codes detected.

Figure 14. Reception of BOP Message

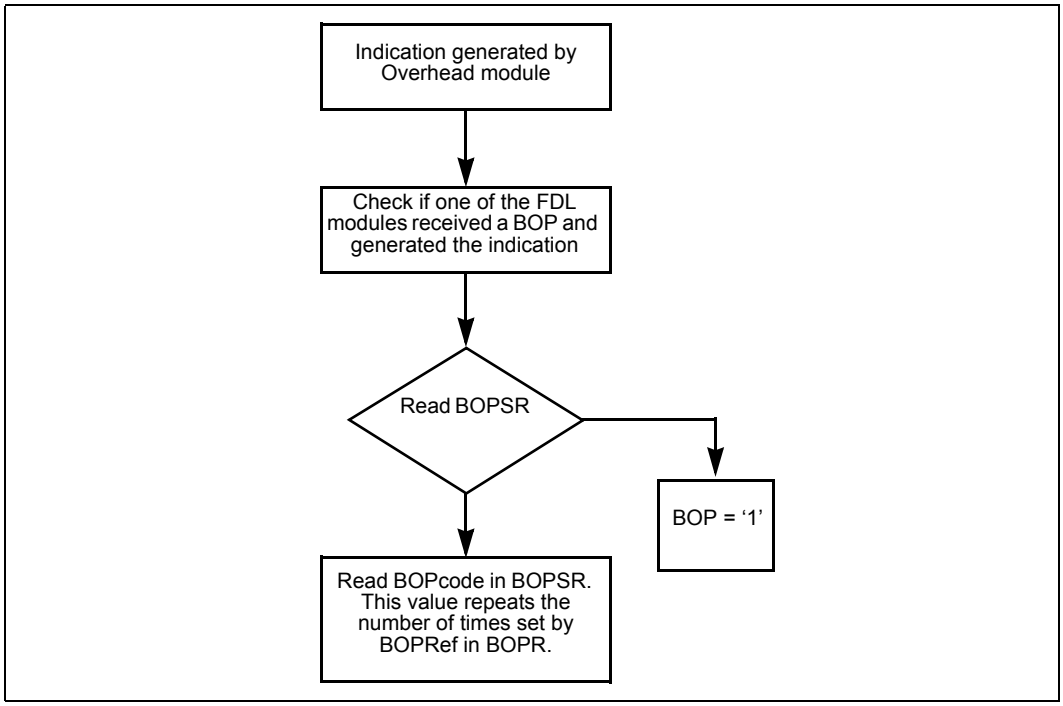

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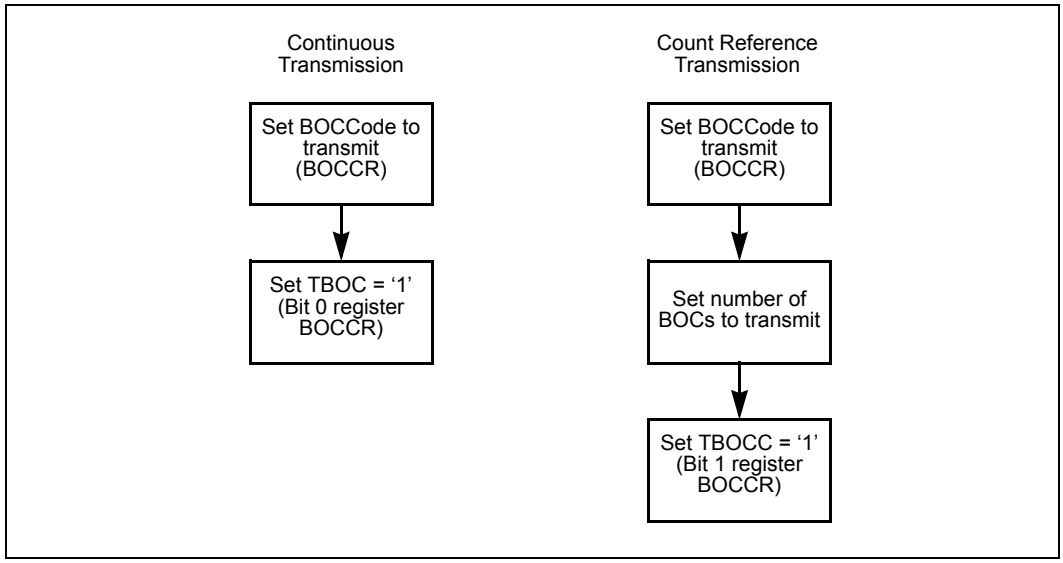
Figure 15 shows how the user can enable the IXF3204 framer to transmit a BOP message in one of two ways:

- Continuous transmission, in which the message is sent continuously until the message sending process is stopped
- Count reference transmission, in which the user can send a BOP code for a specified number of N times (from 1 to 65535)

Note: For details on BOP-message registers, see the memory map document for the IXF3204 framer.

Figure 15. Transmission of BOP Messages



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13.0 Slip Buffers

The slip buffers in the IXF3204 framer are always engaged. They can be set either to minimum delay or two frames.

13.1 Minimum-Delay Slip Buffers

When the slip-buffer mode selected is for minimum delay, the read and write pointers are typically close to each other, with an average distance of three time slots. In minimum-delay mode, slip operations are indicated but not executed. A slip operation indication means that either an overlap of the pointers is detected or that the separation exceeds six time slots. This indication is useful to the user for fine-tuning the timing settings.

13.2 Two-Frame Slip Buffer

When the slip-buffer mode selected is for the two-frame mode, the slip buffer generates one of the following options:

- Slip Repeat: A frame is repeated.
- Slip Delete: A frame is deleted.

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13.3 Slip Buffer Re-Center Process

The IXF3204 framer provides a re-center process to be performed either under host-processor control or whenever the IXF3204 framer detects a Change Of Frame Alignment (COFA).

The re-center process, which is performed only on frame boundaries, occurs as follows:

1. The slip buffer waits for the read pointer to be on time slot 0.
2. The slip buffer performs a re-center operation by selecting the best distance between the read and write pointers, depending on the mode.
3. When the slip buffer mode is:
   a. Minimum-delay mode, the distance is minimized by selecting the proper page for read and write pointers.
   b. Two-frame mode, the slip buffer maximizes the distance between the read and write pointers. (Two pages are available, each containing one frame.)

In the re-center process, the slip buffer indicates the type of slips occurring and maintains information on the number of slips generated in the last second, after which the IXF3204 framer counters are updated with an internal one-second signal.

The host processor can read the distance between pointers at any time. An absolute value is provided.

Note: The user can enable the re-center process to be performed automatically whenever either the line side or the backplane side detect a COFA. This operation is useful to separate the pointers as much as possible even if a change of time slot 0 position happens on either side of the slip buffer. A COFA in the backplane side is generated if an external device is providing the framing pulse and its position is changed.

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14.0 Backplane Specification

This chapter discusses the following backplane topics:

14.1 Backplane Features

Backplane features include the following:

- User-defined framed code insertion
- Unframed AIS and AUXP insertion
- T1-to-E1 channel mapping both in non-fourth time slots and according to ITU-T G.802
- BERT towards the backplane
- Serial TDM bus interfaces with fractional streams and stream replication supporting MVIP, H-MVIP, ST, CHI, and H.100 at the signal waveform level
- Framing pulse synchronization and data-alignment functions
- Multiframe pulse propagation to/from the line side through the slip buffers

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14.2 Backplane Interface

The backplane interface connects to external balls that support any of the backplane bus formats. Depending on the selected configuration parameters, the backplane can support several bus standards, thereby allowing the IXF3204 framer to integrate with other devices.

The backplane interface must allow a rate up to 8 times one rate (such as the E1 rate of 2.048 Mbps) so all four ports can be output/input in one single serial line. The backplane interface manages channel mapping (T1 to E1), PCM blanking (trunk conditioning), stream replication, and AIS insertion.

Table 43 lists the backplane bus formats the IXF3204 framer supports.

Table 43. Supported Backplane Bus Formats

Backplane Bus Format	Complete Name	Source
MVIP H-MVIP	Multi-Vendor Integration Protocol High-Density MVIP	Global Organization for Multi-Vendor Integration Protocol
H.100 CT Bus	Computer Telephony Bus	Enterprise Computer Telephony Forum
ST-Bus	Serial Telecom Bus	Mitel* Networks
CHI	Concentration Highway Interface	AT&T Microelectronics

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14.3 Backplane Bus Standards

The backplane bus standards that the IXF3204 framer supports include the following:

- Section 14.3.1, “MVIP Bus”
- Section 14.3.2, “H-MVIP Bus”
- Section 14.3.3, “H-100 Bus”
- Section 14.3.4, “1.544-MHz ST Bus”
- Section 14.3.5, “2.048-MHz ST Bus”
- Section 14.3.6, “CHI Bus”

14.3.1 MVIP Bus

Figure 16 and Figure 17 show the MVIP bus functionality. The synchronization pulse is negative and fixed to the first bit of the first time slot (TS 0). The signaling byte is ‘0000ABCD’, and it is aligned to each time slot byte. When the direction is:

- Rx, data are delivered on the rising edge and the framing pulse is delivered on the falling edge.
- Tx, data are sampled on the falling edge and the framing pulse is sampled on the rising edge.

Note: For Figure 16 to Figure 24, bit 1 is the first bit of the time slot.

Figure 16. MVIP Delivery (Rx)

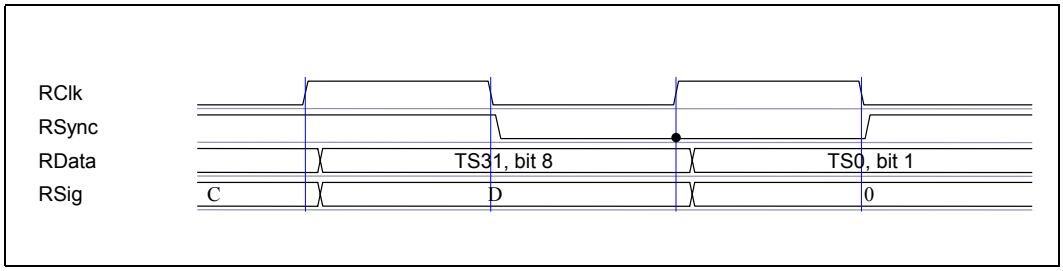
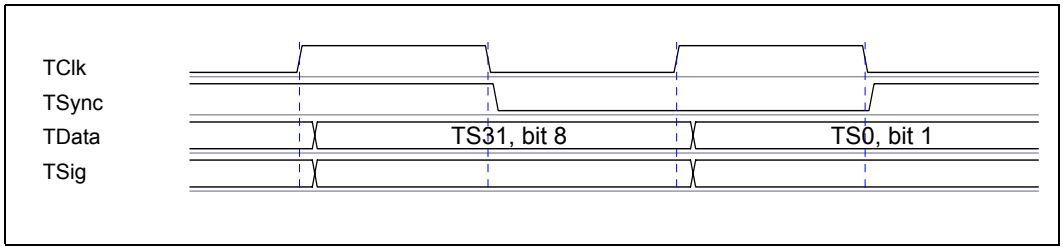


Figure 17. MVIP Sampling (Tx)



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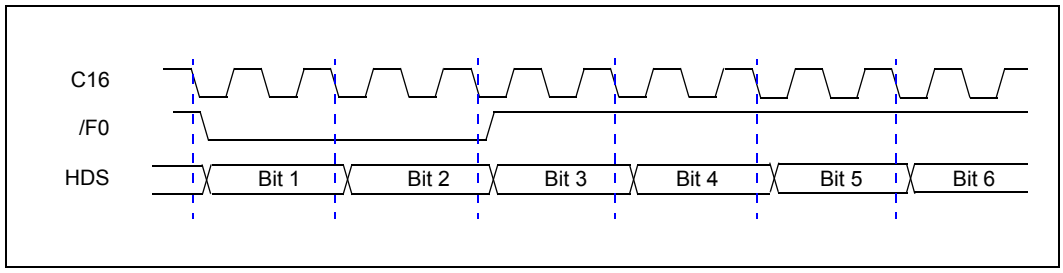
14.3.2 H-MVIP Bus

Figure 18 and Figure 19 show how the H-MVIP bus format manages within a single stream four byte-multiplexed ports. The synchronization pulse, which is negative, lasts two bit periods and it is fixed to the first bit of the first time slot. The 'C16' clock used is a 16-MHz clock (which equals 8 times 2.048 MHz). The 'HDS' data stream (HDS) and signaling stream (not shown but it follows the same waveform as HDS) are separate.

Figure 18. H-MVIP Waveform (Sync-Data)

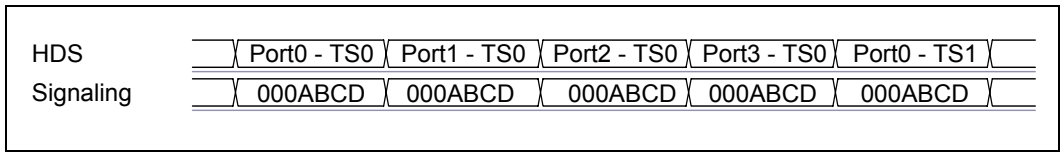


The H-MVIP standard calls for byte interleaving, so that time slot 0 is driven for port 0, and then time slot 0 is driven for port 1, and so on. Any time slot that is not driven must be placed into a tristate.

Each HDS can handle up to four 2.048 Mbps streams, byte interleaved. Data are delivered and sampled as follows:

- The data are delivered with the falling edge of C16.
- The data are sampled with the rising edge of C16, on the second phase.

Figure 19. H-MVIP Byte Interleaving



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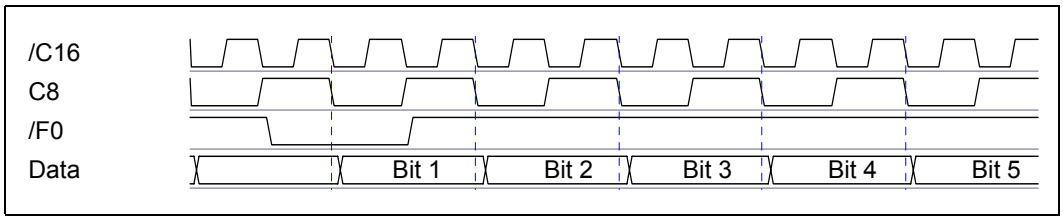
14.3.3 H-100 Bus

Figure 20 and Figure 21 show the H-100 bus functionality. The synchronization pulse is negative and fixed to the first bit (bit 1) of the first time slot used (TS 0). C16 is a 16-MHz clock signal.

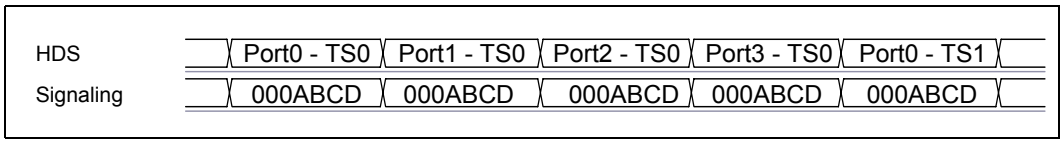
Figure 20. H-100 Waveforms (Sync-Data)



Each data signal can manage up to four 2.048-Mbps streams, byte interleaved or in any order. There is no restriction on the mapping. The H-100 bus must be considered a 128 TS bus. For a fair delay distribution, a byte-interleaved scheme can be used.

The sampling point is on the rising edge of the C16 clock, after the rising edge of the C8 clock. Data are delivered with the rising edge of C8 (falling edge of C16). Any TS that is not driven must be placed into a tristate.

Figure 21. H-100 Byte Interleaving

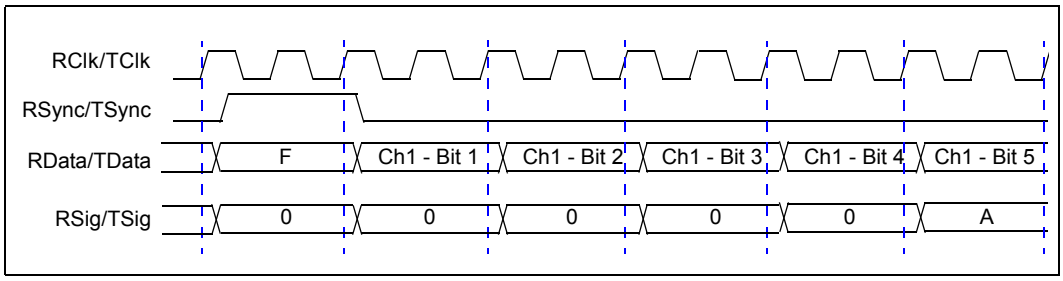


14.3.4 1.544-MHz ST Bus

Figure 22 shows an ST bus wave form at 1.544 MHz.

The RData/TData bus has 193 bits per frame, and each frame is repeated every 125 microseconds. The signaling byte is ‘0000ABCDh’. The upper nibble has a default value of ‘0000h’, but it can be configured with a user-defined value. The edge to sample and deliver data and sync is programmable. The sync pulse polarity and position can also be programmed. The sync pulse lasts one clock cycle.

Figure 22. 1.544-MHz ST Bus Wave Form



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14.3.5 2.048-MHz ST Bus

The RData/TData bus has 256 bits per frame and each frame is repeated every 125 microseconds. The signaling byte is ‘0000ABCDh’. The upper nibble has a default value of ‘0000h’, but it can be configured with a user-defined value in the Rx direction. The edge to sample and deliver data and sync are programmable. The sync pulse polarity and position can also be programmed. The sync pulse lasts one clock cycle.

14.3.6 CHI Bus

After power-up/reset, the CHI bus requires the data balls to be in a tristate. The data can be sampled/delivered with either the rising or falling edge of the clock. Also, the sync pulse can be sampled/delivered with either edge.

For the CHI bus, the position of the first bit of TS0 can be specified relative to the framing pulse. (Some limitations apply.) The positions are separated by clock transitions. The allowed locations are 3, 4, 5, 6...16, 17, 18.

In one operation mode, the clock can be run at twice (2x) the data speed. In this mode:

- Data are driven two clock cycles and sampled only on a clock edge defined by the user. Any of the four edges are available.
- The clock edges to deliver and sample can have only the following values:
  - Delivery: 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28, 31 and 32
  - Sampling: 6, 7, 10, 11, 14, 15, 18, 19, 22, 23, 26, 27, 30, 31, 34 and 35

The CHI bus supports the following modes:

- Data-only streams at 1x (see Figure 23)
- Data-only streams at 2x, 4x (not shown)
- Data stream with associated signaling at 2x (see Figure 24) or 4x (not shown)

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Figure 23 shows the CHI bus data-only stream at 1x. This mode has 32 time slots (256 bits) in a 125-microsecond frame. In this case, data are delivered as one bit every clock cycle.

When the data are in:

- An E1 data stream, the data fit completely in this mode.
- A T1 data stream, the 24 time slots are mapped in one of the two following modes: one-in-four or G.802.

Figure 23. CHI Bus Data-Only Stream at 1x

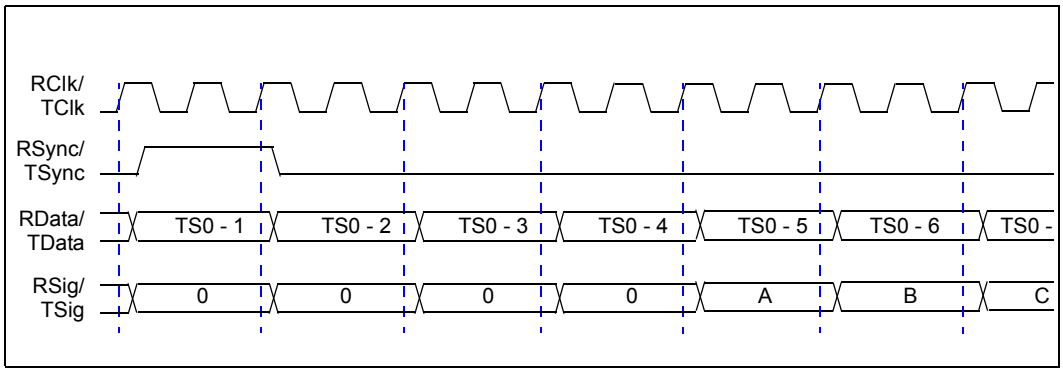
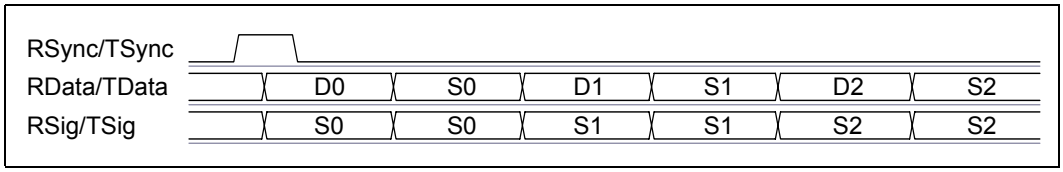


Figure 24 shows the CHI bus with data streams that have associated signaling at 2x. This mode has 32 time slots in a 125-microsecond frame. In this case, each time slot has 16 bits: 8 data bits and 8 signal bits.

Figure 24. CHI Bus Data Streams with Associated Signaling at 2x



14.4 Backplane Byte Replication

The IXF3204 framer backplane byte-replication feature allows the replication of a byte in the backplane interface in any of eight possible positions. The user can define replication of 2x, 4x, and 8x bytes. In each case, the user must define into which replicated position the data are driven. In the rest of the positions, the signal that the ball is driving is placed into a tristate.

Example:

If 4x replication is used, then the user can select from one of the following slots to be the slot where the data are driven: 0, 1, 2, or 3. If the selected slot is 2, then positions 0, 1, and 3 go into a tristate. (In this way, a higher speed bus can be generated by externally connecting several ports and properly selecting the replication slots.)

Note: H-MVIP waveforms can be constructed by selecting 4x replication in ports 2, 4, 5, and 6 and connecting them externally.

14.5 Backplane Concentration Modes

The IXF3204 framer supports a 'backplane concentration mode' in which four ports can be output on one ball. When the concentration mode is:

- 4x, the ball associated with port 0 outputs the data related to ports 0, 1, 2, and 3.
- 8x, the ball associated with port 0 outputs the data of the four ports, byte interleaved with port 0 byte output first, and then the byte of port 1 output, and so on.

In each case, the IXF3204 framer internally interleaves data so they are output in a byte-interleaved way. For example, in 4x mode the byte of port 0 is output first, and then the byte of port 1, and so on.

Note: H-MVIP waveforms can be generated on both ports 0 and 4.

14.6 Backplane Data Mapping

Internal per-time slot source mapping can be used to engage BERT and HDLC modules in either the Rx or Tx direction. In both the Rx or Tx direction, the data can be either the whole byte or only some of bits 0 to 7. When the direction is:

- Rx, mapping is used to determine if the source of a particular channel is to be the data from the line side, or the BERT, or any HDLC controller. In this way, BERT or HDLC messages can be sent to the Rx backplane balls.
- Tx, the data on backplane balls can be sent to the line side, or BERT or HDLC modules.

14.7 Backplane Byte Enforcements

Backplane byte enforcements apply only to the Rx direction. All ports can overwrite their normal data stream with a specific 8-bit pattern, which allows for functions such as PCM blanking, trunk conditioning, and AIS/AUXP insertion. The user can select the type of data-stream overwrite from among the following choices:

- Specific value. The user can force a specific value onto the datastream.
- User-specific pattern. Under specific maintenance conditions, the user can choose to transmit toward the backplane a framed pattern (all-zeroes, all ones, and so on). In this case, the byte in the user-configurable register is substituted for data bytes obtained from the RxSlipBuffer.
- AIS or AUXP insertion. Under specific maintenance conditions, the user can choose to transmit toward the backplane either an unframed all-ones code (AIS) or a 1:1 code (AUXP).

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14.8 Backplane T1-to-E1 Mappings

Two T1-to-E1 mappings are supported for the backplane:

- Section 14.8.1, “Channel-to-Channel Mapping”
- Section 14.8.2, “ITU-T G.802 (Annex B) Mapping”

14.8.1 Channel-to-Channel Mapping

With this method, a 1.544-Mbps T1 signal can be accommodated within the E1 structure in a channel-per-time-slot basis. The T1 channel TS0 carries the F-bit information. Whenever TS mod 4 is different from the value ‘0’, then a T1 channel is inserted in the E1 stream.

Figure 25 lists the mapping between the time slot number and the T1 channel. (TS1 maps to channel 1, TS5 maps to channel 4, and so on.)

In Figure 25, ‘x’ means non-relevant data.

Figure 25. T1-to-E1 Per-Channel Mapping

Time Slot Number	0	1	2	3	4	5	6	7	8	9	10	11	12	13
T1 Channel	F Bit	1	2	3	x	4	5	6	x	7	8	9	x	10

.
.

Time Slot Number	18	19	20	21	22	23	24	25	26	27	28	29	30	31
T1 Channel	14	15	x	16	17	18	x	19	20	21	x	22	23	24

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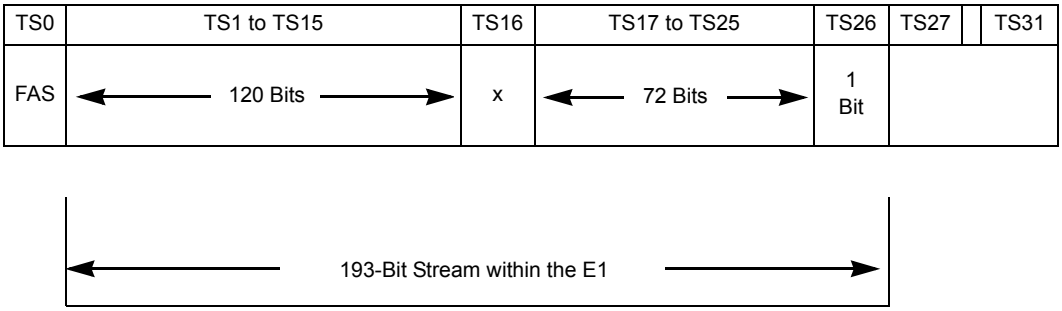
14.8.2 ITU-T G.802 (Annex B) Mapping

With this method, the 193-bit T1 structure to be accommodated within the E1 TS structure does not need a particular arrangement, such as channels. The 193 bits of an arbitrary 125-microsecond period of the 1544-kbps signal are to be accommodated within a structured 2048-kbps frame.

Figure 26 shows the mapping between the TS and the 193 bits that make up the complete T1 frame, where FAS is the Frame-Alignment Signal.

- The entire E1 TS structure includes all bits from TS0 through TS31.
- In contrast, the bit stream within the E1 TS structure for the T1 structure being carried includes only the following 193 bits:
  - The 120 bits from TS1 through TS15
  - The 72 bits from TS17 through TS25
  - The 1 bit in TS26

Figure 26. T1-to-E1 G.802 Mapping



On the Rx side case, the IXF3204 framer stores the following:

- F-bit in TS26 bit 0
- Channel 1 in TS1
- Channel 2 in TS2, on so on up to channel 15 in TS15
- Channel 16 is stored in TS17, and so on up to channel 24 in TS25

The memory map is organized such that the first global control section contains the information of the whole 8 ports regarding reset, interrupts, and status. Each port is mapped so that to gain access to similar information on each port, the user adds an offset to a base address. (For details, see the memory map document for the IXF3204 framer.)

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15.0 Timing Configurations

This chapter discusses the following timing configuration topics:

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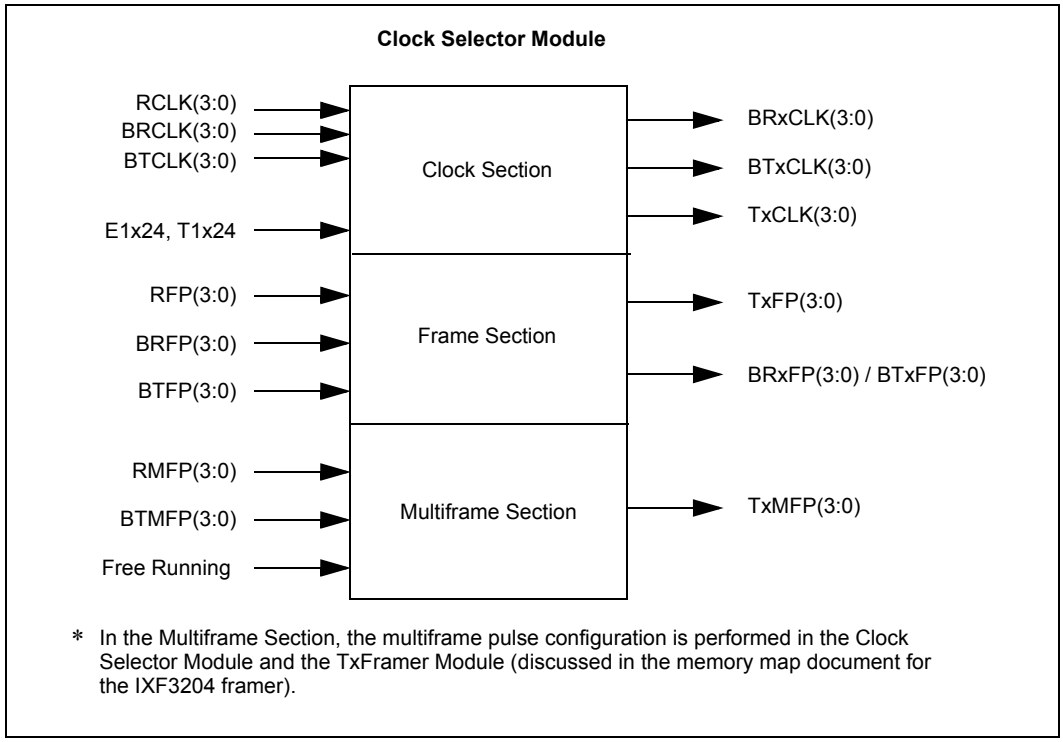
15.1 Clock and Frame-Pulse Timing Configuration

All timing information is concentrated in one selector module, from where it is distributed to all other regions.

Figure 27 shows the clock selector module inputs and outputs.

Figure 27. Clock Selector Module Inputs and Outputs



Timing configurations manage two aspects of device configuration: clocks and frame-pulse selection.

Sources for clock configurations are the following:

- Rx line clock (RCLK)
- Rx backplane clock (BRCLK) and Tx backplane clock (BTCLK)
- External clocks from E1x24 or T1x24 balls, divided down to 1x
- Signal from the phase-locked loop whose input is the Rx line clock or Tx backplane clock (in Figure 28, PLLCLKRX or PLLCLKTX)

Sources for frame-pulse configurations are the following:

- Rx line side (RFP)
- Rx backplane ball (BRFP) and Tx backplane ball (BTFP)
- Internally generated signals (not shown)

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15.2 Phase-Locked Loop Modules

There are two phase-locked loop (PLL) modules available: RxPLL and TxPLL.

- The RxPLL module uses the external E1 x 24 or T1 x 24 clocks to lock to any of the Rx line clock signals of the four ports. The output of this module is PLLClkRx.
- The TxPLL module uses the external E1 x 24 or T1 x 24 clocks to lock to any of the Tx system backplane clock signals of the four ports. The output of this module is PLLClkTx.

The PLL modules divide the reference signal to 8 kHz and perform the adjustments on phase after comparing the 8-kHz reference signal and the 8-kHz generated signal. The adjustment is done by shifting the phase by one clock period E1 x 24 or T1 x 24.

15.3 External and Internal Clocks

There are two balls for external clock sources: E1x24 and T1x24, which allow for clocks of 1, 8, 16, and 24 times the base frequencies for T1 or E1. The E1x24 and T1x24 signals are both used in two ways: as the high-speed clock for the PLL modules and as an internal divide-down to obtain 1x the base frequency. The output of the dividers are DivT1 and DivE1.

Internal clocks ClkIntA and ClkIntB are generated from the following sources:

- Rx line clocks (four ports)
- Tx backplane clock (four ports)
- DivT1
- DivE1

The internal clocks are available to all the Rx and Tx backplane modules and to the Tx line module. Internal clocks are used for a common timing configuration distributed to all ports.

15.4 Rx and Tx Backplane Clock Configuration

The Rx backplane clock can be the input to or output from the IXF3204 framer. When selected as an output, the sources are:

- Rx line clock from the same port
- Internal clocks ClkIntA and ClkIntB
- The output of RxPLL

The Tx backplane clock can be the input to or output from the IXF3204 framer. When selected as an output, the sources are:

- Rx line clock from the same port
- Internal clocks ClkIntA and ClkIntB
- The output of RxPLL

15.5 Tx Line Clock Configuration

The Tx line clock sources are:

- Rx line clock from the same port
- Tx backplane clock from the same port
- Internal clocks ClkIntA and ClkIntB
- The output of TxPLL

15.6 One-Second Clock Configuration

The internal one-second clock signal can be generated from the following sources:

- Rx line clock from any of the ports
- Tx backplane clock from any of the ports
- External clocks T1 x 24 and E1 x 24

The one-second clock signal is used internally to load registers with performance data such as framing, bit errors, and bipolar violations. It is also used to interrupt the internal processor to gather data every second. In addition, the one-second clock signal can be used to enable an interrupt with this same period.

15.7 Reference Clock Configuration

The reference clock is an output to a dedicated ball. The source is the Rx line clock from any of the ports.

15.8 Rx and Tx Backplane Frame-Pulse Configurations

The Rx backplane frame pulse can be an input to or output from the IXF3204 framer. When selected as an output, the sources are:

- Rx line frame pulse from the same port
- Internal free-running generator using the Rx backplane clock

The Tx backplane frame pulse can be an input to or output from the device. When selected as an output, the sources are:

- Rx line frame pulse from the same port
- Internal free-running generator using the Tx Backplane Clock

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15.9 Tx Line Frame Pulse Configurations

The Tx line frame sources are:

- Rx line frame pulse from the same port
- Internal free-running generator using the Tx line clock
- Tx backplane pulse from the same port

15.10 Tx Line Multiframe Pulse Configurations

The Tx line multiframe sources are:

- Rx line multi-frame pulse from the same port
- Internal free-running generator using the Tx line clock
- Tx backplane multi-frame pulse from the same port

15.11 Rx and Tx Backplane Multiframe Pulse Configurations

The Rx backplane multiframe pulse is an output and is generated from the Rx line multiframe.

The Tx backplane multiframe pulse is an input from an external device.

15.12 Backplane and Transmit Line Clock Source Selection

This section describes the options for selecting the clock source for the backplane and transmit line sides, with examples of how clock source selection can take place.

Figure 28 shows possible clock selections for backplane and transmit lines.

Figure 28. Clock Source Selections for Backplane and Transmit Lines

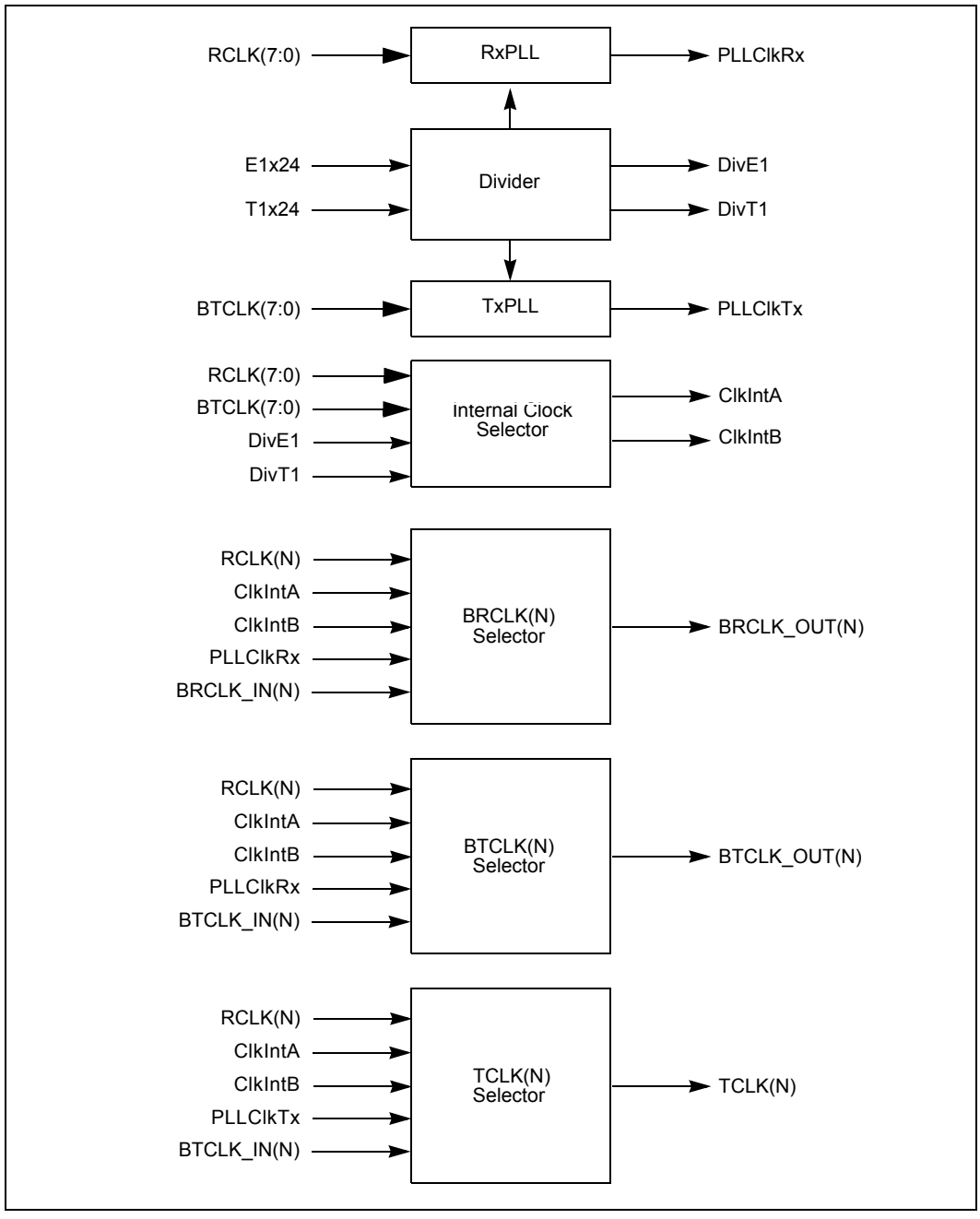

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Figure 29 shows the result when an RCLK source drives all clocks of a port (both backplane and transmit line). In this example, the master timing reference comes from a line-side RCLK.

Figure 29. Clocks Driven from RCLK for Port N Configuration

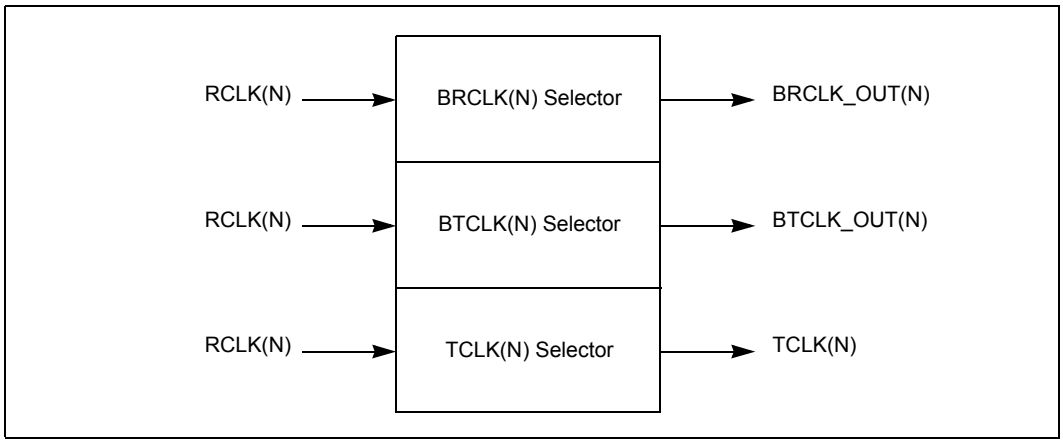


Figure 30 shows the result when TCLK is generated from BTCLK, which along with BRCLK, comes from an external source. In this example, the master timing source for a port is provided at the backplane balls by an external device.

Figure 30. Clocks Driven from BRCLK and BTCLK for Port N Configuration

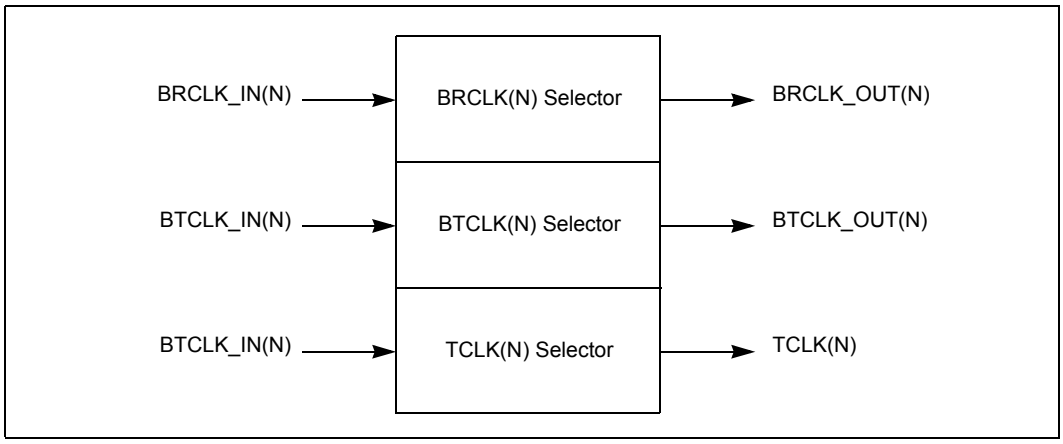


Figure 31 shows the result when all clocks are generated from ClkIntA. In this example, a local T1 x 24 clock is the master timing reference. The T1 x 24 clock frequency can be M x T1 frequency, where M = 1, 8, 16, or 24.

Figure 31. All Clocks Generated from ClkIntA with T1 x 24 Timing Reference

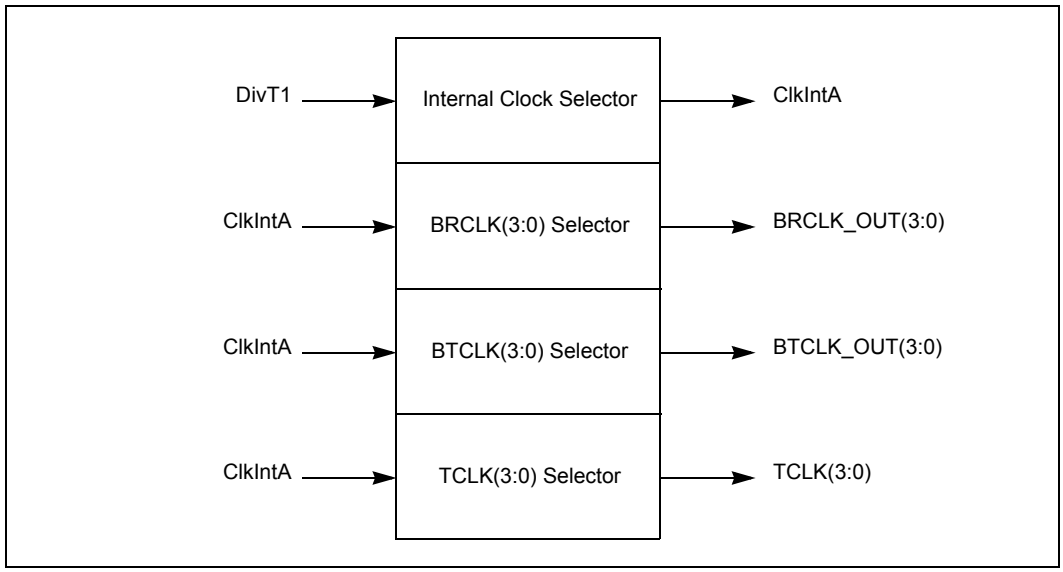
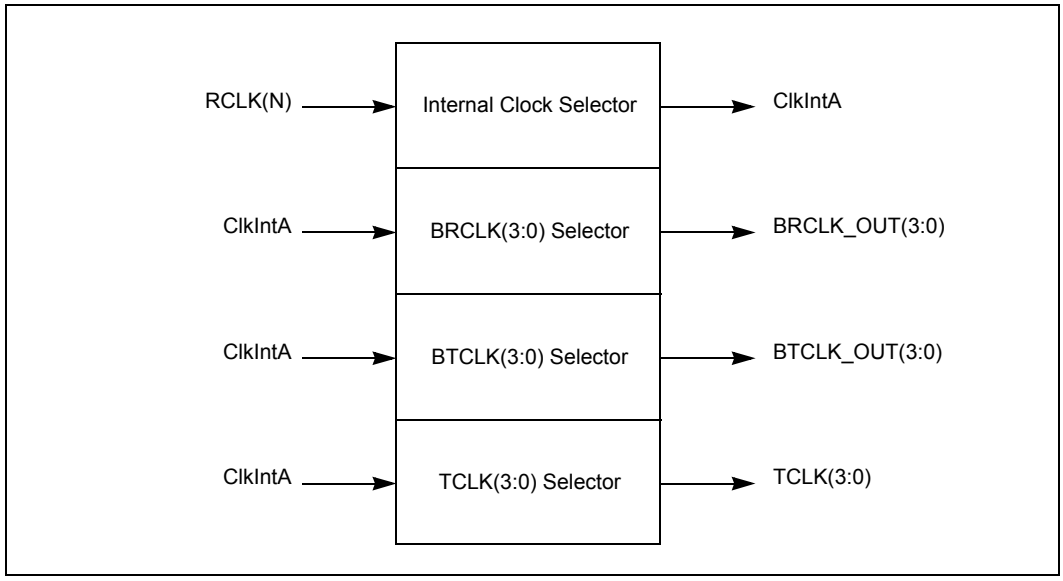


Figure 32 shows the result when a common clock source configures all ports. In this example, the line clock [RCLK(N)] is from port N. All clocks are generated from ClkIntA, and one receive line clock [RCLK(N)] is the master timing reference.

Figure 32. Common Clock Configures All Ports



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16.0 Loopbacks

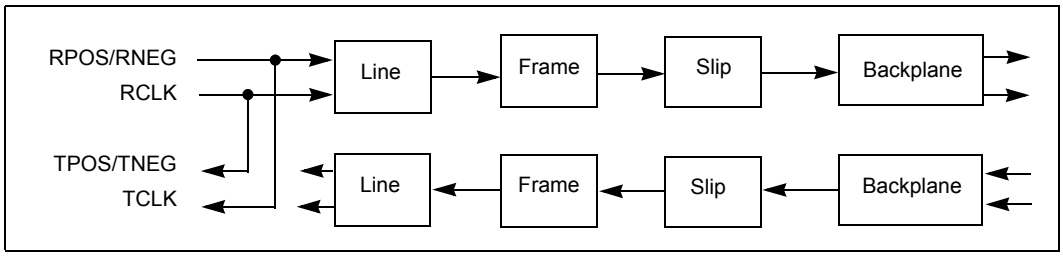
This chapter discusses the following IXF3204 framer loopback topics:

- Section 16.1, “Line Loopback”
- Section 16.2, “Payload Loopback”
- Section 16.3, “Time Slot Loopback”
- Section 16.4, “Digital Loopback”
- Section 16.5, “Dual Loopbacks”
- Section 16.6, “Loopback Priorities”

16.1 Line Loopback

Figure 33 shows a line loopback (LLB) operation, which is performed by returning the data and clock from the receive line balls to the transmit line balls. No processing is done to the data. The LLB behaves like a wire between Rx and Tx line ports. In addition to looping back, the data and timing information go to the Rx path.

Figure 33. Line Loopback



Note: The IXF3204 supports automatic line loopback generation upon detecting specific codes in T1 streams. For details, see Section 11.3, “Alarm Handling and Consequent Actions”.

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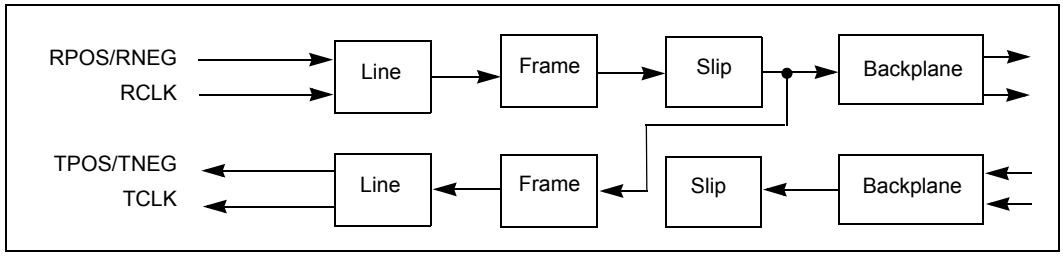
16.2 Payload Loopback

Figure 34 shows a payload loopback (PLB) operation, which is performed by returning the payload data from the receive path to the transmit data balls. In the:

- Rx path, PLB is performed after coding, framing, and storing the payload in the Rx path slip buffers.
- Tx path, PLB is performed after framing and coding the data being looped back.

Any code violations are removed. The frame structure is re-generated and the data transmitted using the user-programmed clock for the Tx line side.

Figure 34. Payload Loopback



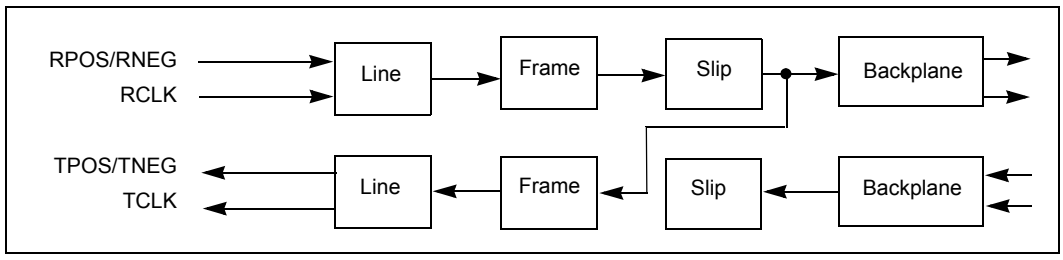
16.3 Time Slot Loopback

Figure 35 shows a time slot loopback (TLB) operation. The TLB is similar to the PLB, but the difference is that the TLB is performed on a per-time slot basis. Any number of time slots can be selected. The TLB is performed by returning the data from the receive path to the transmit data balls. In the:

- Rx path, TLB is performed after coding, framing, and storing the payload in the Rx path slip buffers.
- Tx path, TLB is performed after framing and coding the data being looped back.

Any code violations are removed. The frame structure is re-generated and the data transmitted using the user-programmed clock for the Tx line side. The user can select any number of time slots to be looped back.

Figure 35. Time Slot Loopback



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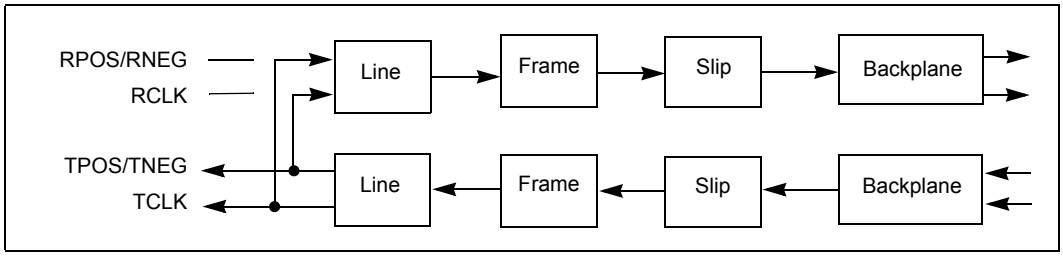
16.4 Digital Loopback

Figure 36 shows a digital loopback (DLB) operation, which is performed by returning the data and clock going to the Tx line balls to the Rx line inputs.

Note: For DLB to work properly, the clock source for the Tx line path must be other than the Rx line clock of the same port.

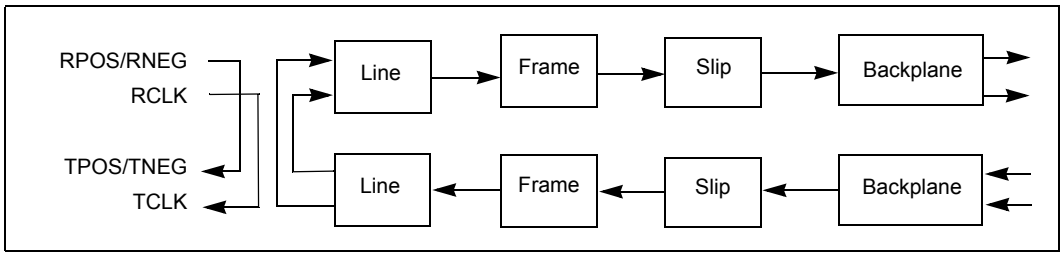
Figure 36. Digital Loopback



16.5 Dual Loopbacks

Figure 37 shows how dual loopbacks (a digital loopback and a line loopback) can be performed at the same time.

Figure 37. Dual Loopbacks



16.6 Loopback Priorities

Loopback priorities are as follows:

- LLB and DLB can be set at the same time.
- LLB has priority over PLB and TLB.
- DLB has priority over PLB and TLB.
- PLB has priority over TLB.

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17.0 Bit Error Rate Tester

This chapter discusses the following Bit Error Rate Tester (BERT) topics:

17.1 BERT Description

The Bit Error Rate Tester (BERT) module can be used to test either all T1/J1/E1 ports or only sections of them. The BERT circuitry provides on-chip functions for testing the quality of links. Up to eight simultaneous tests can be done on multiple time slots and ports. The IXF3204 framer provides generation and analysis capabilities that can be used with either repetitive or pseudo-random bit sequences (PRBS). Multiple BERT modules are available and they can be used in any time slot of any port.

The BERT module has eight programmable pattern generators and eight analyzers that support pseudo-random and repetitive sequences of up to 32 bits. The user must program the time slot associated with the selected BERT module. Each generator or analyzer can be associated with one or more time slots in any one port.

- Each of the eight generators uses PRBS and has a Digital Milliwatt (DmW) generator and a DRS pattern generator.
- Each of the eight analyzers has a programmable threshold to declare in-sync and out-of-sync states.

The IXF3204 framer provides bit error counters and total bit counters to calculate bit error rates. In addition, the IXF3204 framer supports the detection of all zeroes or all ones.

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17.2 BERT Analyzer

As Figure 38 shows, to use any of the BERT analyzers the sequence is the following:

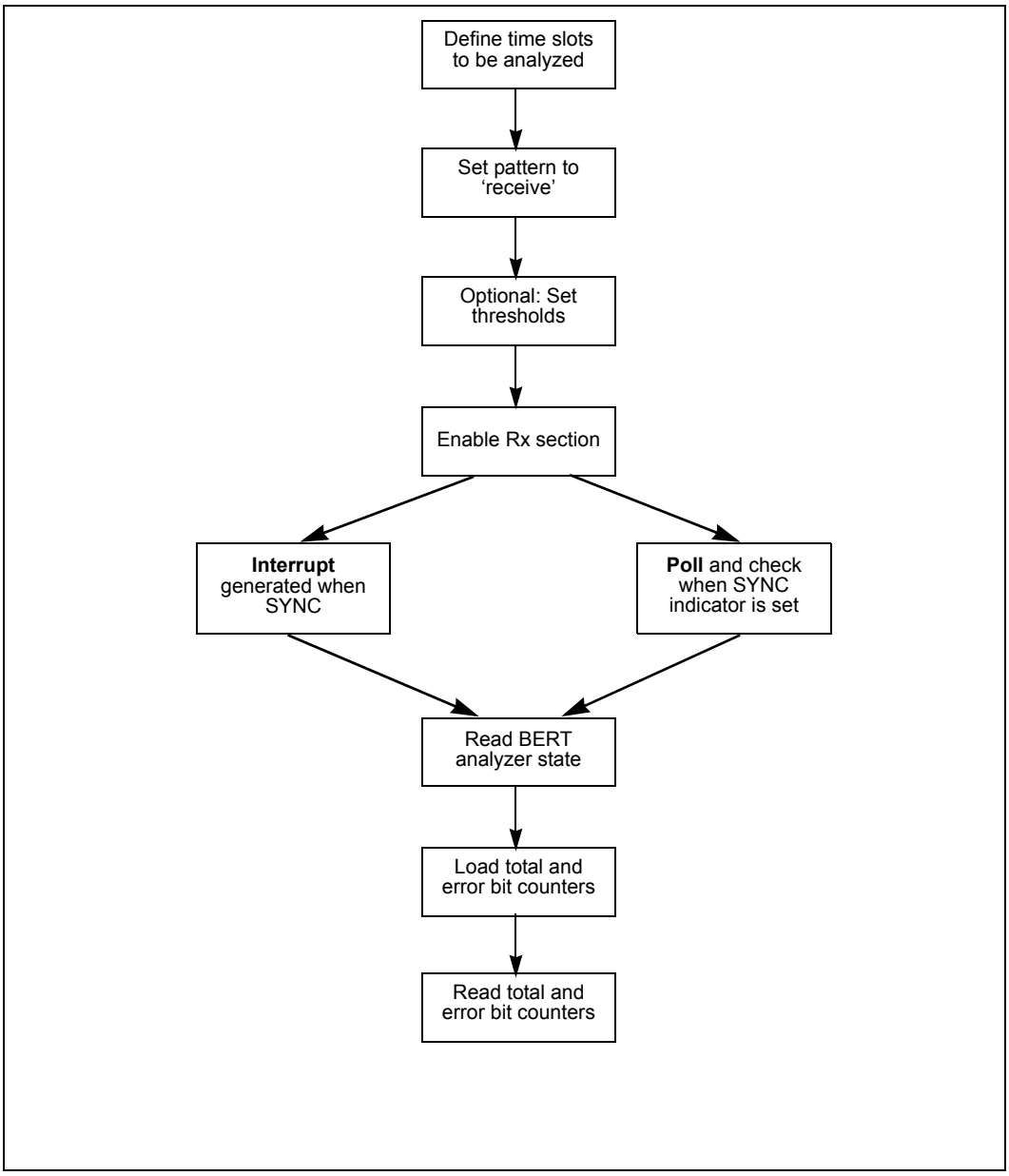
1. Define (that is, map) the time slots to be analyzed.
2. To configure BERT for the 'receive' pattern, do the following:
   a. Associate the selected time slots with the corresponding BERT analyzer 0 to 7. (To select only certain bits of each time slot, a mask can be used.)
   b. Program the 'receive' pattern in the selected BERT module by setting the type, length, invert, and so on.
3. If a change in thresholds is required, set the new thresholds to declare both sync and out-of-sync. The default values are as follows:
   a. If 64 consecutive bits match the expected pattern, a synchronization is declared.
   b. If there are ten or more errors in a window of 100 bits, an out-of-sync is forced.
4. Enable reception for the selected BERT analyzer, after which the BERT analyzer generates indicators and interrupts (if the latter are enabled by the user) and status bits to convey the state (either synchronized, not synchronized, or receiving errors).
5. The host processor can operate in either an interrupt mode or a polling mode. If the host processor operates in an:
   a. Interrupt mode, then once the BERT analyzer generates an interrupt, the host processor must perform the last two steps.
   b. Polling mode, the host processor must keep polling the state of the indicator bits until synchronization is detected and then perform the last two steps.
6. The IXF3204 framer reads the BERT analyzer state.
7. The user can then check the error rate by loading and then reading the total-bit and error-bit counters.

Note:

- The maximum count of the total bit counter and the error-bit counter is 2^{24}, so the host processor must read them faster than that to avoid overflow of the counters. Assuming the highest rate (2.048 Mbps), then after achieving synchronization overflow must be reached in approximately 8 seconds. Intel suggests that the host processor read these counters every second.
- As an option, the IXF3204 framer can be programmed to load the counters automatically every second. After the counters are loaded, the counters must be read-only.
- As another option, as commanded by the host processor, the counters can be loaded with the current values by setting the IXF3204 framer LOADC bit. After that, the values are ready in the host processor-accessible total count and error bit counters. The IXF3204 framer internal counters are re-started when the LOADC bit is set.
- The programming of time slots is done in a region of memory different from the BERT region.

For details on BERT analyzer registers, see the memory map document for the IXF3204 framer.

Figure 38. BERT Analyzer



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17.3 BERT Generator

As Figure 39 shows, to use any of the BERT generators the sequence to follow is:

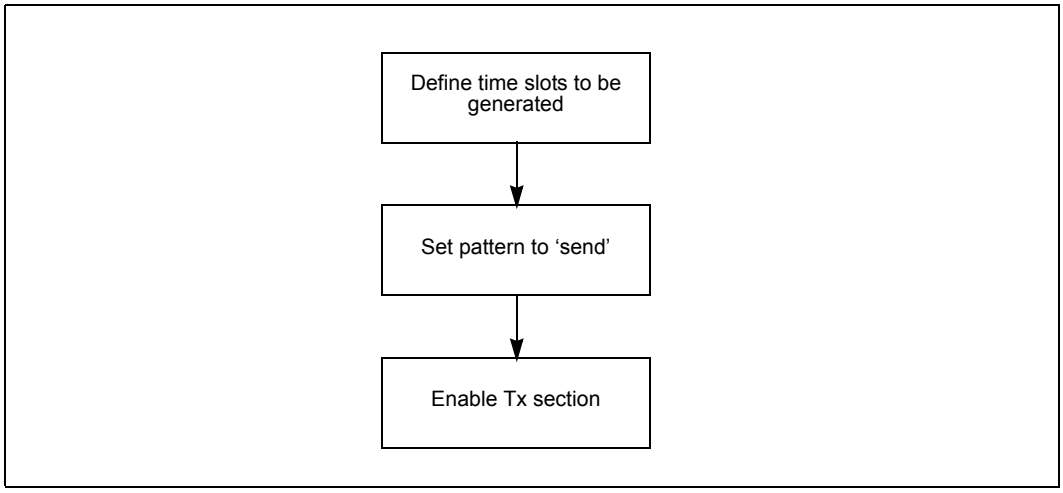
1. Define (that is, map) the time slots to be generated.
2. To configure BERT for the ‘send’ pattern, do the following:
   a. Associate the selected time slots with the selected BERT generator. (To select only certain bits of each time slot, a mask can be used.)
   b. Program the ‘send’ pattern in the selected BERT module by setting the type, length, invert, and so on.
3. Enable transmission for the selected BERT generator, after which the BERT generator sends the information.

To use any of the fixed generators that are DmW or DRS, do the following:

1. Associate the selected time slots with the selected BERT generator. The pattern is sent to the whole time slot, as masking bits is allowed for neither DmW nor DRS codes.
2. Program and enable the generator to output A-law or Mu-law codes.

Note: The programming of time slots is done in a region of memory different from the BERT region. For details on BERT generator registers, see the memory map document for the IXF3204 framer.

Figure 39. BERT Generator



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17.4 BERT Patterns Supported

Table 44 lists the registers that must be programmed to define a BERT pattern.

Table 44. Supported Patterns

Register Name	Register Width (Bits)	Description
CTR	3:0	**Control Register.** Used to define PRBS or QRSS patterns or if the pattern is inverted in the Rx or Tx direction. Bit 3 (INV Tx) • 0 = No inversion of pattern of Tx data output from BERT generator • 1 = Inversion of pattern of Tx data output from BERT generator Bit 2 (INV Rx) • 0 = No inversion of pattern of Rx data input to BERT analyzer • 1 = Inversion of pattern of Rx data input to BERT analyzer Bit 1 (Pseudo-Random Bit Sequence) • 0 = PRBS pattern not enabled • 1 = PRBS pattern enabled Bit 0 (Quasi-Random Sequence Signal) • 0 = QRSS pattern not enabled • 1 = QRSS pattern enabled
PTR	4:0	**Pattern TAP Register.** This field is used to indicate the test-access port (TAP) for a BERT pattern. This field is used only with PRBS. • 00h is for repetitive use. • 01h to 1Fh indicates the bit position where the TAP is located, and 0 indicates the TAP is located in the first flip-flop.
PLR	4:0	**Pattern Length Register.** This field is used to select the length of the BERT pattern, which can be from 1 to 32 bits. • 00h indicates the pattern length is 1 bit. • 1Fh indicates the pattern length is 32 bits.
PS(3:0)	7:0	**Pattern Sequence 3:0.** Each of the four 8-bit Pattern Sequence registers is used to configure a repetitive BERT pattern.

Table 45 lists the possible patterns that can be selected for a BERT, using the settings programmed for the registers listed in Table 44.

Table 45. BERT Pattern Selection (Sheet 1 of 2)

Number	Pattern	CTR (Hex)	PTR (Hex)	PLR (Hex)	PS3 (Hex)	PS2 (Hex)	PS1 (Hex)	PS0 (Hex)
00	2^3-1	02	00	02	FF	FF	FF	FF
01	2^4-1	02	00	03	FF	FF	FF	FF
02	2^5-1	02	01	04	FF	FF	FF	FF
03	2^6-1	02	04	05	FF	FF	FF	FF

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Table 45. BERT Pattern Selection (Sheet 2 of 2)

Number	Pattern	CTR (Hex)	PTR (Hex)	PLR (Hex)	PS3 (Hex)	PS2 (Hex)	PS1 (Hex)	PS0 (Hex)
04	2^7-1	02	00	06	FF	FF	FF	FF
05	2^7-1 (T1 LB Activate)	02	03	06	FF	FF	FF	FF
06	2^7-1 (T1 LB Deactivate)	0E	03	06	FF	FF	FF	FF
07	2^9-1	02	04	08	FF	FF	FF	FF
08	2^{10}-1	02	02	09	FF	FF	FF	FF
09	2^{11}-1	02	08	0A	FF	FF	FF	FF
0A	2^{15}-1 (Not Inverted)	02	0D	0E	FF	FF	FF	FF
0B	2^{15}-1 (ITU O.151)	0E	0D	0E	FF	FF	FF	FF
0C	2^{17}-1	02	02	10	FF	FF	FF	FF
0D	2^{18}-1	02	06	11	FF	FF	FF	FF
0E	2^{20}-1 (ITU O.153)	02	02	13	FF	FF	FF	FF
0F	2^{20}-1 (ITU O.151 QRSS)	03	10	13	FF	FF	FF	FF
10	2^{20}-1	02	10	13	FF	FF	FF	FF
11	2^{21}-1	02	01	14	FF	FF	FF	FF
12	2^{22}-1	02	00	15	FF	FF	FF	FF
13	2^{23}-1	02	11	16	FF	FF	FF	FF
14	2^{25}-1	02	02	18	FF	FF	FF	FF
15	2^{28}-1	02	02	1B	FF	FF	FF	FF
16	2^{29}-1	02	01	1C	FF	FF	FF	FF
17	2^{31}-1	02	02	1E	FF	FF	FF	FF
18	All Ones	00	00	00	FF	FF	FF	FF
19	All Zeroes	00	00	00	FF	FF	FF	FE
1A	Alternating (101010...)	00	00	01	FF	FF	FF	FE
1B	Double alternating (0011...)	00	00	03	FF	FF	FF	FC
1C	D4 Line Loopback Deactivated (1:3)	00	00	02	FF	FF	FF	FC
1D	1:4	00	00	03	FF	FF	FF	F4
1E	D4 Line Loopback Activated (1:5)	00	00	04	FF	FF	FF	F0
1F	1:7	00	00	06	FF	FF	FF	81
20	1:8	00	00	07	FF	FF	FF	40
21	1:16	00	00	0F	FF	FF	40	00
22	3:24	00	00	17	FF	44	00	04
23	User Defined	User	00	User	User	User	User	User

18.0 High-Level Data Link Controller

This chapter discusses the following topics concerning the high-level data link control (HDLC):

18.1 HDLC Features

- Twenty-four HDLC modules available. In E1 mode only, if the user must report Sa/Si bits, then the IXF3204 framer must use Rx HDLC modules 16 to 23 to perform this function. In this case, only 16 HDLC controllers (HDLC 0 to 15) are left available to the user.
- Flexible HDLC module assignments. Each HDLC module can be assigned to any port in any combination of time slot of the same port.
- Subrate support, using a mask to define which bits to use
- Support for all T1, J1, and E1 frame formats
- Two 128-byte FIFOs per HDLC module, one for Rx and the other for Tx
- Storage of up to four messages in each FIFO in either Rx or Tx direction
- Provision of status information for each message and FIFOs
- Detection/generation of start/end flags for HDLC link messages
- Detection/generation of Frame Check Sequence (FCS) for HDLC link messages
- Zero stuffing/destuffing for HDLC link messages
- Detection of short messages (less than 2 bytes)
- Both transmission and detection of abort character
- LAPB, LAPD, LAPV5, or transparent operation modes
- Address-matching and message-filtering support
- Enable/disable control for Frame Check Sequence (FCS) checking/generation
- Provision of byte alignment in transparent mode
- Abortion of messages above specified Maximum Frame Length

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18.2 HDLC Functional Description

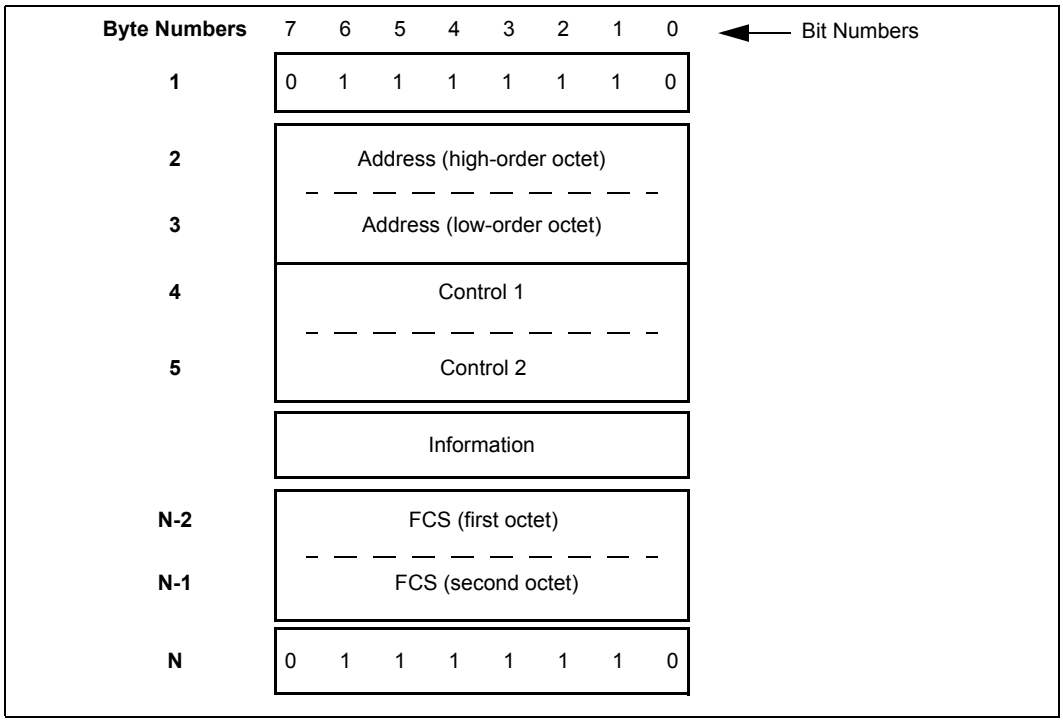
This section describes the following topics concerning HDLC functionality:

- Section 18.2.1, “HDLC Protocols”
- Section 18.2.2, “HDLC Field Descriptions - LAPB, LAPD, and LAPV5”
- Section 18.2.3, “HDLC Address Field Format - LAPD and LAPV5”
- Section 18.2.4, “HDLC Message Processing and Detection”
- Section 18.2.5, “HDLC Address Matching”
- Section 18.2.6, “HDLC Transparent Mode Operation”

18.2.1 HDLC Protocols

HDLC messages are signals conforming to an HDLC protocol (LAPB, LAPD, or LAPV5, as defined in ITU-T recommendations Q.921 and G.964). The HDLC messages are filtered according to the HDLC message address field. Figure 40 shows the HDLC protocol frame format.

Figure 40. HDLC Protocol Frame Format



All HDLC protocol frames must start and end with a flag sequence consisting of the following:

- One zero
- Six contiguous ones
- Another zero

In some applications, the closing flag can also be the opening flag of the next frame.

18.2.2 HDLC Field Descriptions - LAPB, LAPD, and LAPV5

For each field shown in Figure 40, details are in ITU-T recommendations Q.921 and G.964.

Address field. The address field identifies the entities used in establishing an HDLC link.

- LAPB messages have an address field one byte long (the first address byte).
- LAPD or LAPV5 messages have an address field two bytes long.

For the LAPB and LAPV messages, the address field is discussed in more detail in Section 18.2.3, "HDLC Address Field Format - LAPD and LAPV5".

Control field. The control field identifies the type of frame (which will be either a command or a response).

Information field. The information field (if any) consists of an integer number of bytes.

FCS field. The Frame Check Sequence ('FCS') is a CRC16 checksum of the data between the opening flag and the FCS field.

18.2.3 HDLC Address Field Format - LAPD and LAPV5

As referenced in Section 18.2.2, "HDLC Field Descriptions - LAPB, LAPD, and LAPV5", this section further describes the format of the HDLC address field for LAPD and LAPV5 messages.

Figure 41 shows the address field format for LAPD messages.

Figure 41. Address Field Format for LAPD Messages

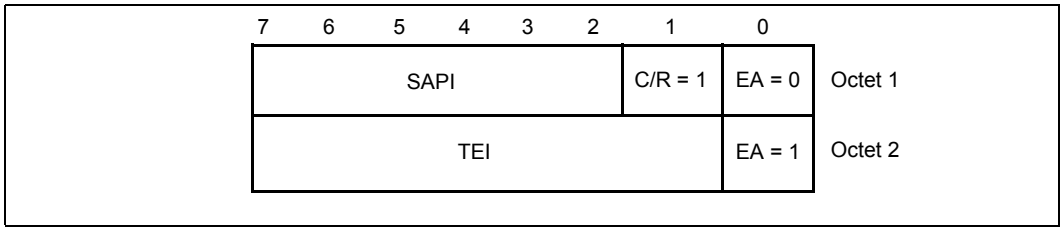
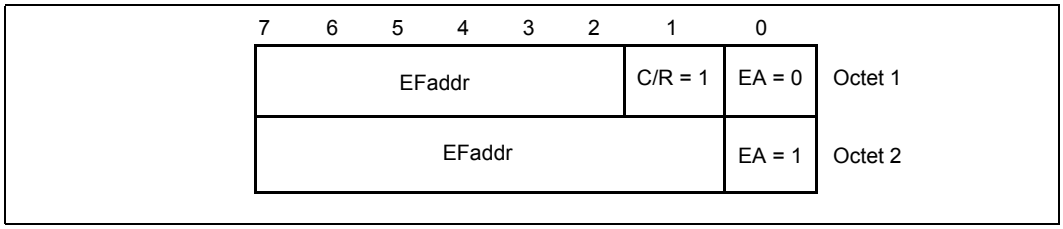


Figure 42 shows the address field format for LAPV5 messages.

Figure 42. Address Field Format for a LAPV5 Message



SAPI field. For LAPD messages only, the Service Access Point Identifier ('SAPI') field is used to address a point being serviced with data-link procedures.

C/R bit. For both LAPD and LAPV5 messages, the Command/Response ('C/R') bit indicates if a message is a command or a response.

EA bits. For both LAPD and LAPV5 messages, there is a double-octet Extend Address bit (EA bit). For both LAPD and LAPV messages, the EA bits must be set as follows:

- EA bit in octet 1 (bit 0) set to '0'.
- EA bit in octet 2 (bit 0) set to '1' (indicating this second field octet is the final octet of the address field)

TEI field. For LAPD messages only, the Terminal Endpoint Identifier ('TEI') field is used to address terminal equipment being serviced with data-link procedures.

EFaddr field. For LAPV5 messages only, the Envelope Field Address (EFaddr) field can take values from 0 to 8191 and serves the same purpose as the SAPI and TEI fields.

18.2.4 HDLC Message Processing and Detection

Stuffing / Destuffing.

- Stuffing occurs on the receive side of a message. To avoid the situation of detecting opening/closing flags in the information field (described in Section 18.2.2, "HDLC Field Descriptions - LAPB, LAPD, and LAPV5"), zero stuffing is performed by inserting a zero when a sequence of 5 consecutive ones is found in the fields between the opening and closing flag.
- Destuffing occurs on the transmit side of a message. Destuffing is performed by removing any zero found after five consecutive ones in the fields between the opening and closing flag of a frame.

Message detection. A message is detected by the following main events:

1. Opening flag detection: A new HDLC frame is detected when a flag is received and sequences that are different from either flags or ones (that is, information bits) are being received.
2. Destuffing: While the HDLC module is receiving information bits, it performs zero destuffing. Received information bytes are stored in a 128-byte FIFO, excluding flags or interframe sequences.
3. Closing flag detection: A closing flag is detected when information bits are being received and next a flag sequence is detected.
4. CRC checking: When a closing flag is detected, the last two bytes before the closing flag are considered the FCS field (described in Section 18.2.2, "HDLC Field Descriptions - LAPB, LAPD, and LAPV5"). This value is compared to the internally calculated value for a cyclic redundancy check.

Updating process. After a closing flag is detected, status signals are updated for the following:

- If an error was received
- The message length
- If an abnormal receive termination took place

18.2.5 HDLC Address Matching

The HDLC module can perform address matching. Four address bytes are used to compare the received message address with the expected one:

- Address-low 1 (1-1)
- Address-low 2 (1-2)
- Address-high 1 (2-1)
- Address-high 2 (2-2)

Address matching can be enabled/disabled in any operation mode. When the operation mode is:

- LAPB, address matching uses only address-high 1 (2-1) and address-high 2 (2-2).
- LAPD, all four address bytes are used such that any combination of the address-high and address-low bytes (1-1, 2-2, 1-2, and 2-1) is received.
- LAPV5 checks the address bytes for the following values:
  - In the first address byte, the C/R bit must equal ‘0’ and the EA bit must equal ‘0’.
  - In the second address byte, the EA bit must be equal to ‘1’.

  For LAPV5, if the C/R and EA bit values match the expected value, then the entire message is received and processed. Otherwise, if one or more of the values do not match, then the entire message is discarded.

If the operation mode is configured to be:

- LAPB and the address byte received is FFh, then the address is considered to be a broadcast address and the message is considered to be valid.
- LAPD and the TEI sub-field of the address field is FFh, then the address is considered to be a broadcast address and the message is considered to be valid.
- LAPV5, there is no support of broadcast addresses.

18.2.6 HDLC Transparent Mode Operation

If an HDLC module is configured for a transparent operation mode, then no flag checking, no destuffing, and no FCS checking are performed (that is, all bytes are sent to the Data FIFO). Byte alignment can be provided in this mode such that the data in the time slot is stored aligned in the Data FIFO.

- For the transmission side, the bytes stored in the HDLC Tx FIFO are sent aligned to the time slot bits. For the alignment to occur, the whole time slot must be used to carry the data. The host processor can store up to four consecutive messages, provided the total length is not more than 128 bytes.
- For the receive side, up to four messages can be stored before the host processor retrieves them. As soon as one message is received, an indication is generated to the host processor. Reception can continue even if the host processor has not read the first message. A FIFO of up to four status messages is associated with the Data FIFO.

  Once the host processor reads the first message, it informs the HDLC module so the next status can be presented to the host processor. As an example, messages of size 6, 16, 32, and 54 bytes can be stored. However, the total number of bytes must not exceed 128 bytes. The host processor must read the messages before an overflow can occur on either the 128-byte Data FIFO or the status FIFO (which has a limit of 4 status messages).

Abortion of an HDLC message occurs on the:

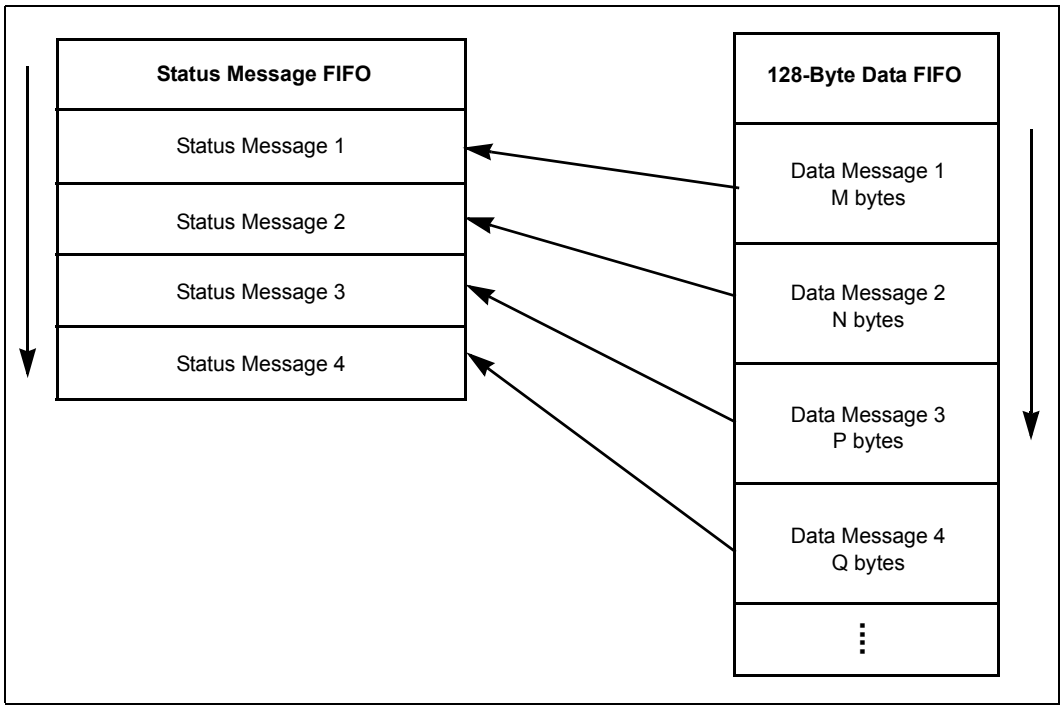
- Reception side for one of several reasons:
  - A sequence of seven or more consecutive ones is received in the information field
  - There is either a FIFO overflow or underflow.
  - The maximum message length parameter is reached.
- Transmit side only if instructed by the user.

18.3 HDLC Message Reception Process

Figure 43 shows the HDLC message reception process. Each of the HDLC engines has both a Status Message FIFO (consisting of 4 status messages) and a 128-byte Data FIFO. The Status Message FIFO stores one of two types of status indicators:

- End Of Message (EOM), which signals the end of a message
- 'Half', which indicates reception of 64 byes (half of the data FIFO)

Figure 43. HDLC Message Reception Process



If — before the host processor reads a previously stored message — it receives a new message, then the next location of the Status Message FIFO stores the status of the new message. In this way, the Status Message FIFO can receive four back-to-back messages as long as the total size of the data message is below 128 bytes.

The Status Message FIFO generates a 'half' indication when it receives the first 64 bytes of a message but the message has not completed. If the message has more than 64 bytes, then one or more status indicators are 'half' and the last status indicator is EOM.

Both the Status Message FIFO and the Data FIFO wrap around once each reaches its limit (four messages for the Status Message FIFO and 128 bytes of data for the Data FIFO).

The HDLC module issues an indication to request service on each 'half' or 'EOM' status indicator, and each indication generates an interrupt if an interrupt is enabled. The host processor can be programmed to work either according to interrupt-based mechanisms or according to polling based on message-indication bits. Once a message indication is set (or an interrupt is generated), the host processor must service that indication by checking the HDLC component that generated it.

18.3.1 Steps to Configure the HDLC Receive Path

After all modules are configured for the proper format and operation conditions, the configuration of HDLC-specific receive functions occurs as follows:

1. Enable the HDLC module. (In the E1 mode only, not all HDLC modules are available at all times.)
   - If the user does not need to report Rx Sa/Si bits, then all HDLC modules (0 to 23) are available for use.
   - If the user does need to report Rx Sa/Si bits, then the IXF3204 framer uses Rx HDLC modules 16 to 23 to report the bits. In this case, the user has available only the HDLC modules 0 to 15.
2. Configure the module for either LAPB, LAPD, LAPV5, or transparent receive modes.
3. If the HDLC module is configured for LAPV5, then addresses do not need to be programmed to match other addresses. However, if the HDLC module is configured for either LAPB or LAPD, program the addresses to match the following:
   - Address-high 1
   - Address-low 1
   - Address-high 2
   - Address-low 2
4. Assign the time slot carrying data to be mapped to the selected HDLC module.
   - Any number of time slots of the same port can be assigned to the selected HDLC module.
   - However, time slots from different ports are not allowed to be mapped in the same HDLC module.
5. Define the mask to use in every selected time slot. A mask can be used so that subrate streams can be supported. Any combination of bits is available. Once the mask is selected, it applies to all the time slots in that port.
6. As an option, enable the interrupt generation for events in the selected HDLC. At this point, the HDLC path is configured and messages can be received

18.3.2 Reading an HDLC Message

Figure 44 shows how the HDLC reads a received message, which occurs in the following sequence:

1. When an event related to the reception of the message occurs, one of the HDLC modules generates an indication.
2. If the host processor is operating in:
   a. Interrupt mode, then the indication from the HDLC module propagates as an interrupt.
   b. Polling mode, the host processor detects the indicator bit set. After this step occurs, go to the next step.
3. The host processor must check which of the HDLCs generated the indication (or interrupt) after which, the host processor selects the one that generated the indication.
4. The host processor must read the status register of the corresponding HDLC module. Available status bits include the following:
   — HALF - Indicates when the number of bytes the Rx engine stored in Data FIFO reaches half of 128 bytes (that is, 64 bytes). If the status bit is ‘HALF’, then there is a read of 64 bytes from Data FIFO and go to the last step.
   — EOM - Indicates an end of message is set because the last byte of the message has been received (that is, either a closing flag or an abort flag is detected). If the status bit is ‘EOM’, read the ‘message length register’ and then read the number of bytes from the Data FIFO as specified by the message length register.
   — UNF - Set when an underflow has occurred, which occurs when the host processor performs a read data operation when Data FIFO is empty. If this status is received, clear the HDLC module by setting the bit ‘CLR’ in the GCR register (general control register) and skip steps 5 and 6.
   — OVF - Set when an overflow has occurred, which occurs when either of the two following conditions exist:
      • The 128 bytes of the Data FIFO are full and a new byte is subsequently received.
      • There are already 4 messages stored in the Status Message FIFO and a new status message is subsequently generated. If this status is received, clear the HDLC module by setting the bit ‘CLR’ in the GCR register (general control register) and skip steps 5 and 6.
5. Read the status of the message. Available states include the following:
   — Short message
   — Large message
   — CRC error
   — Valid message
   — Aborted message
   — Non-octet message
6. The host processor completes the process by setting the bit ‘HDone’ by writing 01h to register HCR. This handshake process informs the HDLC receive module that it can re-use the Data FIFO section.

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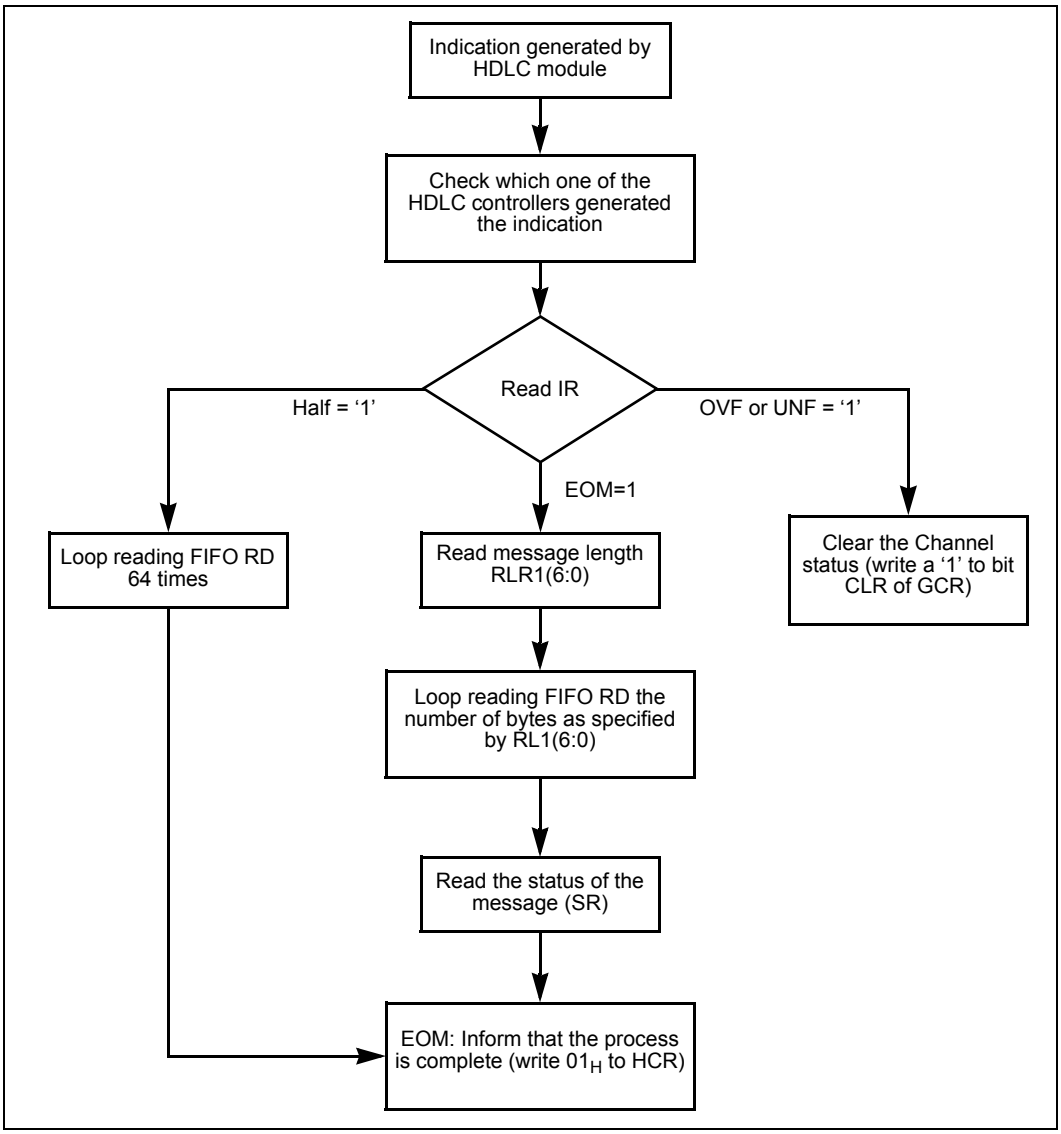
Note: Figure 44 applies to T1, E1, and J1 modes for the following reasons.

- In T1/J1 modes, all HDLC controllers are available for use.
- In the E1 mode, if the user:
  - Does not need to receive Sa/Si bits, all 24 HDLC controllers are available.
  - Does need to use Sa/Si bits, then only 16 HDLC controllers (0 to 15) are available.

For details on the HDLC registers, see the memory map document for the IXF3204 framer.

Figure 44. Receiving an HDLC Message



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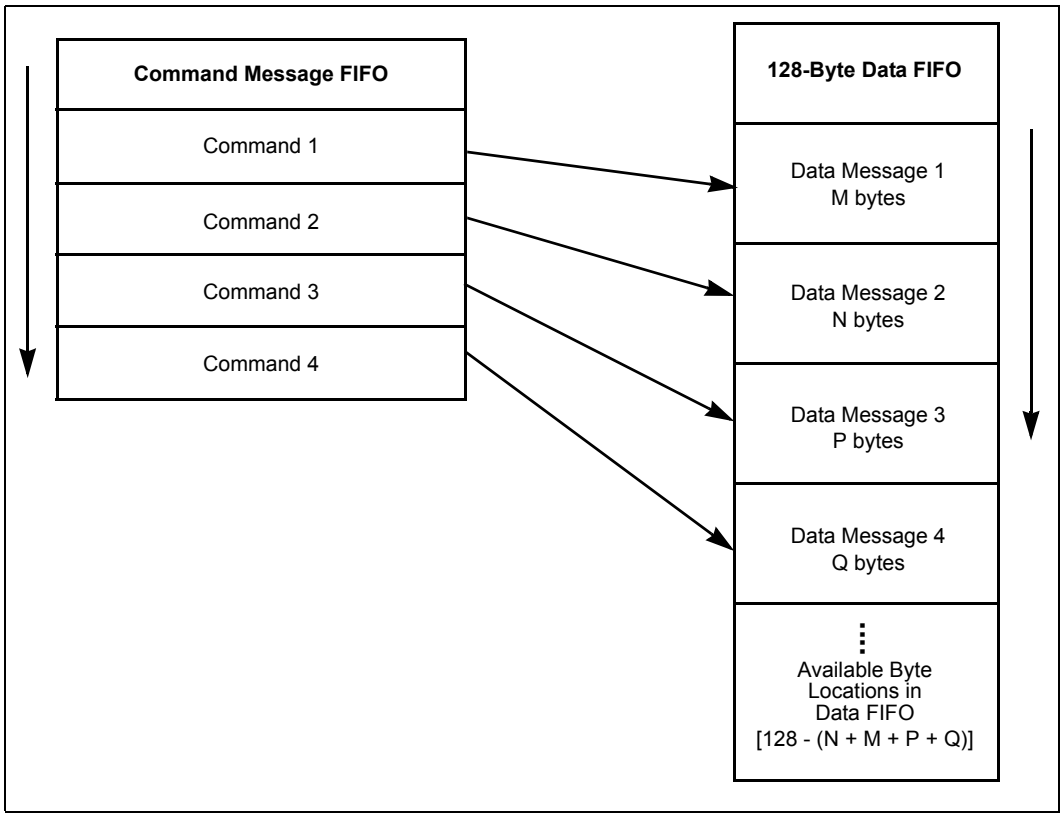
18.4 HDLC Message Transmission Process

Figure 45 shows the HDLC message transmission process. Each of the HDLC engines has both a Command FIFO (consisting of 4 locations) and a 128-byte Data FIFO. The Command FIFO stores one of two types of command indicators:

- End Of Message (EOM), which signals the end of a message
- 'Half', which indicates transmission of 64 byes (half of the data FIFO)

Figure 45. HDLC Message Transmission Process



The Command FIFO can store up to four command indicators, and the Data FIFO can store up to 128 bytes. At any time, the user cannot go over either the limit for the Command FIFO (4 locations) or the limit for the Data FIFO (128 bytes). After space becomes available for both a new command and for data, the next message (or part of it) can be stored in the respective FIFOs.

If the length of the message is:

- Below 64 bytes or equal to 64 bytes, the user must set one 'EOM' command and store the data bytes in the Data FIFO.
- Above 64 bytes, then one or more commands are 'half' (with each transmitting 64 bytes) and the last command is EOM. In this case, the user must set at least one HALF command and one EOM command.

Both the Command FIFO and the Data FIFO wrap around once each reaches its limit.

The HDLC module informs the host processor when there are at least 64 bytes available to accept another message to be transmitted. When there are less than 64 bytes available or if all four of the command locations are being used, then the HDLC module does not issue any indication. In this case, the host processor must wait until both FIFOs indicate they are available for use.

18.4.1 Steps to Configure the HDLC Transmit Path

After all modules are configured for the proper format and operation conditions, the configuration of HDLC-specific transmit functions occurs as follows:

1. Enable and configure an HDLC module.
2. Assign the time slot carrying data to be mapped to the selected HDLC module.
   - — Any number of time slots of the same port can be assigned to the selected HDLC module.
   - — However, time slots from different ports are not allowed to be mapped in the same HDLC module.
3. Define the mask to use in every selected time slot. A mask can be used so that subrate streams can be supported. Any combination of bits is available. Once the mask is selected, it applies to all the time slot in that port.
4. As an option, enable the interrupt generation for events in the selected HDLC.
5. Enable the interrupt of the selected HDLC. At this point, the HDLC path is configured and messages can be transmitted.

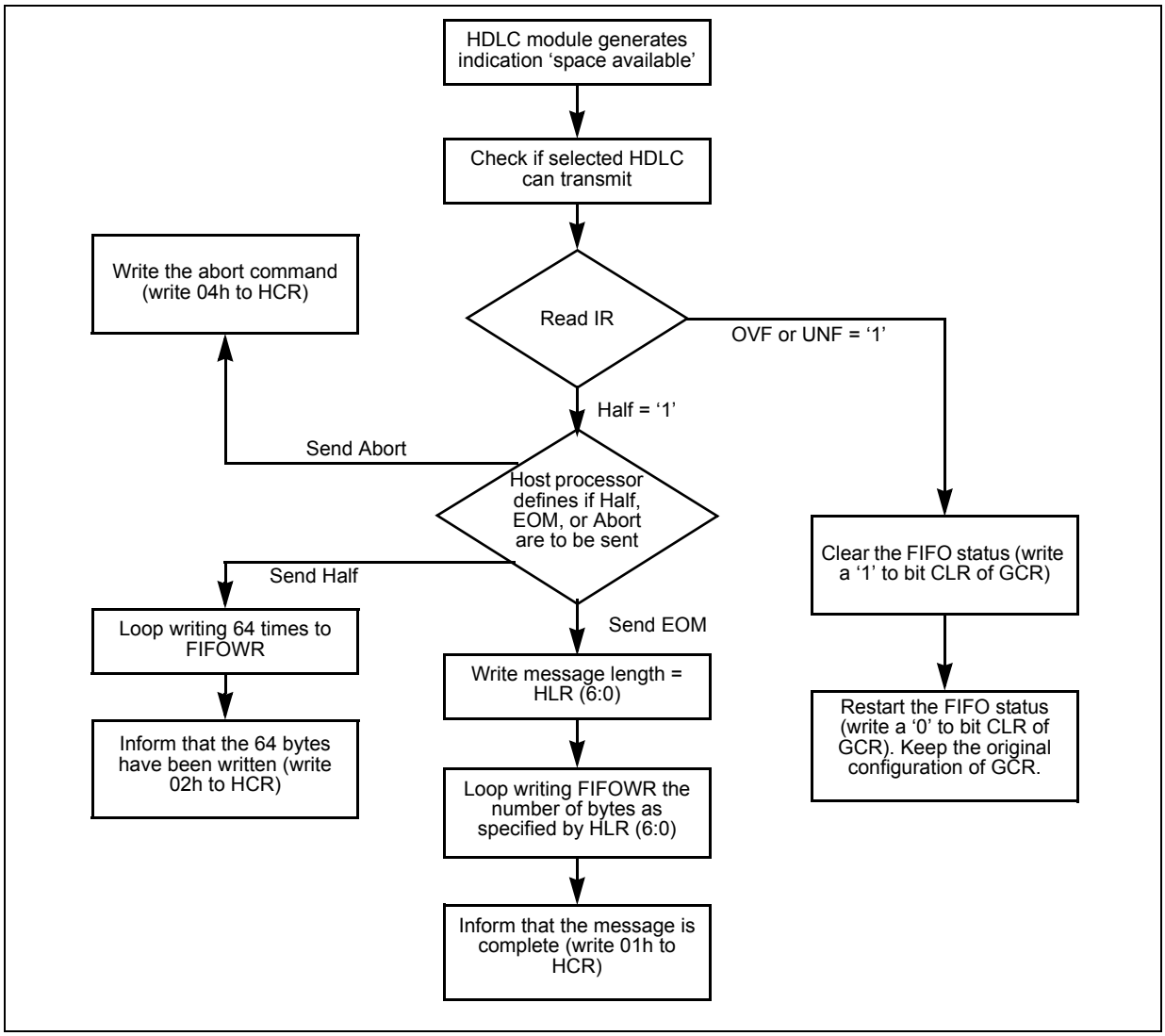
18.4.2 Sending an HDLC Message

Figure 46 shows how the HDLC sends a message, which occurs in the following sequence:

1. The host processor checks that there is space available (at least 64 bytes) to write the HDLC message in preparation for sending it. The HDLC module indicates the availability of space by setting the ‘half’ indicator bit.
2. Once the host processor verifies the availability of space, it can write the message and command the HDLC module to send it. When the message is:
   - — Less than or equal to 64 bytes, the full message is written in the Data FIFO and then the ‘EOM’ command must be written in the command register.
   - — More than 64 bytes, there must be at least one ‘half’ command that indicates that only 64 bytes have been written in the Data FIFO and the last byte of the message has not yet been received
3. The host processor uses:
   - — The command register to set either ‘half’ (that is, 64 bytes) or ‘EOM’ commands.
   - — The indicator register to check if there is space available and if previous commands were executed. Whenever a command is executed, the HDLC module gives an indication to the host processor.

Note: For details on the HDLC registers, see the memory map document for the IXF3204 framer.

Figure 46. Sending an HDLC Message



19.0 Performance Monitoring

The IXF3204 framer monitors performance with specific modules that store data on anomalies, defects, and failures. An internal processor retrieves the data every second and builds the related database.

If data streams are:

- T1, the IXF3204 framer must generate PRM every second. A database is created that contains 33 bins, each containing 15 minutes of data. The T1 performance elements follow the T1.231 standard.
- E1, accumulated results are maintained. The E1 performance elements follow the G821/G826 standard.

This chapter discusses the following performance-monitoring topics:

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19.1 T1 Performance Elements

To create T1 performance elements, the IXF3204 framer firmware must obtain status information from the near-end and far-end parameters.

19.1.1 T1 Near-End Performance Elements

The performance elements for T1 near-end are the following, per ANSI T1.231:

- Line Parameters – Near-end
  - CV-L: Code Violation - Line
  - ES-L: Errored Second - Line
  - SES-L: Severely Errored Second - Line
- Path parameters – Near-end
  - CSS-P: Cascading Style Sheets - Path
  - CV-P: Code Violation - Path
  - ES-P: Errored Second - Path
  - SAS-P: **S**everely Errored Frame / **A**larm Indication Signal **S**econds - **P**ath
  - SES-P: Severely Errored Seconds - Path
  - UAS-P: Unavailable Seconds - Path

Table 46 lists how T1 near-end performance elements must be stored. The 24-hour period starts at time 00:00 and keeps counting until 24 hours have elapsed. The current 24-hour data are then stored in the previous 24-hour data, and the count is initialized again.

Table 46. T1 Near-End Performance Elements Storage

Time Frame	Storage	Bits
Current Day	Current 24-hour period	32
Previous Day	Previous 24-hour period	32
Current 15 minutes	Current 15-minute interval	16
Previous 15 minutes	Previous 15-minute interval	16
31 Recent 15 minutes	31 most-recent 15-minute intervals before previous interval	16

To initialize the database for a specific port, perform the following steps:

1. Clear to ‘0’ the firmware PRM enable bit at address [(D2D0) + N x 5A4h], where N = port number.
2. In the T1 performance database, clear all regions related to port N.
3. Set to ‘1’ the firmware PRM enable bit at address [(D2D0) + N x 5A4h], where N = port number.

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19.1.2 T1 Far-End Performance Elements

The performance elements for T1 far-end are the following, per ANSI T1.231:

- Line Parameters– Far-end
  - ES-LFE: Errored Seconds - Line Far End
- Path Parameters – Far-end
  - CSS-PFE: Cascading Style Sheets - Path Far End
  - CV-PFE: Code Violation - Path Far End
  - ES-PFE: Errored Seconds - Path Far End
  - ESA-PFE: Errored Seconds, Type A - Path Far End
  - ESB-PFE: Errored Seconds, Type B - Path Far End
  - SEFS-PFE: Severely Errored Framing Seconds - Path Far End
  - SES-PFE: Severely Errored Seconds - Path Far End
  - UAS-PFE: Unavailable Seconds - Path Far End

These elements are calculated based on the PRM received. The bins are updated with the internal one-second signal, even if the one-second signal is not synchronized with the PRM received. If there is no PRM at the one-second interval, update the far-end database with all values set to ‘0’.

Table 47 lists how T1 far-end performance elements must be stored.

Table 47. T1 Far-End Performance Elements Storage

Time Frame	Storage	Bits
Current Day	Current 24-hour period	32
Previous Day	Previous 24-hour period	32
Current 15 minutes	Current 15-minute interval	16
Previous 15 minutes	Previous 15-minute interval	16
31 recent 15 minutes	31 most-recent 15-minute intervals before previous interval	16

19.2 E1 Performance Elements

E1 performance elements are designed to follow the G.821/G.826 recommendations for E1. The counters keep the accumulated value. If the maximum value is reached, then the counter keeps this maximum value until the counter is cleared.

19.2.1 E1 Error Ratios

Table 48 lists the E1 near-end and far-end error ratio types and how G.826 parameters can be evaluated either during or at the end of a measurement period 'P', taking into account Unavailable Seconds ('UAS'). The measurement period 'P' is provided by the variable 'Time' described in Table 49, where 'Time' equals the total time since the counter was initialized.

Note: In Table 48, 'c' = count.

Table 48. E1 Near-End and Far-End Error Ratio Types

Error Ratio Type	Description	Counter Length (Bits)	Equation to Evaluate G826 Parameters
ESR	Errored Seconds Ratio	32	ESR = cES / (P - UAS)
SESR	Severely Errored Seconds Ratio	32	SESR = cSES / (P - UAS)
BBER	Background Block Error Ratio	32	BBER = cBBE / [(P - UAS - cSES) x blocks per second]

For both the E1 near end and far end, the error ratio is represented in percent values that are multiplied by 1 x 10^{-6}. For example:

- 100000000 = 100%
- 1000000 = 1%
- 100000 = 0.1%, and so on.

Errored Seconds Ratio (ESR): The ratio of errored seconds (ES) to the total seconds in the available time during a measurement interval.

Severely Errored Seconds Ratio (SESR): The ratio of severely errored seconds (SES) to the total seconds in the available time during a measurement interval.

Background Block Error Ratio (BBER): The ratio of background block errors (BBE) seconds to the total blocks in the available time during a measurement interval. The count of total blocks excludes all blocks during SESs.

Calculation of ES, SES, and BBE is described in Section 19.2.3, "E1 Near-End Performance Elements" and Section 19.2.3, "E1 Near-End Performance Elements".

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19.2.2 E1 Total Time Available and Unavailable

For both the E1 near end and far end, as listed in Table 49 variables are stored in an internal memory database.

Note:

- The AvailR variable is a percentage multiplied by 10^6.
- The granularity for AvailT, Time, and UAS is in seconds.
- The variable ‘Time’ is the same as the measurement period ‘P’ used in the calculation of ESR, SESR, and BBER. To initialize the measurement period and restart the E1 database, set the variable ‘Time’ to ‘0’ by writing 0000h to Address [(568 to 56B) + (N x 54Ah)], where N = the port number.
- For a reliable operation, perform two back-to-back writes to the four bytes of the variable ‘Time’. In this case, the firmware detects the value ‘0’ and re-initializes the whole database.

Table 49. Stored Variables

Variable	Description	Length (Bits)
AvailR	Ratio of available time to unavailable time	32
AvailT	Time since the IXF3204 framer last entered into the available state	32
Time	Total time since the counter was last initialized	32
UAS	Unavailable seconds time	32

Using the ESR, SESR, and BBER values and the variables listed in Table 49, as needed the user can calculate ES, SES, and BBE as follows:

- ES = ESR x (Time - UAS) / 10^6
- SES = SESR x (Time - UAS) / 10^6
- BBE = BBER x [(Time - UAS - SES) x 500)] / 10^6

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19.2.3 E1 Near-End Performance Elements

Anomaly and defect events are used to generate performance elements. As defined in G826, anomalies and defects are used to declare BBE, ES, and SES parameters. This section and Section 19.2.4, "E1 Far-End Performance Elements" discuss the anomalies and defects used to declare the IXF3204 framer E1 near-end and E1 far-end BBE, ES, and SES parameters.

Table 50 lists the E1 near-end anomalies, per the G.826 recommendation.

Table 50. E1 Near-End Anomalies

Anomaly	Description
a1	An errored frame-alignment signal
a2	An errored block (EB) as indicated by an Error Detection Code (EDC)

Table 51 lists the E1 near-end defects, per the G.826 recommendation.

Table 51. E1 Near-End Defects

Defect	Description
d1	Loss of signal
d2	Alarm-indication signal
d3	Loss-of-frame alignment

Declarations are made as follows.

- BBE is declared when there occurs in a block that is not part of an SES either one of the anomalies (a1 or a2).
- ES is declared when during one second there occurs either one of the anomalies (a1 or a2) or one of the defects (d1, d2, or d3).
- SES is declared when during one second there occurs either at least 805 anomalies (a1 or a2) or one of the defects (d1, d2, or d3).

19.2.4 E1 Far-End Performance Elements

Table 52 lists the E1 far-end anomaly and defect as used by the IXF3204 framer.

Table 52. E1 Far-End Anomaly and Defect

Anomaly / Defect	Description
Anomaly - a1	E bit received in '0'
Defect - d1	AIS signal

Declarations are made as follows.

- BBE is declared when there occurs in a block that is not part of an SES one anomaly (a1).
- ES is declared when during one second there occurs at least one anomaly (a1) or one defect (d1).
- SES is declared when during one second there occurs either at least 805 anomalies (a1) or one defect (d1).

19.3 Generic Performance Elements

Table 53 lists the generic performance elements that apply to both T1 and E1. These elements are updated every second and are 16 bits long.

Table 53. Generic Performances Elements - T1 and E1

Element	Description	Length (Bits)
COFA	Increments by one if COFA occurs during the one-second interval	16
CRC	The number of CRC errors that occur in a one-second interval	16
CSR	Increments by one if a controlled slip in the Rx slip buffer (CSR) occurs during the one-second interval	16
CST	Increments by one if a controlled slip in the Tx slip buffer (CST) occurs during the one-second interval	16
FE	The number of F-Bit errors that occur in a one-second interval	16
LCV	The number of BPVs that occur in a one-second interval	16
OOF	Increments by one if OOF occurs during the one-second interval	16

19.4 Performance Elements Database

The host processor can access the performance elements database, a database created to store in memory the performance elements for both near-end and far-end parameters. For a description of the specific memory locations used to access the defined parameters, see the memory map document for the IXF3204 framer.

19.5 Managing Performance Report Messages

The IXF3204 framer supports automatic management of performance report messages, per ANSI T1.403. As briefly described in Section 19.5.1, "PRM Reception" and Section 19.5.2, "PRM Transmission", an internal firmware routine manages the reception and transmission of PRMs. (For details, see the memory map document for the IXF3204 framer.)

19.5.1 PRM Reception

For PRM reception, the firmware performs the following steps:

1. Every second, the firmware checks for a PRM by checking registers in the Receive FDL PRM section of the memory map. (For register details, see the memory map document for the IXF3204 framer.)
2. If a received PRM:
   a. Is invalid, the firmware discards it. [An invalid received PRM has either (1) a CRC error or (2) it is not within octet boundaries as indicated by the PRM message status registers.]
   b. Is valid, the firmware reads and processes the PRM values to generate far-end performance elements.

19.5.2 PRM Transmission

For PRM transmission, the firmware performs the following steps:

1. Every second, the firmware builds and transmits a new PRM.
2. The firmware writes the new PRM into registers in the Transmit FDL PRM section of the memory map. (For register details, see the memory map document for the IXF3204 framer.)
3. The firmware commands the Transmit FDL section to send the PRM message.

20.0 Host Processor Interface

20.1 Host Processor Configuration Modes

The host processor interface consists of both a non-multiplexed 16-bit address bus and an 8-bit data bus. It supports asynchronous modes for both the Motorola MC68302 and MPC860 processors and the Intel® I486™ processor.

Table 54 lists the possible configuration modes and how to select the configuration mode with the IXF3204 framer I/M# and MTYPE balls.

Note: The IXF3204 framer interrupt ball INTB is asynchronous to the bus interface.When the I/M# ball sets the processor mode for a:

- Motorola processor mode, INTB is active in the '0' state.
- Intel® processor mode, INTB is active in the '1' state.

Table 54. Configuration Modes for Host Processor Interface

Configuration Mode	Intel® IXF3204 Framer I/M# Ball	Intel® IXF3204 Framer MTYPE Ball
Motorola MPC860 Processor	0	0
Motorola MC68302 Processor	0	1
Intel® i486™ Processor	1	0

The IXF3204 framer RDYB signal is used to indicate when a transfer can be completed. Since the host processor access is to the IXF3204 framer internal registers or RAM, the time taken to complete a transfer varies. As a result, the 'ready' signal inserts wait states as necessary. For host processors that do not support wait states, the IXF3204 framer provides a mechanism based on an 'access window' to deliver a constant transfer time.

20.2 Host Processor Access Window

The IXF3204 framer 'access window' consists of a set of fixed registers (WADDR, WDATA, WCMD, and WSTS at addresses 0004h to 0008h) that can be used in constant access time to perform any read or write operation to any internal memory region. When these registers are used for an operation that is a:

- Write operation, the host processor must set up the address in WADDR and the data in WDATA. Then it must write to WCMD a 00h to indicate a write operation. After that, the host processor polls the WSTS register for a 01h, which indicates the transfer is complete.
- Read operation, the host processor must set up the address in WADDR. Then it must write to WCMD a 01h to indicate a read operation. After that, the host processor polls the WSTS register for a 01h, which indicates the transfer is complete. The host processor can then read the resulting data in the WDATA register.

Table 55 lists the ball names for the IXF3204 framer and the corresponding pin names for the three target processors.

Table 55. Correspondence between Intel® IXF3204 Framer and Target Processors

Intel® IXF3204 Framer Ball Name	Motorola MPC860 Processor 8-Bit Pin Name	Motorola MC68302 Processor 8-Bit Pin Name	Intel® I486™ Processor Pin Name
ADR0	A31	A0	BLE#
ADR1	A30	A1	A1
ADR2	A29	A2	A2
ADR3	A28	A3	A3
ADR4	A27	A4	A4
ADR5	A26	A5	A5
ADR6	A25	A6	A6
ADR7	A24	A7	A7
ADR8	A23	A8	A8
ADR9	A22	A9	A9
ADR10	A21	A10	A10
ADR11	A20	A11	A11
ADR12	A19	A12	A12
ADR13	A18	A13	A13
ADR14	A17	A14	A14
ADR15	A16	A15	A15
CSB	CSx	CSx	CSx
DB0	D0	D0	D0
DB1	D1	D1	D1
DB2	D2	D2	D2
DB3	D3	D3	D3
DB4	D4	D4	D4
DB5	D5	D5	D5
DB6	D6	D6	D6
DB7	D7	D7	D7
DSB	OE	LDS	ADS
RDYB	TA#	DTACK#	RDY#
RWB	R/W#	R/W#	W/R#
WEB	WE0	-	CLK

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21.0 Electrical Characteristics

Note: The minimum and maximum values in Table 56 through Table 58 represent the performance specifications of the IXF3204 framer and are guaranteed by test, except where noted by design.

Table 56. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply core (reference to ground)	V_{CC}	-0.5	1.98	V
DC supply I/O (reference to ground)	V_{CCIO}	-0.5	3.63	V
Input voltage on any digital ball	V_{IN}	GND - 0.5	VccIO + 0.5	V
Input current on any ball	I_{IN}	-10	+10	mA
Storage temperature	T_{STG}	-65	+150	°C
Thermal resistance, junction to ambient, PBGA[1]	θJA	30C/W	38C/W	°C/W
ESD voltage on any ball [2,3]	V_{IN}	–	2,000	V

Caution: Operation at these limits can permanently damage the IXF3204 framer. Normal operation at these extremes is not guaranteed.

1. JEDEC Standard 2S2P Board.
2. ESD sensitivity classification: Human body model.
3. The ESD voltage parameter is a design target and not a product specification.

Table 57. Recommended Operating Conditions

Parameter	Sym	Min	Typical	Max	Unit
DC supply core (reference to GND)	V_{CC}	1.62	1.80	1.89	V
DC supply I/O (reference to GND)	V_{CCIO}	2.97	3.30	3.47	V
Input voltage on any ball	V_{IN}	GND - 0.3 V	–	V_{CC} + 0.3 V	V
Storage temperature	T_{STG}	-65	–	150	° C
Operating current (Core)	ICC_{CORE}	–	118	150	mA
Operating current (I/O)	ICC_{IO}	–	76	100	mA
Operating temperature	T_{OPA}	-40	+25	+85	° C

Caution: Operation at these limits can permanently damage the IXF3204 framer. Normal operation at these extremes is not guaranteed.

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Table 58. DC Characteristics

Parameter	Sym	Min	Max	Unit	Test Condition
Low-level input voltage	V_{IL}	0	0.8	V	
High-level input voltage	V_{IH}	2.0	VccIO	V	
Low-level output voltage	V_{OL}	–	0.4	V	2.0 mA
High-level output voltage	V_{OH}	2.4	–	V	-2.0 mA
Input leakage current	I_{LL}	-1.0	1.0	µA	
Input pull-up current - RESETB, TRISTB, TMS, TDI, TRSTB	I_{LL}	-15	-26	µA	
Input pull-up current - TCK	I_{LL}	-78	-130	µA	
Tristate leakage current (all outputs)	I_{3L}	-1.0	1.0	µA	

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22.0 Line Interface Timing

22.1 Line Interface Receive Timing

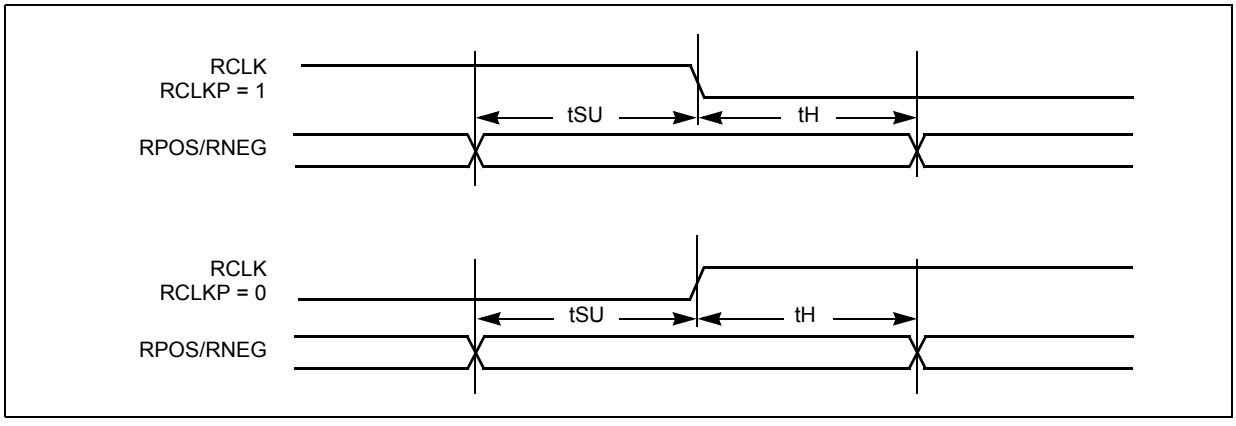
Table 59. Line Interface Receive Timing Characteristics - T1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
T1 Receive clock frequency	RCLK	–	1.544	-	MHz
T1 Receive clock duty cycle	RCLKd	40	50	60	%
RPOS/RNEG to RCLK setup time	t_{SU}	4	–	–	ns
RCLK to RPOS/RNEG hold time	t_H	8	–	–	ns
NOTE: 1. Typical values are for design aid only, not guaranteed, and not subject to production testing.					

Table 60. Line Interface Receive Timing Characteristics - E1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
E1 Receive clock frequency	RCLK	–	2.048	–	MHz
E1 Receive clock duty cycle	RCLKd	40	50	60	%
RPOS/RNEG to RCLK setup time	t_{SU}	4	–	–	ns
RCLK to RPOS/RNEG hold time	t_H	8	–	–	ns
NOTE: 1. Typical values are for design aid only, not guaranteed, and not subject to production testing.					

Figure 47. Line Interface Receive Clock Timing Diagram



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22.2 Line Interface Transmit Timing

Table 61. Line Interface Transmit Timing Characteristics - T1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
T1 Transmit clock duty cycle	TCLKd	40	50	60	%
T1 Transmit clock period	t_{PW}	–	648	–	ns
T1 Transmit clock pulse width high	t_{PWH}	260	324	388	ns
T1 Transmit clock pulse width low	t_{PWL}	260	324	388	ns
TCLK to TPOS/TNEG delay	t_D	3	–	9	ns

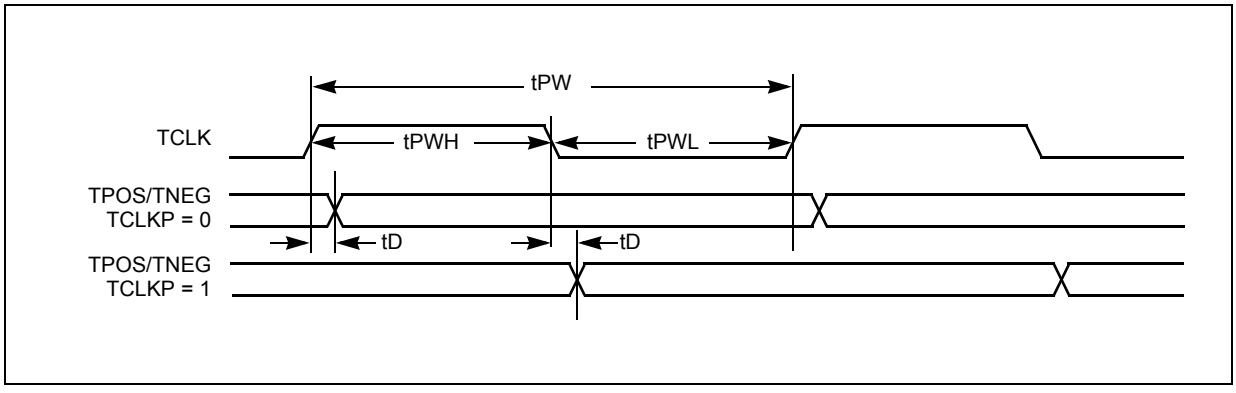
NOTE:
1. Typical values are for design aid only, not guaranteed, and not subject to production testing.
2. TCLK duty cycle widths vary according to extent of received pulse jitter displacement. Maximum and minimum TCLK duty cycles are for worst-case jitter conditions.
3. Worst-case conditions guaranteed by design only.

Table 62. Line Interface Transmit Timing Characteristics - E1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
E1 Transmit clock duty cycle	TCLKd	40	50	60	%
E1 Transmit clock period	t_{PW}	–	488	–	ns
E1 Transmit clock pulse width high	t_{PWH}	195	244	293	ns
E1 Transmit clock pulse width low	t_{PWL}	195	244	293	ns
TCLK to TPOS/TNEG delay	t_D	3	–	9	ns

NOTE:
1. Typical values are for design aid only, not guaranteed, and not subject to production testing.
2. TCLK duty cycle widths vary according to extent of received pulse jitter displacement. Maximum and minimum TCLK duty cycles are for worst-case jitter conditions.
3. Worse-case conditions guaranteed by design only.

Figure 48. Line Interface Transmit Clock Timing Diagram



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23.0 System Backplane Timing

23.1 System Backplane Receive Timing

Table 63. System Backplane Receive Timing Characteristics - T1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
T1 Receive clock frequency - BRCLK an input	BRCLK	1.544	1.544	12.352	MHz
T1 Receive clock duty cycle	BRCLKd	40	50	60	%
T1 Receive clock period - BRCLK an output	t_{PW}	–	648	–	ns
T1 Receive clock pulse width high - BRCLK an output	t_{PWH}	260	324	388	ns
T1 Receive clock pulse width low - BRCLK an output	t_{PWL}	260	324	388	ns
BRFP to BRCLK setup time - BRFP an input	t_{SU}	10	–	–	ns
BRCLK to BRFP hold time - BRFP an input	t_{H}	3	–	–	ns
BRCLK to BRFP delay - BRFP an output	t_{D}	0	–	15	ns
BRCLK to BRMFP delay	t_{D}	0	–	22	ns
BRCLK to BRDATA delay	t_{D}	0	–	15	ns
BRCLK to BRSIG delay	t_{D}	0	–	21	ns

NOTE:
1. Typical values are for design aid only, not guaranteed, and not subject to production testing.

Table 64. System Backplane Receive Timing Characteristics - E1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
E1 Receive clock frequency - BRCLK an input	BRCLK	2.048	2.048	16.384	MHz
E1 Receive clock duty cycle	BRCLKd	40	50	60	%
E1 Receive clock period - BRCLK an output	t_{PW}	–	488	–	ns
E1 Receive clock pulse width high - BRCLK an output	t_{PWH}	195	244	293	ns
E1 Receive clock out pulse width low - BRCLK an output	t_{PWL}	195	244	293	ns
BRFP to BRCLK setup time - BRFP an input	t_{SU}	10	–	–	ns
BRCLK to BRFP hold time - BRFP an input	t_{H}	3	–	–	ns
BRCLK to BRFP delay - BRFP an output	t_{D}	0	–	15	ns
BRCLK to BRMFP delay	t_{D}	0	–	22	ns
BRCLK to BRDATA delay	t_{D}	0	–	15	ns
BRCLK to BRSIG delay	t_{D}	0	–	21	ns

NOTE:
1. Typical values are for design aid only, not guaranteed, and not subject to production testing.

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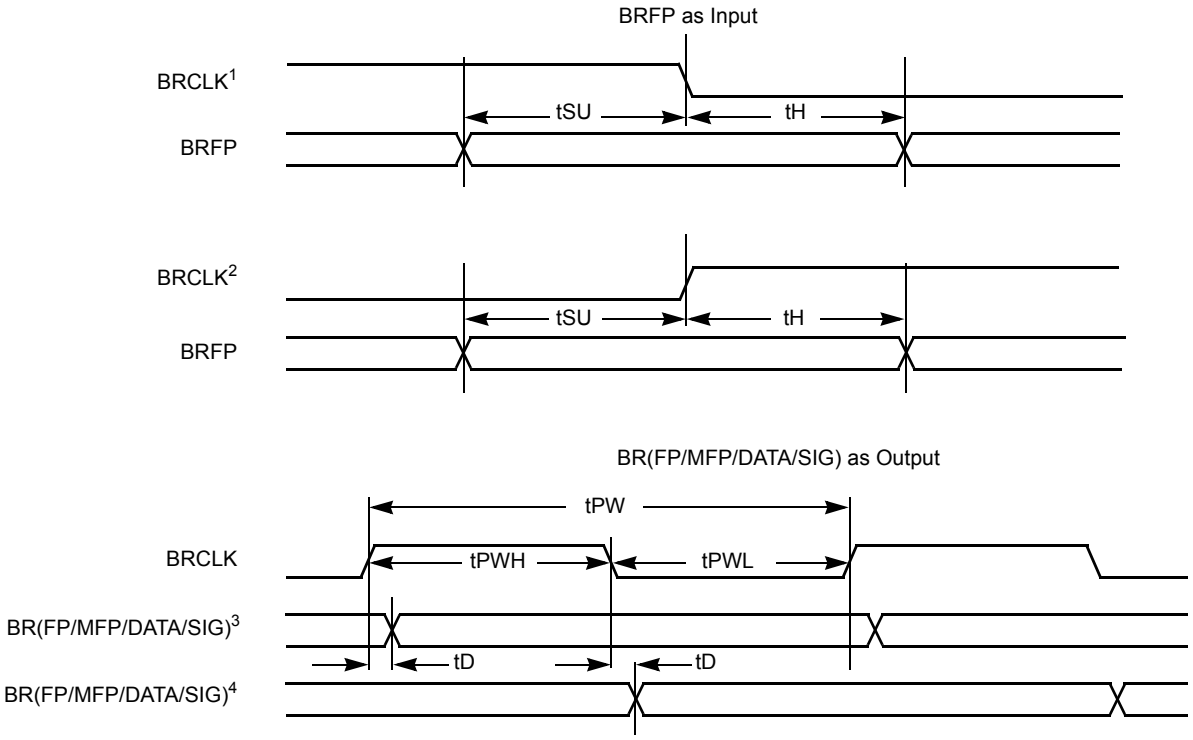
Figure 49. System Backplane Receive Timing Diagram



Notes:
1. Sampling BRFP with the falling edge of BRCLK.
2. Sampling BRFP with the rising edge of BRCLK.
3. BR(FP/MFP/DATA/SIG) delivered with the rising edge of BRCLK.
4. BR(FP/MFP/DATA/SIG) delivered with the falling edge of BRCLK.

23.2 System Backplane Transmit Timing

Table 65. System Backplane Transmit Timing Characteristics - T1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
T1 Receive clock frequency - BTCLK an input	BTCLK	1.544	1.544	12.352	MHz
T1 Receive clock duty cycle	BTCLKd	40	50	60	%
T1 Receive clock period - BTCLK an output	t_{PW}	–	648	–	ns
T1 Receive clock pulse width high - BTCLK an output	t_{PWH}	260	324	388	ns
T1 Receive clock pulse width low - BTCLK an output	t_{PWL}	260	324	388	ns
BTFP to BTCLK setup time - BTCLK an input	t_{SU}	11	–	–	ns
BTCLK to BTFP hold time - BTCLK an input	t_H	4	–	–	ns
BTCLK to BTFP delay - BTCLK an output	t_D	0	–	15	ns
BTMFP to BTCLK setup time	t_{SU}	11	–	–	ns
BTCLK to BTMFP hold time	t_H	4	–	–	ns
BTDATA to BTCLK setup time	t_{SU}	12	–	–	ns
BTCLK to BTDATA hold time	t_H	4	–	–	ns
BTSIG to BTCLK setup time	t_{SU}	12	–	–	ns
BTCLK to BTSIG hold time	t_H	4	–	–	ns

NOTE:
1. Typical values are for design aid only, not guaranteed, and not subject to production testing.

Table 66. System Backplane Transmit Timing Characteristics - E1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
E1 Receive clock frequency - BTCLK an input	BTCLK	2.048	2.048	16.384	MHz
E1 Receive clock duty cycle	BTCLKd	40	50	60	%
E1 Receive clock period - BTCLK an output	t_{PW}	–	488	–	ns
E1 Receive clock pulse width high - BTCLK an output	t_{PWH}	195	244	293	ns
E1 Receive clock out pulse width low - BTCLK an output	t_{PWL}	195	244	293	ns
BTFP to BTCLK setup time	t_{SU}	11	–	–	ns
BTCLK to BTFP hold time	t_H	4	–	–	ns
BTCLK to BTFP delay	t_D	0	–	15	ns
BTMFP to BTCLK setup time	t_{SU}	11	–	–	ns
BTCLK to BTMFP hold time	t_H	4	–	–	ns
BTDATA to BTCLK setup time	t_{SU}	12	–	–	ns
BTCLK to BTDATA hold time	t_H	4	–	–	ns
BTSIG to BTCLK setup time	t_{SU}	12	–	–	ns
BTCLK to BTSIG hold time	t_H	4	–	–	ns

NOTE:
1. Typical values are for design aid only, not guaranteed, and not subject to production testing.

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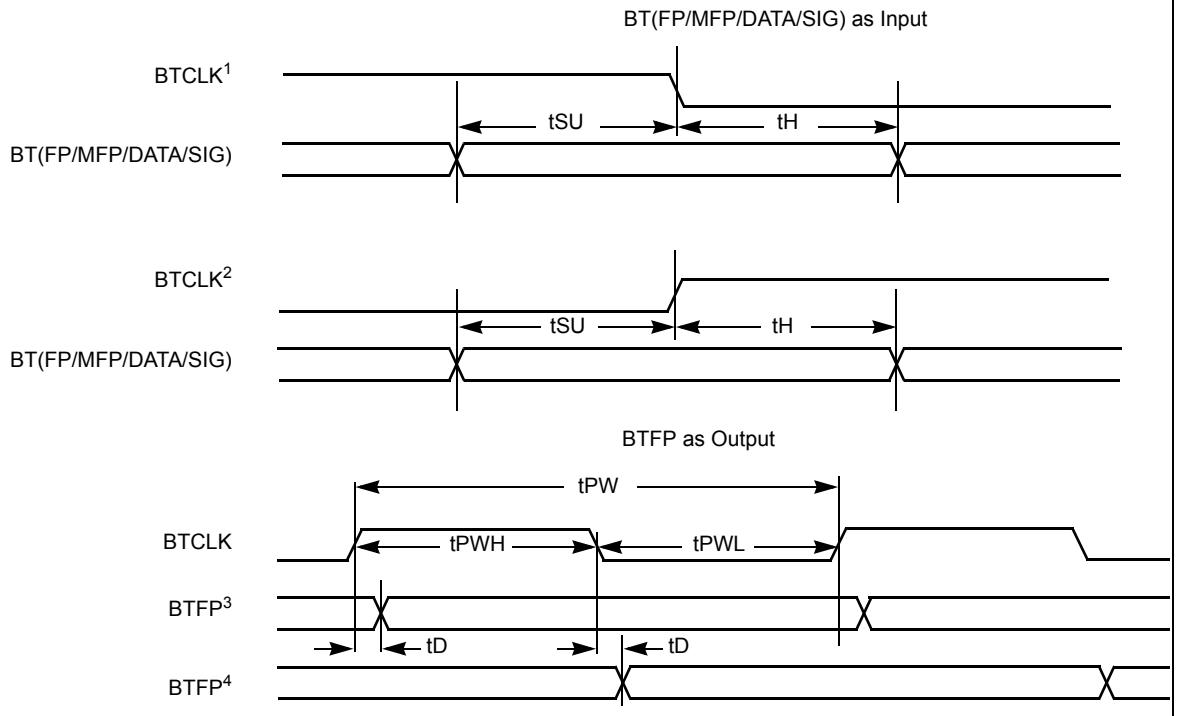
Figure 50. System Backplane Transmit Timing Diagram



Notes:
1. Sampling BT(FP/MFP/DATA/SIG) with the falling edge of BTCLK.
2. Sampling BT(FP/MFP/DATA/SIG) with the rising edge of BTCLK.
3. Data sampled with the falling edge of BTCLK.
4. Data sampled with the rising edge of BTCLK.

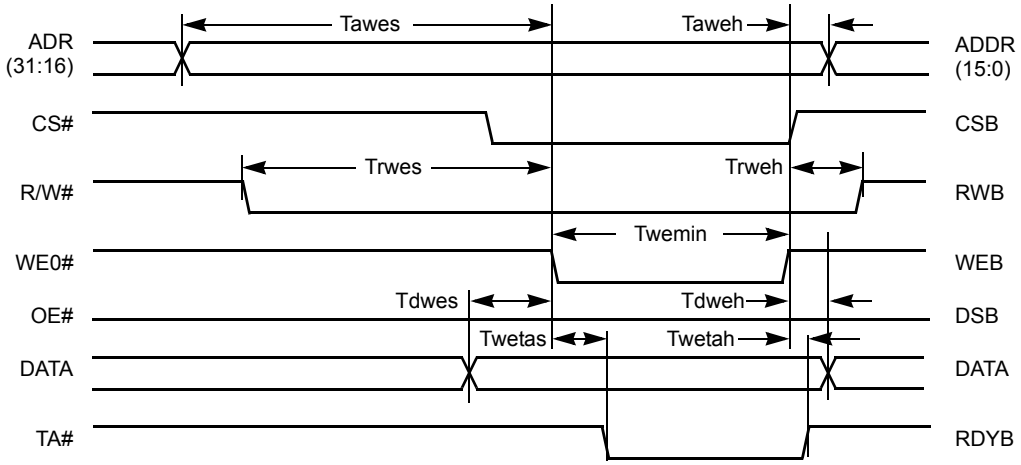
24.0 Host Processor Interface Timing

24.1 Motorola Processor Timing

Table 67. Motorola MPC860 Processor - Write Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Address setup to WE0#	Tawes	1	–	ns
Address hold from WE0#	Taweh	2	–	ns
R/W# setup to WE0#	Trwes	1	–	ns
R/W# hold from WE0#	Trweh	2	–	ns
Data setup to WE0#	Tdwes	1	–	ns
Data hold from WE0#	Tdweh	2	–	ns
WE0# minimum width	Twemin	51	–	ns
WE0# low to TA# asserted	Twetas	50	320	ns
WE0# high to TA# inactive	Twetah	9	30	ns

Figure 51. Motorola MPC860 Processor - Write Timing



Note: WE# timing restrictions apply to CS#.

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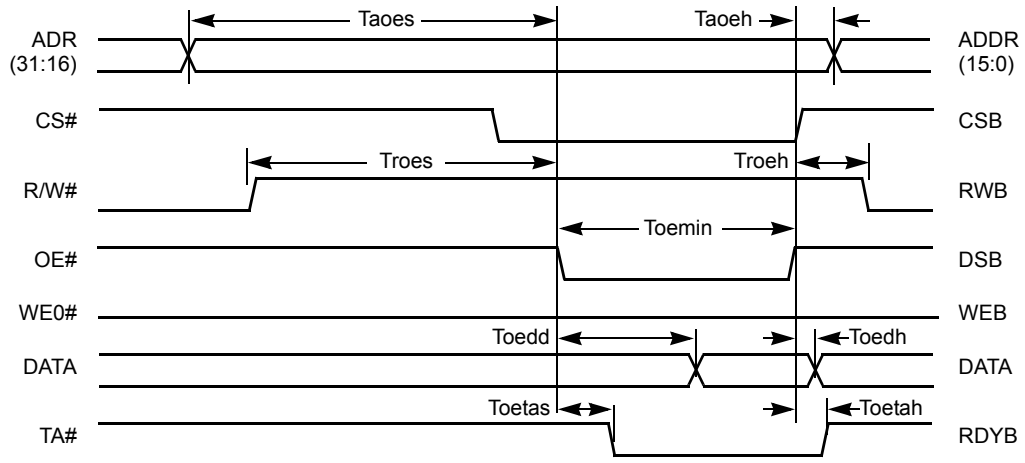
Table 68. Motorola MPC860 Processor - Read Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Address setup to OE#	Taoes	1	–	ns
Address hold from OE#	Taoeh	2	–	ns
R/W# setup to OE#	Troes	1	–	ns
R/W# hold from OE#	Troeh	2	–	ns
OE# asserted to data valid	Toedd	51	–	ns
OE# high to data invalid	Toedh	1	–	ns
OE# minimum width	Toemin	51	–	ns
OE# low to TA# asserted	Toetas	50	320	ns
OE# high to TA# inactive	Toetah	10	25	ns

Figure 52. Motorola MPC860 Processor - Read Timing



Note: WE# timing restrictions apply to CS#.

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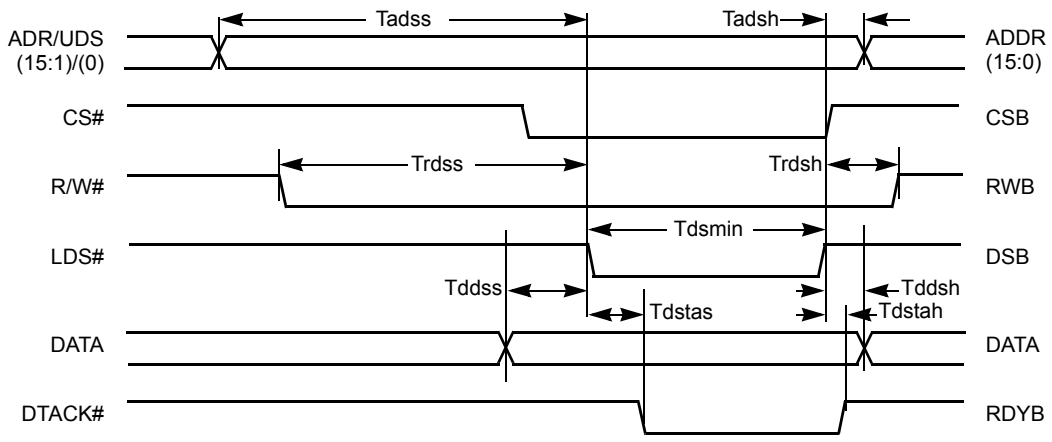
Table 69. Motorola M68302 Processor - Write Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Address setup to LDS#	Tadss	1	–	ns
Address hold from LDS#	Tadsh	2	–	ns
R/W# setup to LDS#	Trdss	1	–	ns
R/W# hold from LDS#	Trdsh	2	–	ns
Data setup to LDS#	Tddss	1	–	ns
Data hold from LDS#	Tddsh	2	–	ns
LDS# minimum width	Tdsmin	51	–	ns
LDS# low to TA valid	Tdstas	50	320	ns
LDS# high to TA invalid	Tdstah	9	30	ns

Figure 53. Motorola M68302 Processor - Write Timing



Note: LDS# timing restrictions apply to CS#.

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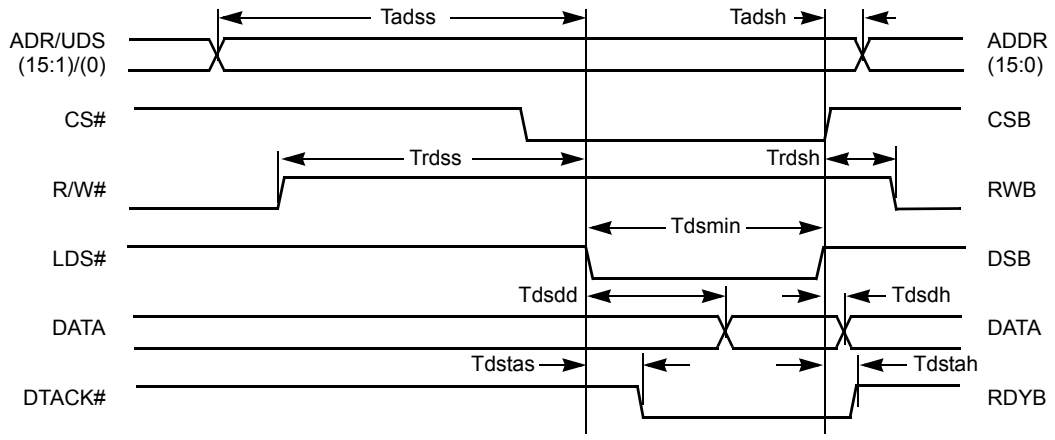
Table 70. Motorola M68302 Processor - Read Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Address setup to LDS#	Tadss	1	–	ns
Address hold from LDS#	Tadsh	2	–	ns
R/W# setup to LDS#	Trdss	1	–	ns
R/W# hold from LDS#	Trdsh	2	–	ns
LDS# low to data valid	Tdsdd	51	–	ns
Data hold from LDS# high	Tdsdh	10	–	ns
LDS# minimum width	Tdsmin	51	–	ns
LDS# low to TA valid	Tdstas	50	320	ns
LDS# high to TA invalid	Tdstah	10	25	ns

Figure 54. Motorola M68302 Processor - Read Timing



Note: LDS# timing restrictions apply to CS#.

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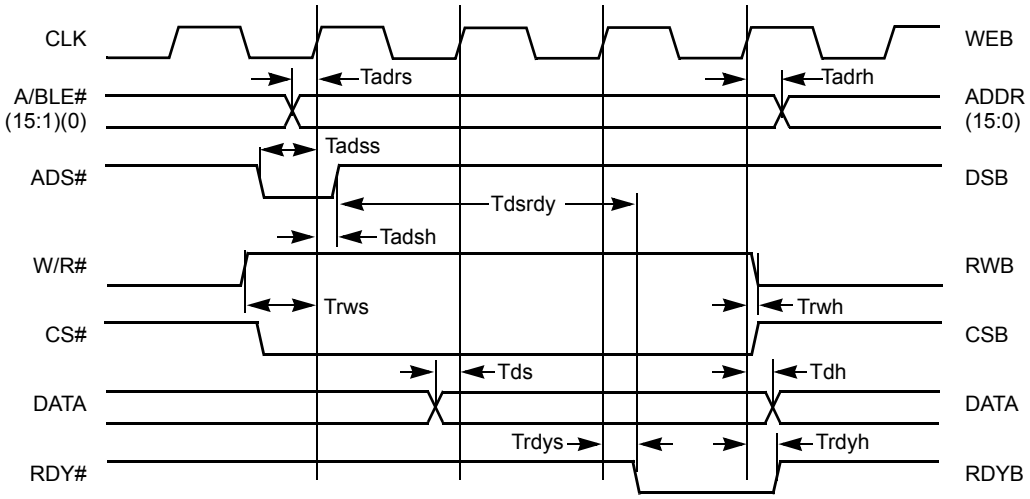
24.2 Intel® Processor Timing

Table 71. Intel® i486™ Processor - Write Timing Characteristics

Parameter	Symbol	Min	Max	Unit
ADS# high to RDY# asserted	Tdsrdy	90	380	ns
Address setup time	Tadrs	1	–	ns
Address hold time	Tadrh	2	–	ns
ADS# setup time	Tadss	3	–	ns
ADS# hold time	Tadsh	2	–	ns
W/R# setup time	Trws	1	–	ns
W/R# hold time	Trwh	2	–	ns
Data setup time	Tds	1	–	ns
Data hold time	Tdh	2	–	ns
CLK to RDY# low	Trdys	5	11	ns
CLK to RDY# high	Trdyh	5	15	ns

Figure 55. Intel® i486™ Processor - Write Timing



Notes:

- W/R# timing restrictions apply to CS#.
- Capacitance load (on RDY# pin) = 60 pF

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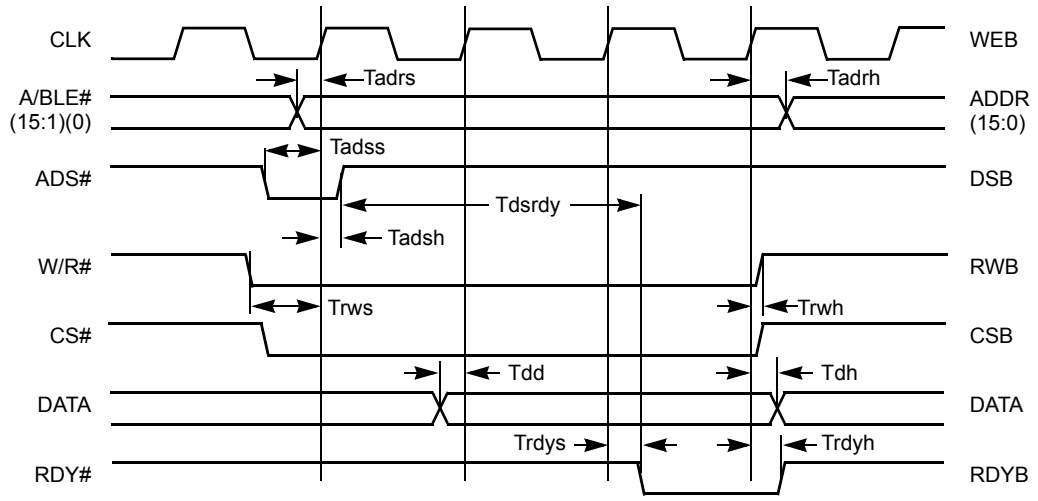
Table 72. Intel® i486™ Processor - Read Timing Characteristics

Parameter	Symbol	Min	Max	Unit
ADS# high to RDY# asserted	Tdsrdy	90	380	ns
Address setup time	Tadrs	1	–	ns
Address hold time	Tadrh	2	–	ns
ADS# setup time	Tadss	3	–	ns
ADS# hold time	Tadsh	2	–	ns
W/R# setup time	Trws	1	–	ns
W/R# hold time	Trwh	2	–	ns
CLK to data valid	Tdd	1	–	ns
Data hold from CLK	Tdh	2	–	ns
CLK to RDY# low	Trdys	5	11	ns
CLK to RDY# high	Trdyh	5	15	ns

Figure 56. Intel® i486™ Processor - Read Timing



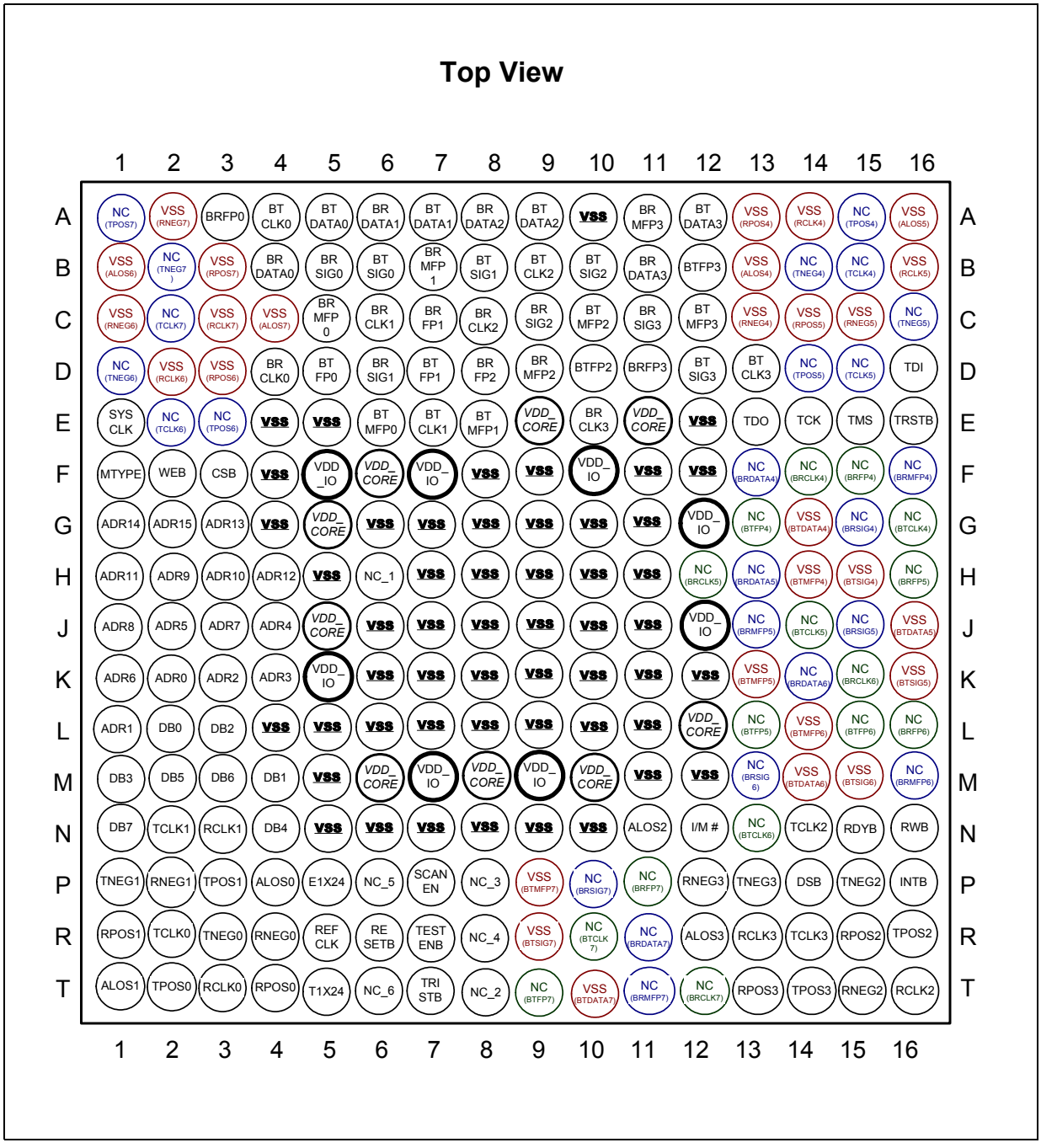
Notes:

- W/R# timing restrictions apply to CS#.
- Capacitance load (on RDY# pin) = 60 pF

25.0 Ball Assignments

Figure 57 shows the ball assignments for the IXF3204 framer.

Figure 57. Intel® IXF3204 Framer 256-Ball PBGA Ball Assignments



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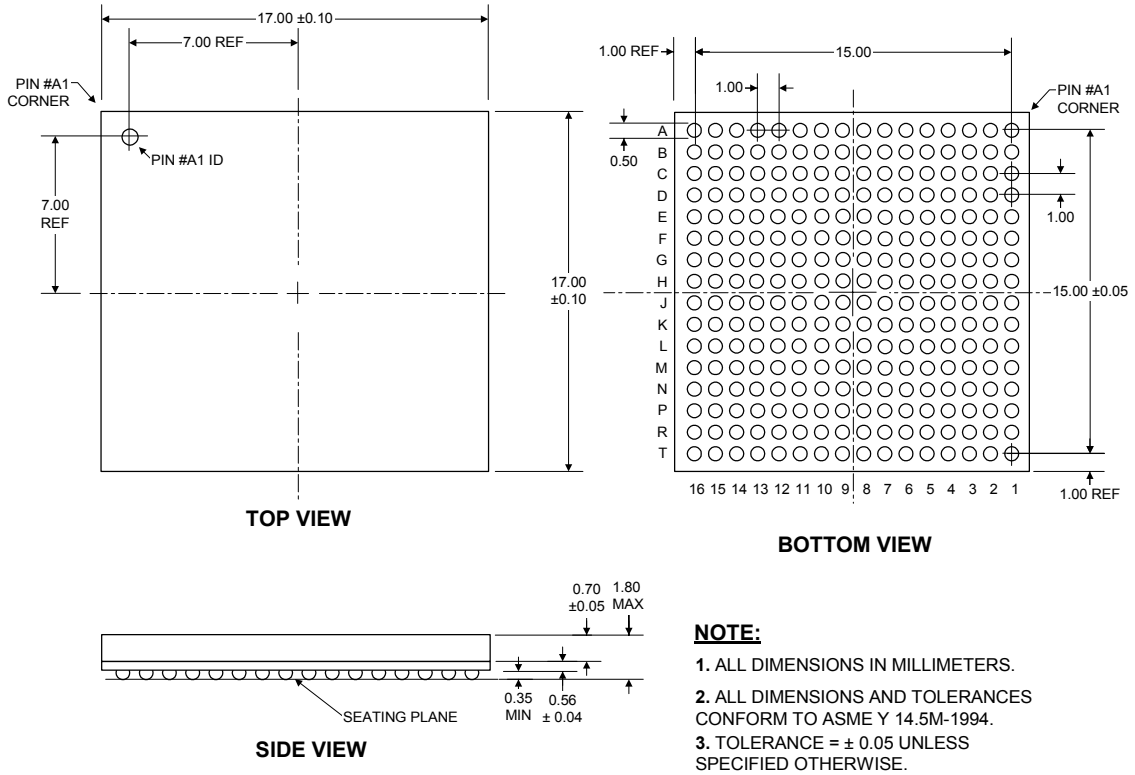
26.0 Mechanical Specifications

Figure 58. Intel® IXF3204 Framer 256-Ball PBGA Mechanical Specification



NOTE:

1. ALL DIMENSIONS IN MILLIMETERS.

2. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y 14.5M-1994.

3. TOLERANCE = ± 0.05 UNLESS SPECIFIED OTHERWISE.

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27.0 Package Markings

Figure 59 shows the location of the package markings for the IXF3204 framer. The change indicator number indicates the IXF3204 framer stepping (which is currently C0).

Figure 59. Package Markings

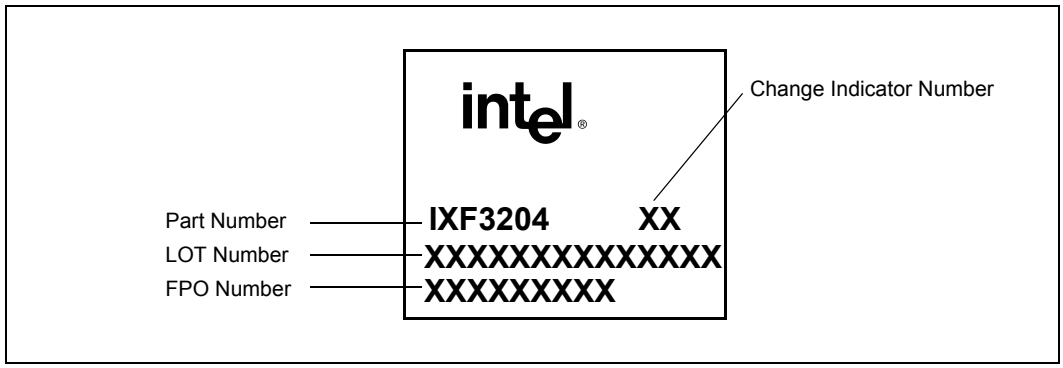

Table 73 lists the packages available for the IXF3204 framer.

Table 73. Packages

Package Markings	Package Type	Stepping
IXF3204BE C0	256 PBGA	C0

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28.0 Product and Order Information

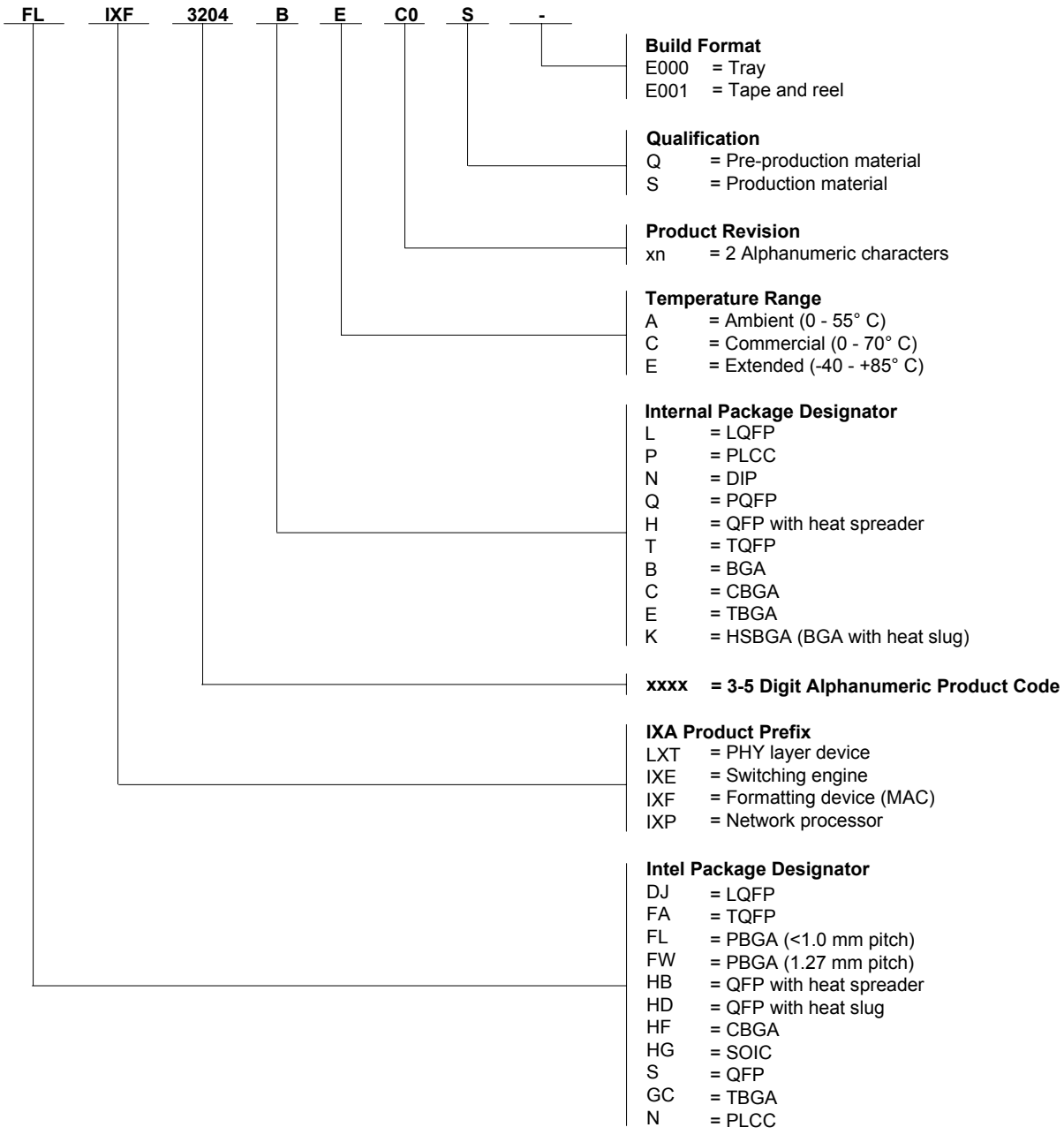
Table 74 lists product information for the IXF3204 framer.

Table 74. Product Information

Number	Revision	Qualification	Tray MM	Tape and Reel MM
IXF3204BE.C0 850086	C0	S	850086	Tray

Figure 60 shows order information for the IXF3204 framer.

Figure 60. Order Information



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29.0 Acronyms

Table 75 lists acronyms and their meaning.

Table 75. Acronyms and Meanings (Sheet 1 of 3)

Acronym	Acronym Meaning
AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
AUXP	Auxiliary Pattern
B8ZS	Binary Eight Zero Substitution
BBE	Background Block Error
BBER	Background Block Error Ratio
BERT	Bit Error Rate Test
BFA	Basic Frame Alignment
BOP	Bit Oriented Protocol
BPV	BiPolar Violation
CAS	Channel Associated Signaling
CCS	Common Channel Signaling
CHI	Concentration Highway Interface
COFA	Change Of Frame Alignment
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DDL	Derived Data Link
DmW	Digital milliWatt
DRS	Digital Reference Signal
DS0	Data Signal (at level Zero)
EB	Errored Block
EOM	End Of Message
ES	Errored Second
ESD	Electrostatic Discharge
ESF	Extended Superframe
ESR	Errored Seconds Ratio
ETSI	European Telecommunications Standards Institute
EXZ	Excess Zeroes
FAS	Frame Alignment Signal
FCS	Frame Check Sequence
FDL	Facility Data Link
FIFO	First In, First Out
GCI	General Circuit Interface
GR-303	Generic Requirements-303

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Table 75. Acronyms and Meanings (Sheet 2 of 3)

Acronym	Acronym Meaning
HDB3	High Density Bipolar Three
HDLC	High-level Data Link Control, High-level Data Link Controller
H-MVIP	High-density Multi-Vendor Integration Protocol
I/O	In/Out
IMAP	Integrated Multi-service Access Platform
ISDN	Integrated Service Digital Network
ITU	International Telecommunication Union
LAPB	Link Access Procedure Balanced
LAPD	Link Access Procedure D
LH	Long Haul
LH/SH	Long Haul/Short Haul
LIU	Line Interface Unit
LLB	Line LoopBack
LOF	Loss Of Frame
LOS	Loss Of Signal
Mbps	Megabits per second
MFAS	Multiframe Alignment Signals
MOP	Message-Oriented Protocol
MVIP	Multi-Vendor Integration Protocol
NEG	Negative
NFAS	Not Frame Alignment Signal
OOF	Out Of Frame
OVF	Overflow
PBGA	Plastic Ball Grid Array
PCM	Pulse-Code Modulation
PLB	Payload LoopBack
POS	Positive
PRBS	Pseudo-Random Bit Sequence
PRM	Performance Report Messaging
QRSS	Quasi-Random Sequence Signal
RAI	Remote Alarm Indication
RAM	Random-Access Memory
REBE	Remote End Block Error
Sa	National Bits
SAPI	Service Access Point Identifier
SAS-P	**S**everely Errored Frame / **A**larm Indication Signal **S**econds - **P**ath
SES	Severely Errored Second
SESR	Severely Errored Seconds Ratio

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Table 75. Acronyms and Meanings (Sheet 3 of 3)

Acronym	Acronym Meaning
SF	SuperFrame
SH	Short Haul
Si	International Bit
SLC®96	Lucent Subscriber Loop Carrier
TDM	Time Division Multiplex
TEI	Terminal Endpoint Identifier
TLB	Time-Slot LoopBack
TS	Time Slot
UNF	Underflow
ZCS	Zero Code Suppression