Introduction

80 CHANNEL SEGMENT DRIVER FOR LCD DOT MATRIX

The KS0786 is a LCD driver LSI which is fabricated by low power CMOS high voltage process technology. This device consists of 80 bit bidirectional shift register, 80 bit data latch and 80 bit driver(refer to fig. 1)
And this device has Power down function on chip.

Dot matrix LCD segment driver with 80 channel output
- Input/Output signal
  -Input: 4 bit parallel display data, control from controller and bias voltage(V_0, V_2, V_3, V_5)
  -Output: 80 channel waveform for LCD driving
- Power down function to make power consumption low

Features

- Power supply voltage: 2.7~5.5(V)
- Supply voltage for display: 10~33(V) (Absolute Max. Rate: 37[V])
- Parallel data processing(4 bit)
- Applicable LCD duty: 1/64~1/400(1/300: 3[V])
- Interface

COM. driver	SEG. driver
KS0789	KS0786

- High voltage CMOS process
  Data transfer speed : 8MHz(6.5MHz : 3[V])
- 98 PIN SLIM TAB

BLOCK DIAGRAM

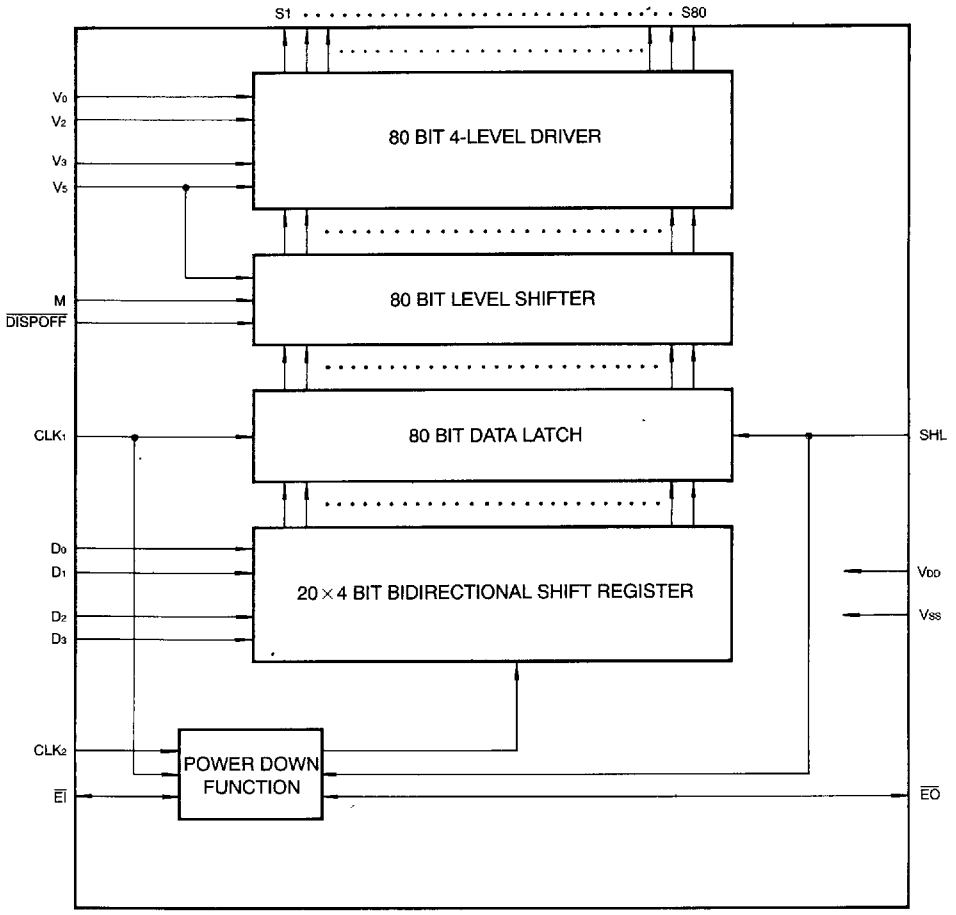
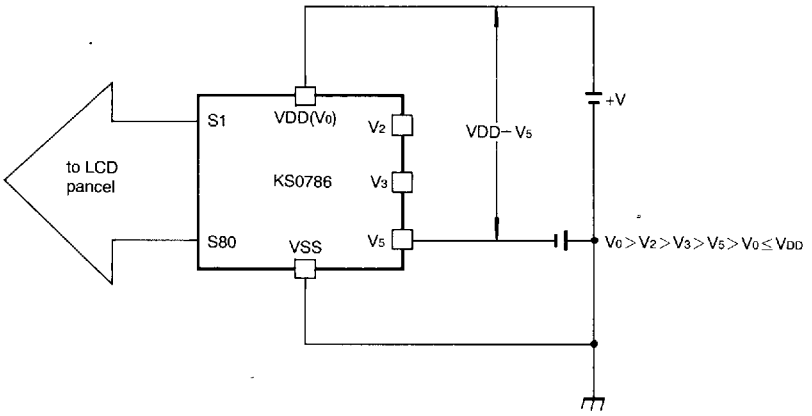


Fig1. KS0786 BLOCK DIAGRAM

MAXIMUM ABSOLUTE LIMIT (Ta=25° C)

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	-0.3 ~7.0	V
Driver supply voltage	V_{LCD}	7~37	V
Input voltage	V_{IN}	-0.3 ~V_{DD}+0.3	V
Operating temperature	T_{OPR}	-25 ~+75	°C
Storage temperature	T_{STG}	-40~+125	°C

Voltage greater than above may result in damage to the circuit.
· reference voltage: V_{SS}



ELECTRICAL CHARACTERISTICS

1) DC Characteristics(V_{DD}=2.7~5.5V, V_{DD}-V5=28V, Vss=0V, Ta=-20~+75° C)

Characteristic	Symbol	Applicable pin		MIN	TYP	MAX	UNIT
Input Voltage	V_{IH}	CLK1,CLK2,EI,EO,DO~D3, SHL,DISPOFF,M		0.8V_{DD}	–	V_{DD}	V
	V_{IL}			0	–	0.2V_{DD}	
Output Voltage	V_{OH}	I_{OH}=-0.4mA (V_{DD}=3V, I_{OH}=-0.2mA)	EI,EO	V_{DD}-0.4 (V_{DD} -0.6)	–	V_{DD}	V
	V_{OL}	I_{OL}=0.4mA (V_{DD}=3V, I_{OL}=0.2mA)		0	–	0.4(0.6)	
Output IMPEDANCE	R_{ON}	V_{DD}-V5=28V, |VN-V0|=0.25V*1)	S1~S80	–	2	4	KΩ
Dissipation Current(*2)	I_{ST}	fM=35Hz fCLK2=6.5MHz fCLK1=14KHz	stand-by mode*3)	–	–	200	μA
	I_{DD}		operating Mode	–	–	3	mA
Input Current	I_{IL1}	V_{IN}=V_{DD}~Vss	CLK1,CLK2,$\overline{EI}$,$\overline{EO}$,D0~D3, SHL,$\overline{DISPOFF}$,M	-1	–	1	μA
	I_{IL2}	V_{IN}=V_{DD}~V5	V0, V2,V3	-100			μA

*1) V_n=V_{DD}~V5, V0 = V_{DD}
V2 = V_{DD}-2/15(V_{DD}-V5)
V3 = V_{DD}-13/15(V_{DD}-V5)

2) output: no Load, Input: V_{IH}=V_{DD}, V_{IL}=Vss

3) The current flowing V_{DD} through Vss, when SHL=V_{DD}, $\overline{EI}$=V_{DD} (stand-by mode)

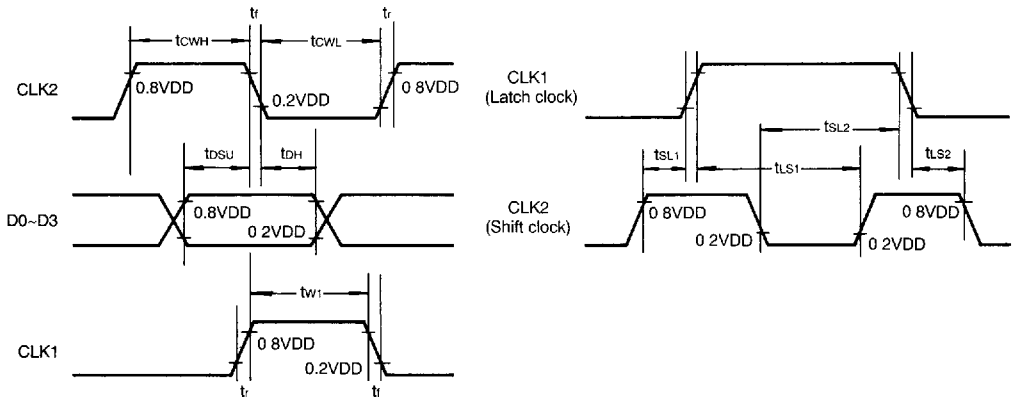
2) AC Characteristics(V_{DD}=2.7~5.5V, V_{DD}-V5=28V, V_{SS}=0V, Ta=-20~+75° C C_L=15pF)

Characteristic	Symbol	Test condition / Applicable PIN		MIN	TYP	MAX	UNIT
Shift clock frequency	f_{CLK2}	duty = 50%	V_{DD}=4.5V	–	–	8	MHz
			V_{DD}=2.7V	–	–	6.5	MHz
CLK2 pulse width	t_{CWH},	V_{DD}=4.5V		45	–	–	ns
	t_{GWL}	V_{DD}=2.7V		60	–	–	
CLK1 pulse width	t_{W1}	V_{DD}=4.5V		45	–	–	
		V_{DD}=2.7V		60	–	–	
Clock rising/falling time	t_r / t_f	*1)		–	–	15	
Data set-up time	t_{DSU}	–		20	–	–	
Data hold time	t_{DH}	–		20	–	–	
CLK2-CLK1 time(1)	t_{SL1}	–		10	–	–	
CLK2-CLK1 time(2)	t_{SL2}	V_{DD}=4.5V		45	–	–	
		V_{DD}=2.7V		60	–	–	
CLK1-CLK2 time(1)	t_{LS1}	V_{DD}=4.5V		45	–	–	
		V_{DD}=2.7V		60	–	–	
CLK2-CLK1 time(2)	t_{LS2}	–		10	–	–	
Enable Input set-up time	t_{PSU}	$\overline{EI}$, $\overline{EO}$ Input		20	–	–	
Propagation delay time(1)	t_{PD1}	CLK2 → $\overline{EI}$, $\overline{EO}$		–	–	100	
Propagation delay time(2)	t_{PD2}	$\overline{DISPOFF}$ → S1~S80		–	–	1.0	μs
Propagation delay time(3)	t_{PD3}	CLK1 → S1~S80		–	–	1.0	
Propagation delay time(4)	t_{PD4}	M → S1~S80		–	–	1.0	

*1) When shift clock(CLK2) operates high speed, t_r, t_f < (1/f_{CLK2}-2t_{W2})/2

3) TIMING DIAGRAM

Input Timing characteristic



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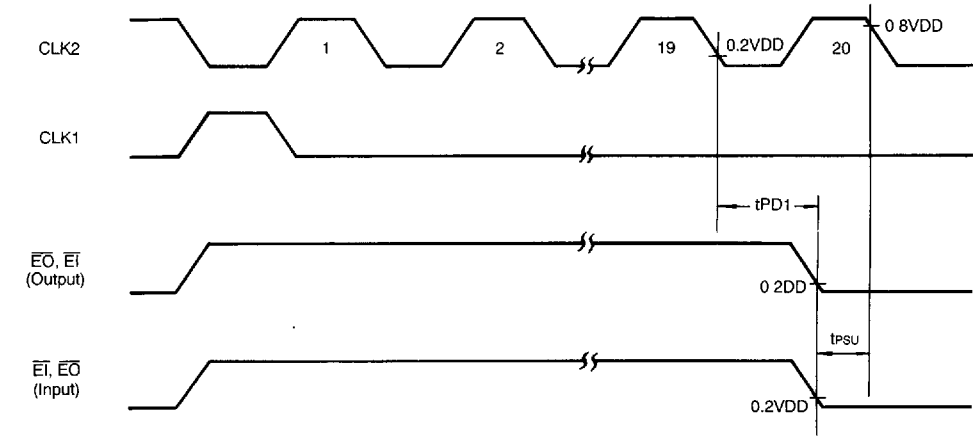
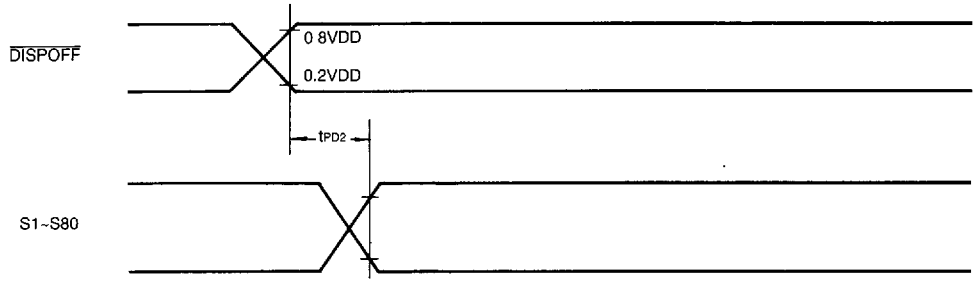
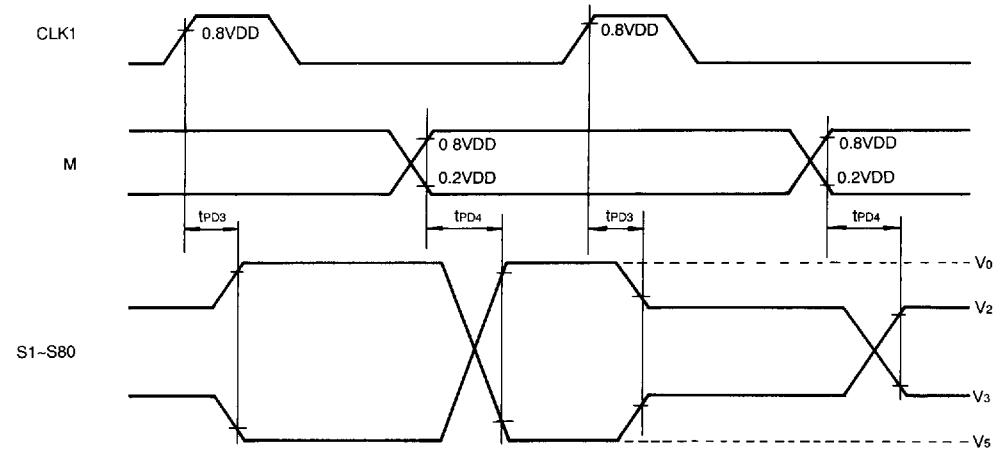
Input/output Timing characteristic



Output Timing Characteristic ①



Output Timing Characteristic ②



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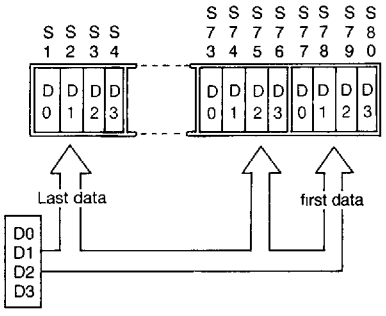
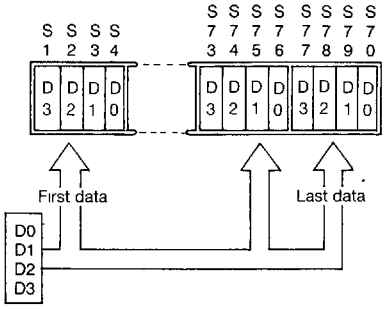
PIN DESCRIPTION

Pin(No)	Input Output	name	Function	Interface
V_{DD}(87,98)		Power supply	For logical circuit(2.7~5.5V)	Power
V_{SS}(85)			0V(GND)	
V_5(84)			For LCD drive circuit	
V_0, V_2, V_3 (81~83)	Input	LCD driver output voltage level	Bias supply voltage terminals to drive the LCD. Bias voltage divided by resistance is usually used as supply voltage source. V_0, V_5 select level V_2, V_3 ·· nonselect level(refer to note1)	Power
S1~S80	Output	LCD driver output	Display data output pin which corresponds to the respective latch contents. One of V0,V2, V3, and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal.(refer to note 2)	LCD Panel
CLK2(92)	Input	data shift clock	Clock pulse input for the 4 bit parallel shift register at the falling edge of the clock pulse. The clock pulse, which was input when the ENABLE FLIP FLOP is not active condition, is invalid.	controller
M(90)	Input	alternate signal for LCD driver output	Alternate signal input pin for LCD driving Normal frame inversion signal is input.	controller
CLK1(91)	Input	data latch clock	The signal for latching the shift register contents is input to this terminal. CLK1 pulse "H" level initializes ENABLE FLIP FLOP.	controller
$\overline{DISPOFF}$ (89)	Input	Display off	Control input pin for display data output level (S1~S80), V0 level is output from S1~S80 terminal during "L" level input. LCD becomes non-selected by V0 level output from every output of segment divers and every output of common drivers	controller

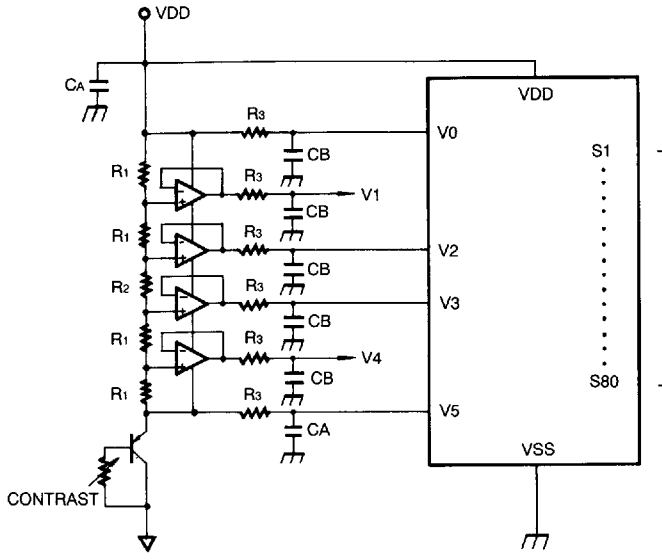
PIN Name(No)	Input Output	Name	Function	Interface
SHL(86)	Input	Data shift direction select	$\overline{EI}$ and $\overline{EO}$ can be used as either input terminal or output terminal according to the condition of	Controller
$\overline{EO}$, $\overline{EI}$ (97, 88)	I/O	Chip enable Input/Output		

PIN	I / O	SHL	Data shift direction	Input Output
$\overline{EO}$	Input	L		$\overline{EI}$ is connected to Next KS0786;s $\overline{EO}$ when the KS0786's are connected in series(cascade connection)
$\overline{EI}$	Output			
$\overline{EI}$	Input	H		$\overline{EO}$ is connected to Next KS0786;s $\overline{EI}$ when the KS0786's are connected in series(cascade connection)
$\overline{EO}$	Output			

D0~D3 (96~93)	Input	Data	Display data input Pins

D0~D3	M	Output level	DISPLAY ON THE LCD
L	L	V_2	OFF
H	L	V_0	ON
L	H	V_3	OFF
H	H	V_5	ON

(Note 1) Divide circuit for LCD driving(1/15 bias, 1/200 duty)



V_0, V_5	Selection level
V_2, V_3	non-selection level

1. Values of R_1 & R_2 are selected, according to LCD Panel
   Bias factor : 1/15

   then, $\frac{R1}{4R1 + R2} = \frac{1}{15}$

   ex) R1= 3KΩ , R2 = 33KΩ

2. Resistor R_3 for protecting over-current is about 150Ω
3. C_B: Capacitor for LCD driving voltage stability. (Several μF)
4. CA ; 0.1 μF

(Note 2) Relation between M and Data.

M	latch data	$\overline{DISPOFF}$	Output Level (S1~S80)
L	L	H	V_2
L	H	H	V_0
H	L	H	V_3
H	H	H	V_5
X	X	L	V_0

*H : "H" level L:"L" level X: Don't care → Fix to High or Low in order to protect floating status.

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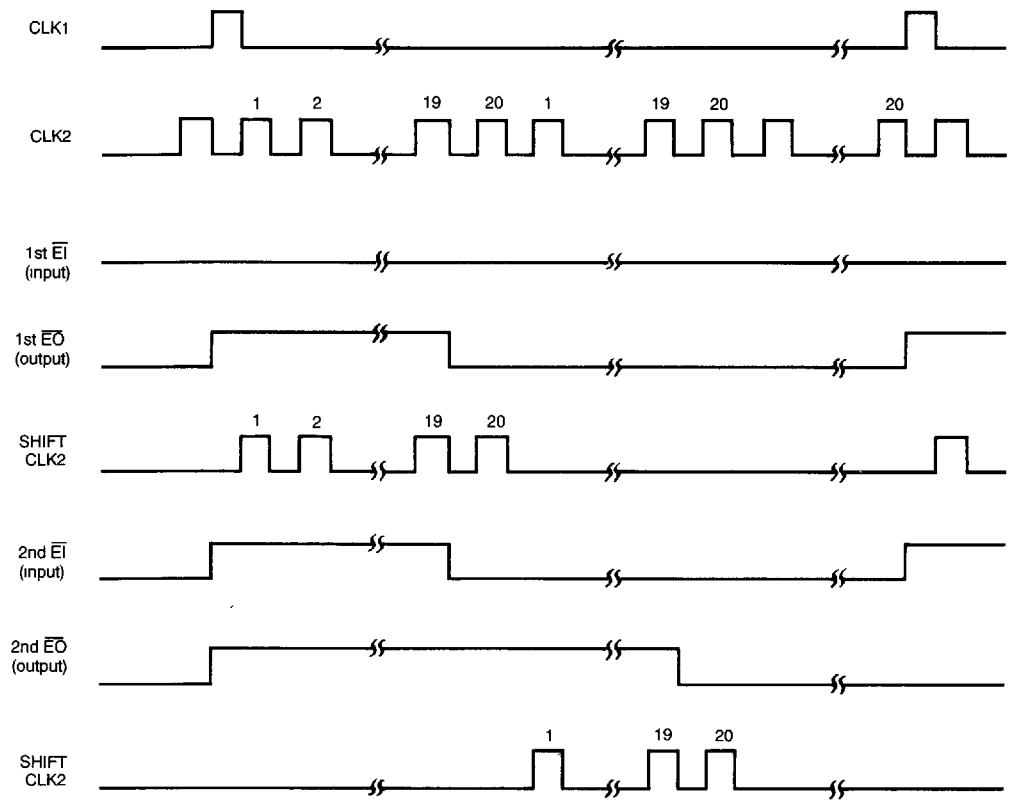
POWER DOWN FUNCTION

In order to reduce the power consumption in case of cascade connection.
KS0786 has a "Power down function".

$\overline{EI}$	Enable input	Enable	L
		Disable	H
$\overline{EO}$	Enable output	$\overline{EO}$ of N'th driver is connected to $\overline{EI}$ of (N+1)'th driver KS0786.	

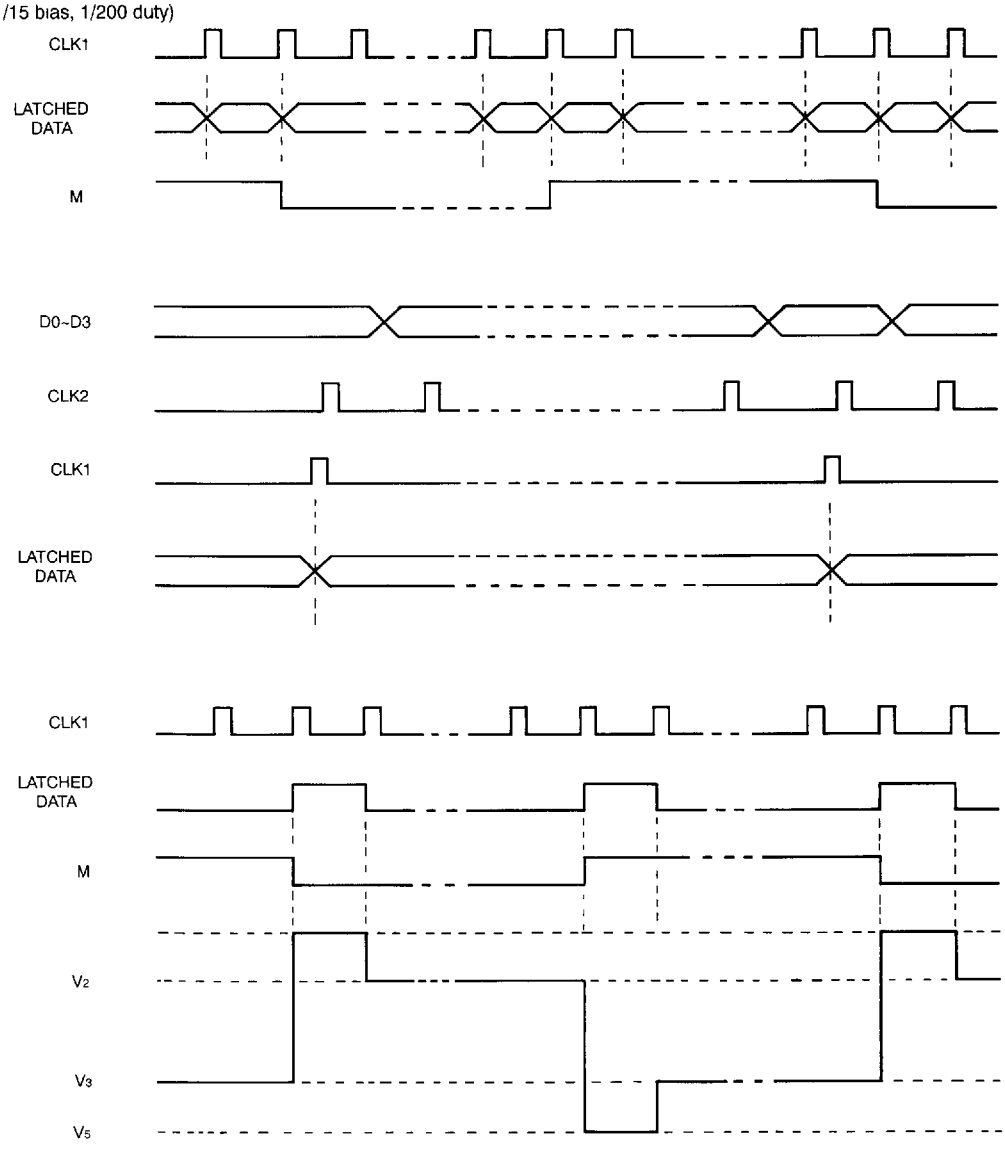


SHL = "H"($\overline{EI}$ = Input, $\overline{EO}$ = Output)
First KS0786's $\overline{EO}$ should be connected to second KS0786's $\overline{EI}$.

Fig 4. Timing Characteristics(cascade connection)

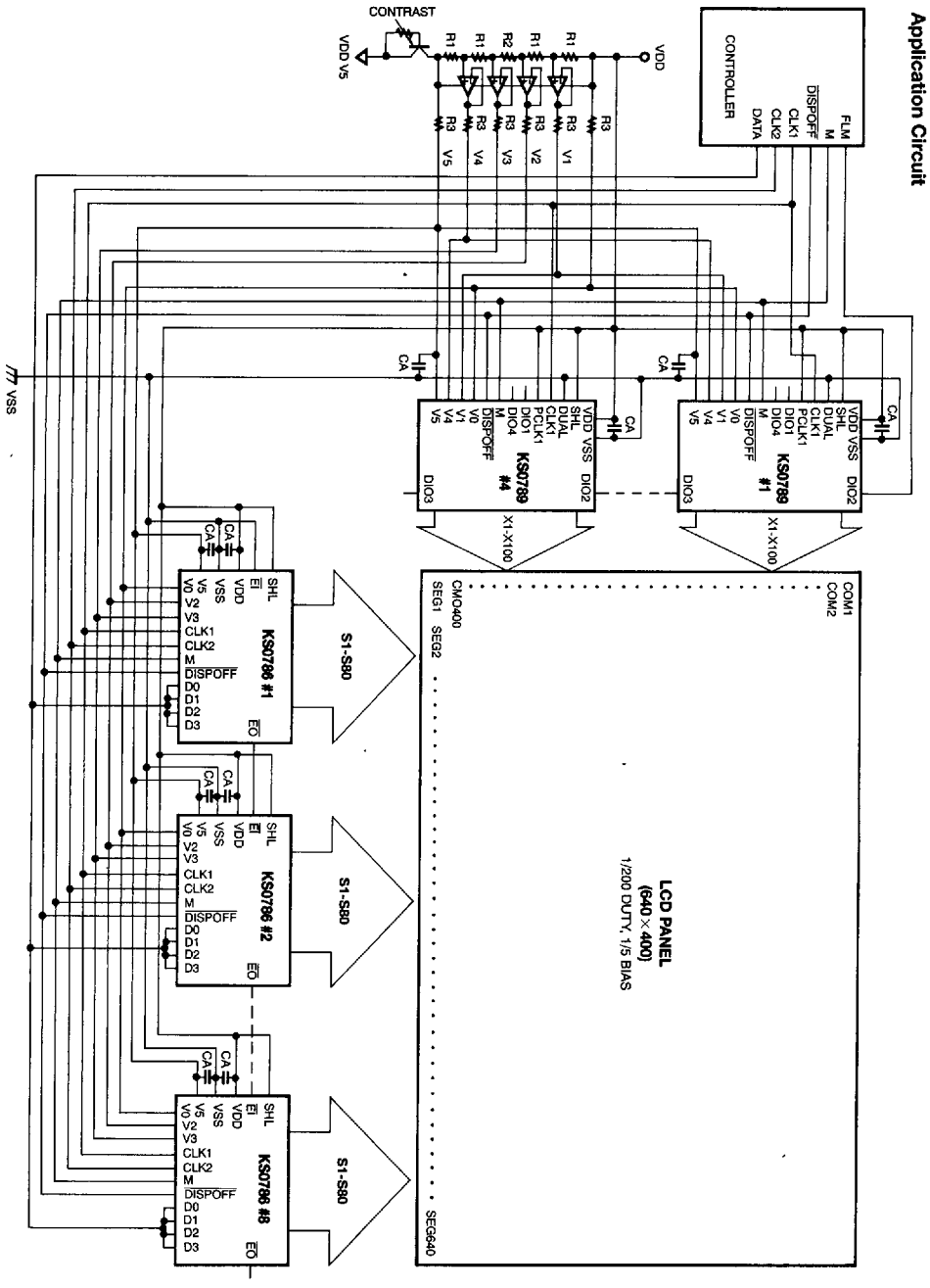
TIMING CHARTS

(1/15 bias, 1/200 duty)



$V_0=V_{DD}$
$V_2=V_{DD}-2/15\ V_{LCD}$
$V_3=V_{DD}-13/15\ V_{LCD}$
$V_{LCD}=V_{DD}-V_5$

Application Circuit



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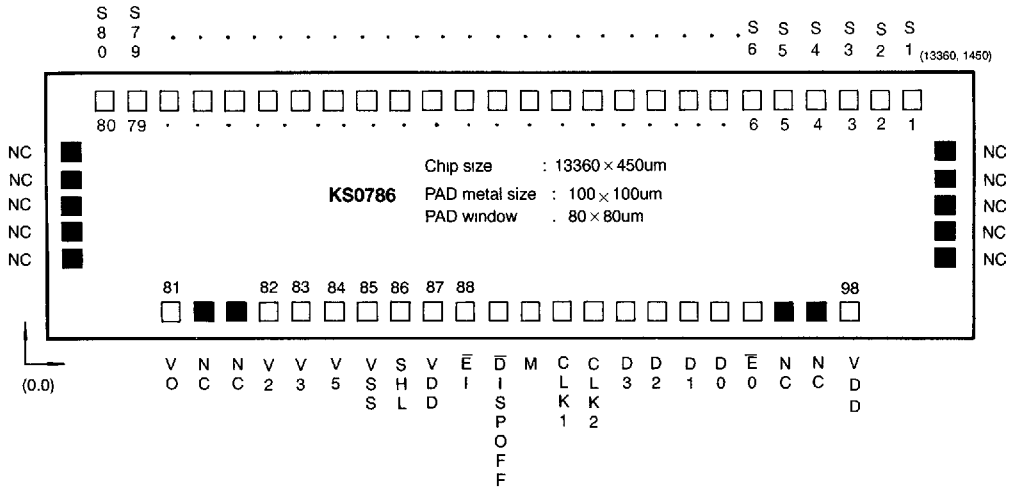
PAD Diagram



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PAD Location

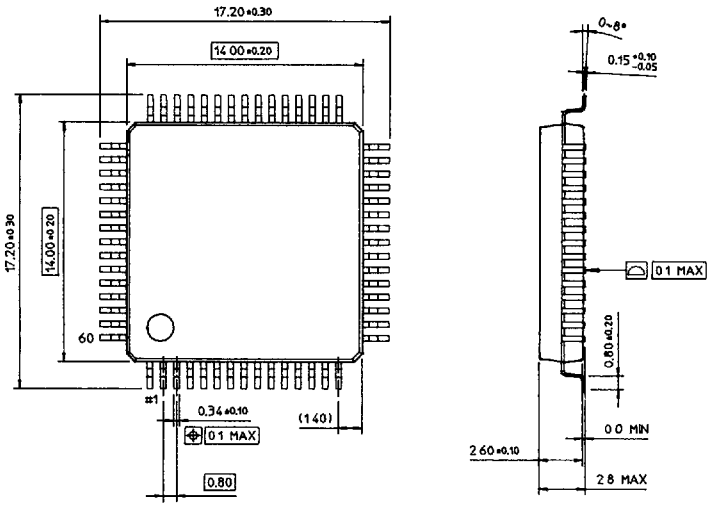
(Unit ;μm)

PAD No.	PAD Name	COORDINATE		PAD No.	PAD Name	COORDINATE		PAD No.	PAD Name	COORDINATE	
		X	Y			X	Y			X	Y
–	NC	13145	410	43	S43	6285	410	83	V_3	3385	215
–	NC	13145	535	44	S44	6125	535	84	V_5	3735	215
–	NC	13145	660	45	S45	5965	660	85	V_{SS}	4085	215
–	NC	13145	785	46	S46	5805	785	86	SHL	4385	215
–	NC	13145	910	47	S47	5645	910	87	V_{DD}	4725	215
1	S1	13005	1235	48	S48	5485	1235	88	$\overline{EI}$	5065	215
2	S2	12845	1235	49	S49	5325	1235	89	$\overline{DISPOFF}$	5784	215
3	S3	12685	1235	50	S50	5165	1235	90	M	7585	215
4	S4	12525	1235	51	S51	5005	1235	91	CLK1	8402	215
5	S5	12365	1235	52	S52	4845	1235	92	CLK2	8685	215
6	S6	12205	1235	53	S53	4685	1235	93	D3	9002	215
7	S7	12045	1235	54	S54	4525	1235	94	D2	9285	215
8	S8	11885	1235	55	S55	4365	1235	95	D1	9602	215
9	S9	11725	1235	56	S56	4205	1235	96	D0	9885	215
10	S10	11565	1235	57	S57	4045	1235	97	$\overline{EO}$	10685	215
11	S11	11405	1235	58	S58	3885	1235	–	NC	11385	215
12	S12	11245	1235	59	S59	3725	1235	–	NC	12070	215
13	S13	11085	1235	60	S60	3565	1235	98	V_{DD}	12270	215
14	S14	10925	1235	61	S61	3405	1235				
15	S15	10765	1235	62	S62	3245	1235				
16	S16	10605	1235	63	S63	3085	1235				
17	S17S	10445	1235	64	S64	2925	1235				
18	S18	10285	1235	65	S65	2765	1235				
19	S19	10125	1235	66	S66	2605	1235				
20	S20	9965	1235	67	S67	2445	1235				
21	S21	9805	1235	68	S68	2285	1235				
22	S22	9645	1235	69	S69	2125	1235				
23	S23	9485	1235	70	S70	1965	1235				
24	S24	9325	1235	71	S71	1805	1235				
25	S25	9165	1235	72	S72	1645	1235				
26	S26	9005	1235	73	S73	1485	1235				
27	S27	8845	1235	74	S74	1325	1235				
28	S28	8685	1235	75	S75	1165	1235				
29	S29	8525	1235	76	S76	1005	1235				
30	S30	8365	1235	77	S77	845	1235				
31	S31	8205	1235	78	S78	685	1235				
32	S32	8045	1235	79	S79	525	1235				
33	S33	7885	1235	80	S80	365	1235				
34	S34	7725	1235	–	NC	215	910				
35	S35	7565	1235	–	NC	215	785				
36	S36	7405	1235	–	NC	215	660				
37	S37	7245	1235	–	NC	215	535				
38	S38	7085	1235	–	NC	215	410				
39	S39	6925	1235	81	V_0	640	215				
40	S40	6765	1235	–	NC	1340	215				
41	S41	6605	1235	–	NC	1985	215				
42	S42	6445	1235	82	V_2	2685	215				

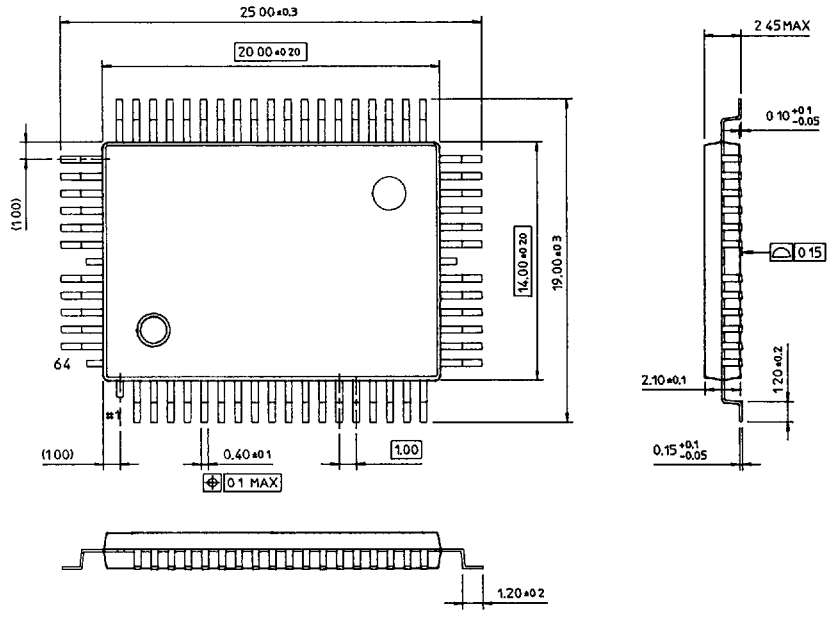
PACKAGE DIMENSIONS

Dimensions in Milimeters

60-QFP-1414A



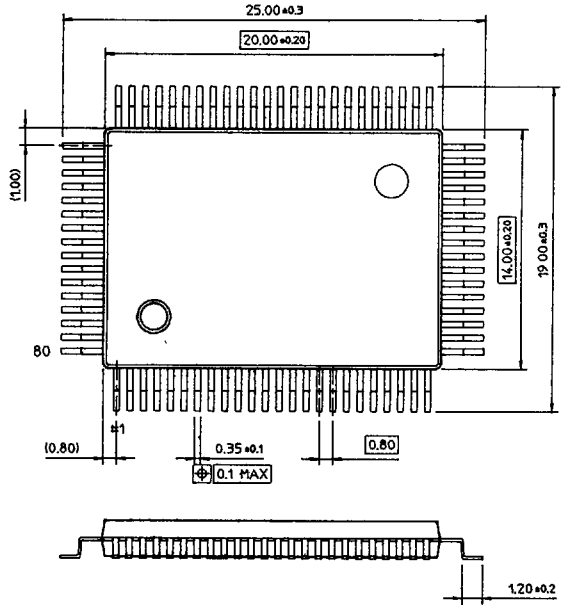
64-QFP-1420D



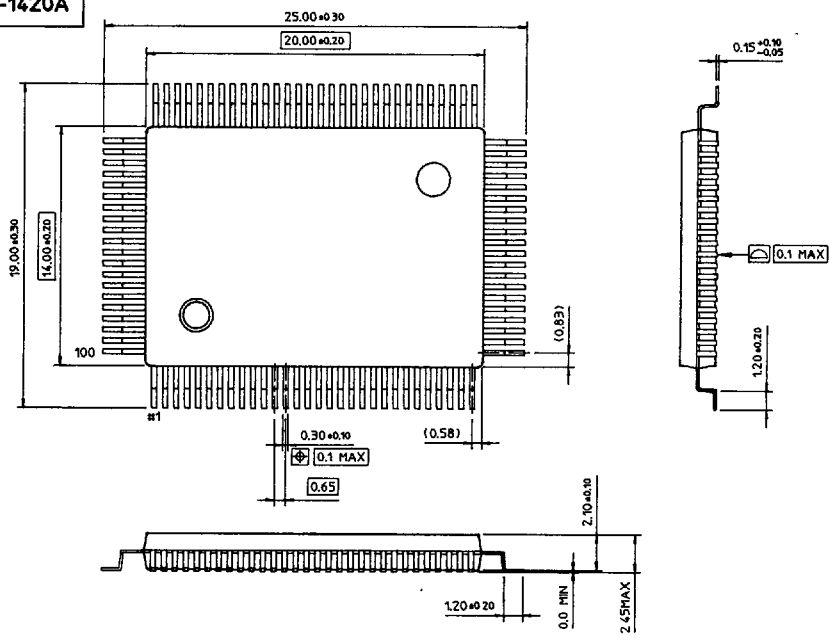
PACKAGE DIMENSIONS

Dimensions in Milimeters

80-QFP-1420A



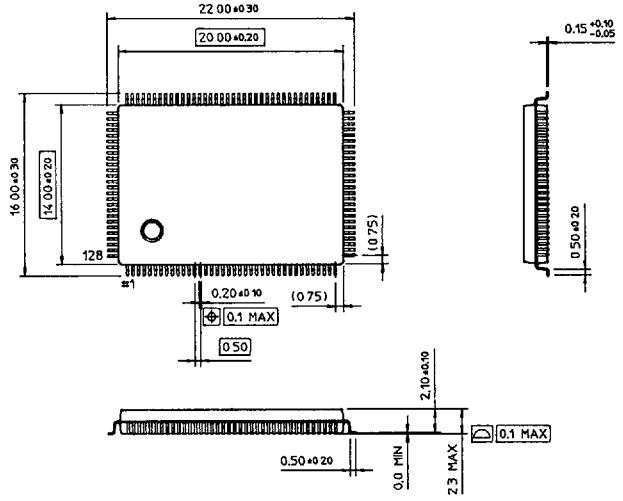
100-QFP-1420A



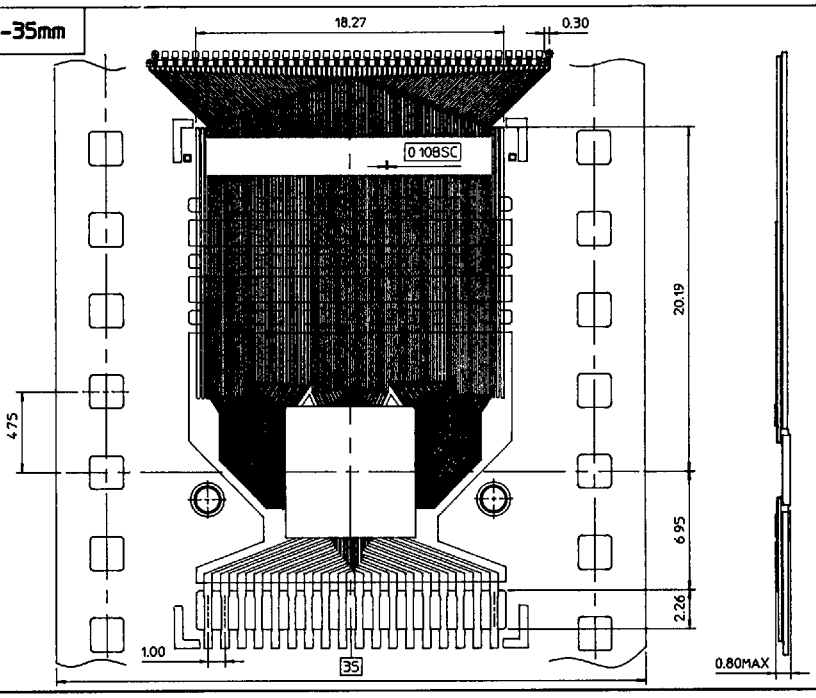
PACKAGE DIMENSIONS

Dimensions in Milimeters

128-QFP-1420



98-TAB-35mm



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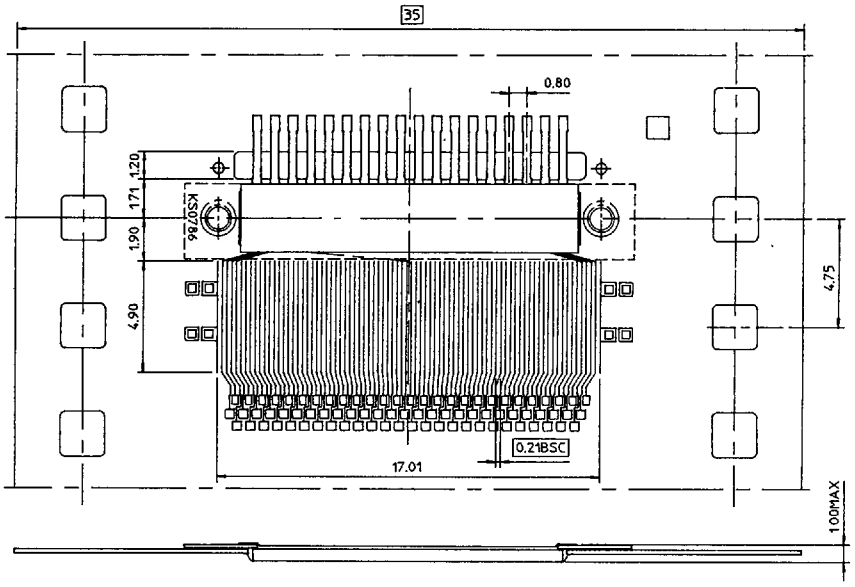
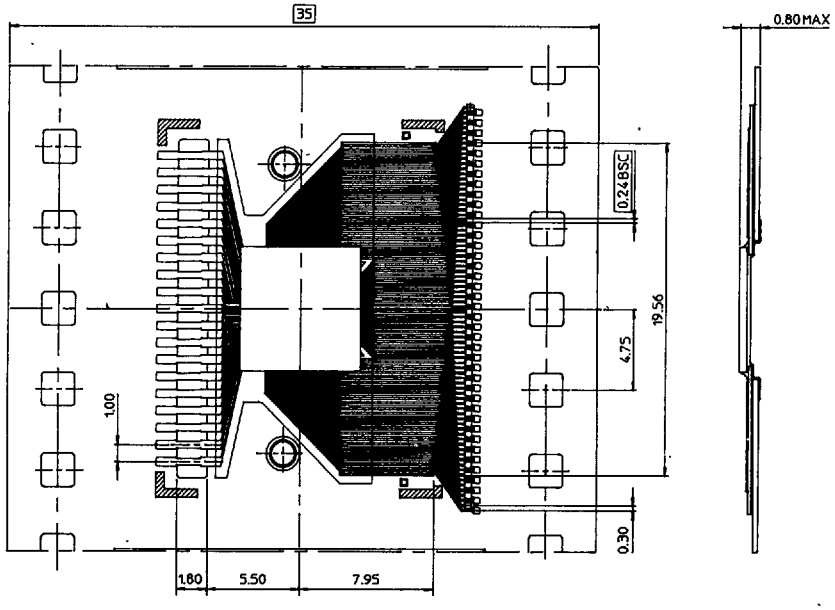
PACKAGE DIMENSIONS

Dimensions in Milimeters

98-STAB-35mm



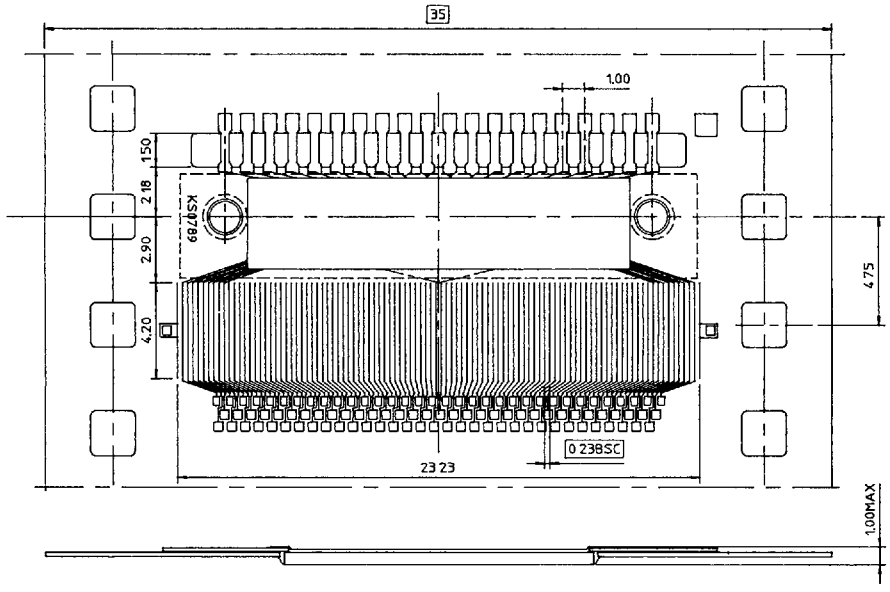
99-TAB-35mm



PACKAGE DIMENSIONS

Dimensions in Milimeters

120-STAB-35mm



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