MOTOROLA

9-Bit Hold Register

Military 100E543

Product Preview

ELECTRICALLY TESTED PER:
100E543

The 100E543 is a 9-bit holding register, designed with byte-parity applications in mind. The 100E543 holds current data or loads new data, with the nine inputs D_0-D_8 accepting parallel input data.

The SEL (Select) input pin is used to switch between the two modes of operation –HOLD and LOAD. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

- 700 MHz Min. Operating Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

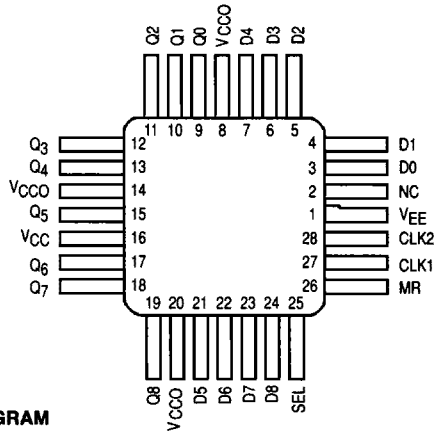
PACKAGE: NON-Compliant
QFP: X

PIN NAME

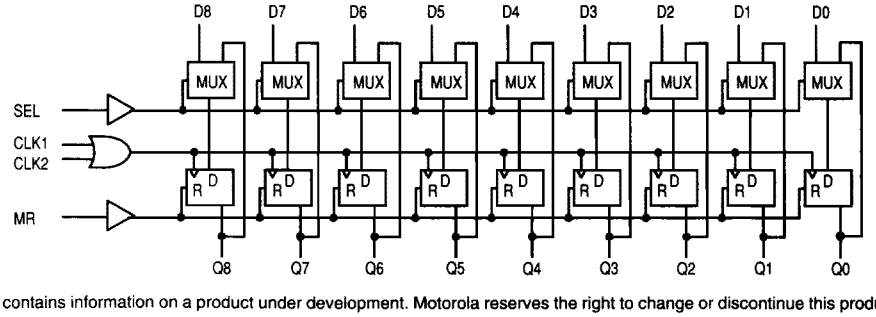
Pin	Function
D_0 - D_8	Parallel Data Inputs
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q_0 - Q_8	Data Outputs
NC	No Connection

Function Table

SEL	Mode
L	LOAD
H	HOLD



LOGIC DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		μA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		150		150		150	μA	
I_{EE}	Power Supply Current		145		165		145	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
f_{SHIFT}	Max. Toggle Frequency	700		700		700		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output								
	Clk	600	1000	600	1000	600	1000	ps	
	MR	600	1000	600	1000	600	1000	ps	
t_S	Setup Time								
	D	50		50		50		ps	
	SEL	300		300		300		ps	
t_H	Hold Time								
	D	300		300		300		ps	
	SEL	75		75		75		ps	
t_{RR}	Reset Recovery Time	900		900		900		ps	
t_{PW}	Minimum Pulse Width								
	Clk, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	75		75		75		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	300	800	300	800	300	800	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.