Bt459

150 MHz Monolithic CMOS 256 x 24 Color Palette RAMDAC™

Distinguishing Features

- 150, 135, 110, 80 MHz Operation
- 1:1, 4:1, or 5:1 Multiplexed Pixel Ports
- 256 x 24 Color Palette RAM
- 16 x 24 Overlay Color Palette
- 1x to 16x Integer Zoom Support
- 1, 2, 4, or 8 Bits per Pixel
- Frame Buffer Interleave Support
- Pixel Panning Support
- On-Chip User-Definable 64 x 64 Cursor
- Programmable Setup (0 or 7.5 IRE)
- X Windows Support for Overlays/ Cursor
- 132-pin PGA or PQFP Package

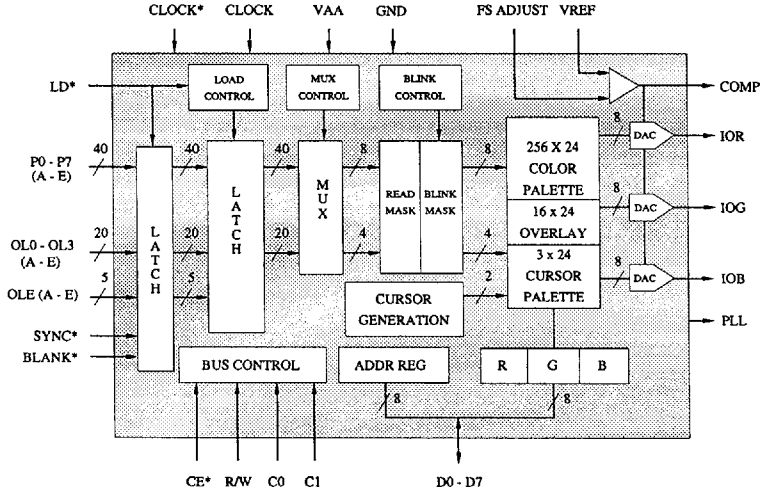
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439
- Bt460, Bt462, Bt468

Functional Block Diagram



Product Description

The Bt459 triple 8-bit RAMDAC is designed specifically for high-performance, high-resolution color graphics. The multiple pixel ports and internal multiplexing enable TTL-compatible interfacing to the frame buffer, while maintaining the 135 MHz video data rates required for sophisticated color graphics.

On-chip features include a 256 x 24 color palette RAM, 16 x 24 overlay color palette RAM, programmable 1:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), pixel panning support, 1x to 16x integer zoom support, and independent cursor generation.

Pixel data may be input as 1, 2, 4, or 8 bits per pixel. Overlay and cursor information may optionally be enabled on a pixel-by-pixel basis for X Windows hardware support.

The Bt459 has an on-chip three-color 64 x 64 pixel cursor and a three-color full-screen (or full- window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with subpixel resolution.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt459 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As detailed in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 16-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

To write color data, the MPU loads the address register with the address of the primary color palette RAM, overlay RAM, or cursor color register location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, overlay RAM, or cursor color registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles when it reads color data.

When the MPU is accessing the color palette RAM, overlay RAM, or cursor color registers, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU. ADDR12–ADDR15 are always a logical zero. ADDR0 and ADDR8 correspond to D0.

The only time the address register resets to $0000 is after accessing location $0FFF (due to wraparound).

Although the color palette RAM, overlay RAM, and cursor color registers are dual ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

ADDR0–15	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–15)
$0000–$00FF	10	reserved
$0100	10	overlay color 0 (Note 1)
:	10	:
$010F	10	overlay color 15 (Note 1)
$0181	10	cursor color register 1 (Note 1)
:	:	cursor color register 2 (Note 1)
$0183	10	cursor color register 3 (Note 1)
$0200	10	ID register ($4A)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0204	10	pixel read mask register
$0205	10	reserved ($00)
$0206	10	pixel blink mask register
$0207	10	reserved ($00)
$0208	10	overlay read mask register
$0209	10	overlay blink mask register
$020A	10	interleave register
$020B	10	test register
$020C	10	red signature register
$020D	10	green signature register
$020E	10	blue signature register
$0220	10	revision register
$0300	10	cursor command register
$0301	10	cursor (x) low register
$0302	10	cursor (x) high register
$0303	10	cursor (y) low register
$0304	10	cursor (y) high register
$0305	10	window (x) low
$0306	10	window (x) high
$0307	10	window (y) low
$0308	10	window (y) high
$0309	10	window width low register
$030A	10	window width high register
$030B	10	window height low register
$030C	10	window height high register
$0400–$07FF	10	cursor RAM
$0000–$00FF	11	color palette RAM (Note 1)

Note 1: Indicates a requirement of three read/write cycles—RGB.

Table 1. Address Register (ADDR) Operation.

Circuit Description *(continued)*

The control registers and cursor RAM are also accessed through the address register in conjunction with the C0 and C1 inputs, as specified in Table 1. All control registers may be written to or read by the MPU at any time. When accessing the control registers and cursor RAM, the address register increments following a read or write cycle.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt459.

Bt459 Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or the overlay registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles when it reads color data.

This mode is useful if only an 8-bit data bus is available. Each Bt459 is programmed to be a red, green, or blue RAMDAC and will respond only to the assigned color read or write cycle. In this application, the Bt459s share a common 8-bit data bus. The CE* inputs of all three Bt459s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU.

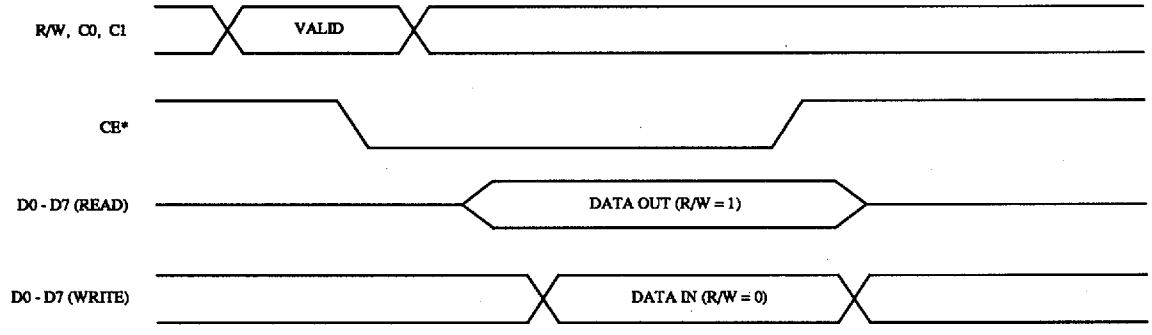


Figure 1. MPU Read/Write Timing.

Circuit Description *(continued)*

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt459 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for either one, four, or five consecutive pixels, are latched into the device. With this configuration, the sync and blank timing will be recognized only with one, four, or five pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

For 4:1 or 5:1 input multiplexing, the Bt459 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, followed by the {C} inputs, etc., until all four or five pixels have been output. At this point, the cycle repeats. In the 1:1 input multiplexing mode, the {B}, {C}, {D}, and {E} inputs are ignored.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase shifted in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by 4 or 5, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one but not more than three clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

If 1:1 multiplexing is specified, LD* is also used to clock the Bt459 (at a maximum of 50 MHz). The rising edge of LD* still latches the P0–P7 {A}, OL0–OL3 {A}, OLE {A}, SYNC*, and BLANK* inputs. However, analog information is output following the rising edge of LD* rather than CLOCK. CLOCK must still run but is ignored.

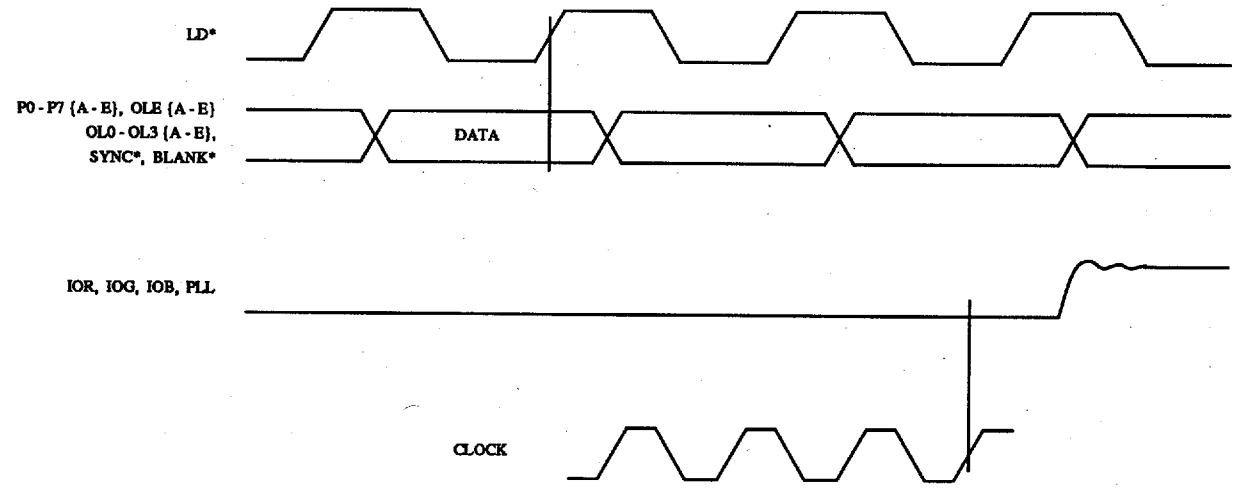


Figure 2. Video Input/Output Timing.

Circuit Description *(continued)*

Read and Blink Masking

Each clock cycle, 8 bits of color information (P0–P7) and 4 bits of overlay information (OL0–OL3) for each pixel are processed by the read mask, blink mask, and command registers. Through the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change caused by blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt459 monitors the BLANK* input to determine vertical retrace intervals (any BLANK* pulse longer than 256 LD* cycles).

The processed pixel data is used to select which color palette entry or overlay register is to provide color information. P0 is the LSB when the MPU is addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM.

The read and blink mask registers are not initialized. They must be initialized by the user after power-up for proper operation.

Pixel Panning

Panning is achieved through the delay of SYNC* and BLANK* by an additional one, two, three, or four clock cycles. To support pixel panning, command register_1 specifies the number of clock cycles to pan. Only the pixel inputs and underlays are panned—overlays and cursors are not.

If 0 pixel panning is specified, pixel {A} is output first, followed by pixel {B}, followed by pixel {C}, etc., until all 4 or 5 pixels have been output. At this point, the cycle repeats (assuming the interleave select is pixel {A}).

If 1-pixel panning is specified, pixel {B} will be first, followed by pixel {C}, followed by pixel {D}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval and will not be seen on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B}, {C}, {D}, and {E} will be output during the blanking interval and will not be seen on the display screen.

The process is similar for panning by 2, 3, or 4 pixels. When a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt459 during the first LD* cycle that BLANK* is a logical zero.

In the 1:1 multiplex mode, 0-pixel panning should be specified.

The cursor position does not change relative to the edge of the display screen during panning.

Pixel Zoom

The Bt459 supports 1x to 16x integer zoom through pixel replication. Only the P0–P7 inputs are zoomed.

If 2x zooming is specified, the {A} pixel is output for two clock cycles, followed by the {B} pixel for two clock cycles, followed by the {C} pixel for two clock cycles, etc. The 3x zooming is similar, except each pixel is output for three clock cycles. For 1:1 multiplexing, only the {A} pixel is output.

LD* must be the pixel clock (1:1 multiplex mode), or one fourth or one fifth the CLOCK rate. Regardless of the zoom factor, P0–P7 data is latched every LD* cycle.

During 2x zoom, new P0–P7 data must be presented every two LD* cycles. During 3x zoom, new P0–P7 data must be presented every three LD* cycles. The pixel data must be held at the P0–P7 {A–E} inputs for the appropriate number of LD* cycles until new P0–P7 information is needed. OL0–OL3, OLE, SYNC*, and BLANK* information are still latched every LD* cycle.

In the 1:1 multiplex mode, 1x zoom must be specified. Also, while in the block mode (1, 2, or 4 bits per pixel), 1x zoom must be specified. Figure 3 illustrates the zoom timing.

Block Mode Operation

The Bt459 supports loading of pixel data at 1, 2, 4, or 8 bits per pixel. Only the P0–P7 inputs are affected.

LD* must be the pixel clock (1:1 multiplex mode), or one fourth or one fifth the CLOCK rate. Regardless of the block mode, P0–P7 data is latched every LD* cycle.

For 8 bits per pixel, new P0–P7 information must be presented every LD* cycle. For 4 bits per pixel, new P0–P7 information must be presented every two LD* cycles. For 2 bits per pixel, new P0–P7 information must be presented every four LD* cycles. For 1 bit per pixel, new P0–P7 information must be presented every eight LD* cycles.

The pixel data must be held at the P0–P7 inputs for the appropriate number of LD* cycles until new P0–P7 information is needed. OL0–OL3, OLE, SYNC* and BLANK* information are still latched every LD* cycle.

Figure 4 illustrates the block mode timing (4 bits per pixel).

Tables 2 and 3 detail the block mode operation and address of the color palette RAM.

In the 1:1 multiplex mode, 8 bits per pixel must be specified. Also, for block modes other than 8 bits per pixel, a 0-pixel interleave must be selected.

Circuit Description *(continued)*

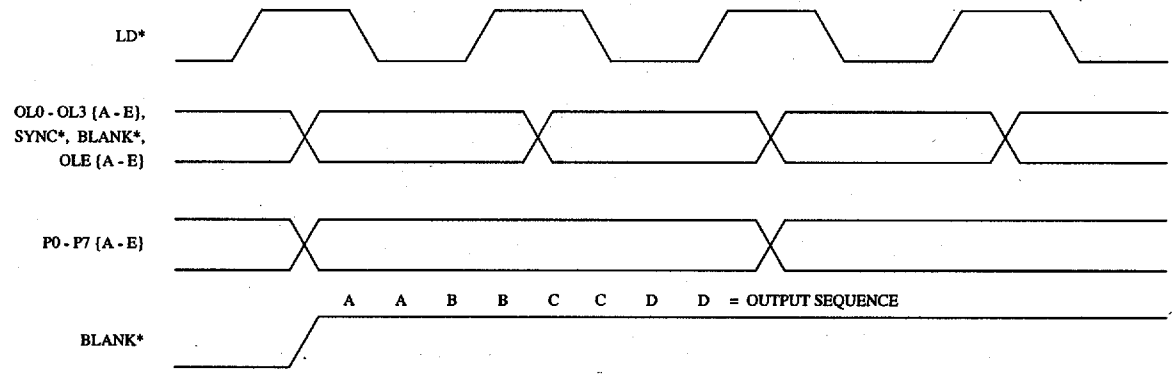


Figure 3. Zoom Input Timing (8 Bits per Pixel, 2x Zoom).

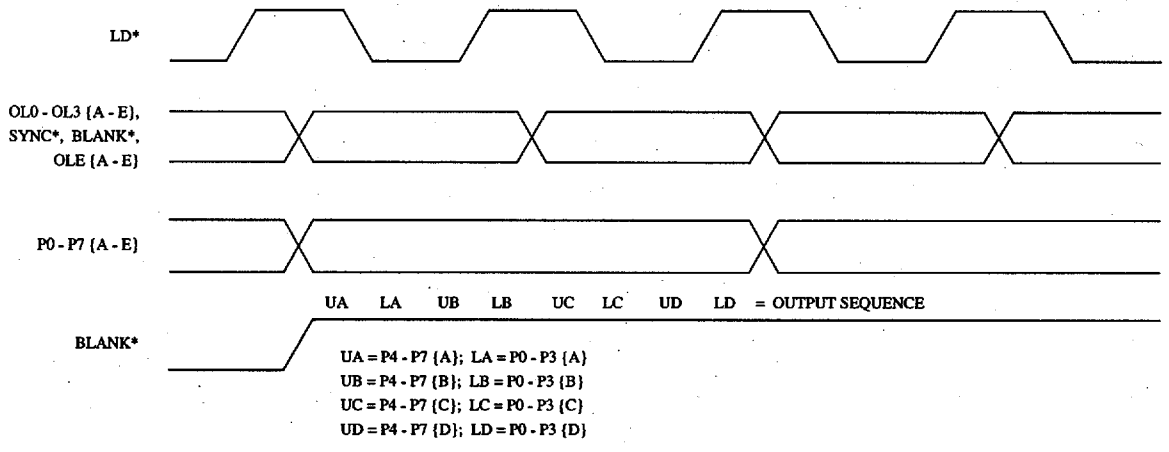


Figure 4. Block Mode Input Timing (4 Bits per Pixel, 1x Zoom, 4:1 Multiplexing).

Circuit Description *(continued)*

Bits per Pixel	Pixels per LD* (1:1 muxing)	Pixels per LD* (4:1 muxing)	Pixels per LD* (5:1 muxing)	Colors Displayed
1	8	32	40	2
2	N/A	16	20	4
4	N/A	8	10	16
8	N/A	4	5	256

Table 2. Block Mode Operation.

1 Bit per Pixel (RA1–RA7 = 0) RA0 =	2 Bits per Pixel (RA2–RA7 = 0) RA1, RA0 =	4 Bits per Pixel (RA4–RA7 = 0) RA3–RA0 =	8 Bits per Pixel RA7–RA0 =
P7A	P7A, P6A	P7A, P6A, P5A, P4A	P7A, P6A, P5A, P4A, P3A, P2A, P1A, P0A
P6A	P5A, P4A	P3A, P2A, P1A, P0A	P7B, P6B, P5B, P4B, P3B, P2B, P1B, P0B (4:1)
:	P3A, P2A	P7B, P6B, P5B, P4B (4:1)	P7C, P6C, P5C, P4C, P3C, P2C, P1C, P0C (4:1)
P0A	P1A, P0A	P3B, P2B, P1B, P0B (4:1)	P7D, P6D, P5D, P4D, P3D, P2D, P1D, P0D (4:1)
P7B (4:1)	P7B, P6B (4:1)	P7C, P6C, P5C, P4C (4:1)	P7E, P6E, P5E, P4E, P3E, P2E, P1E, P0E (5:1)
P6B (4:1)	P5B, P4B (4:1)	P3C, P2C, P1C, P0C (4:1)	
:	P3B, P2B (4:1)	P7D, P6D, P5D, P4D (4:1)	
P0B (4:1)	P1B, P0B (4:1)	P3D, P2D, P1D, P0D (4:1)	
P7C (4:1)	P7C, P6C (4:1)	P7E, P6E, P5E, P4E (5:1)	
P6C (4:1)	P5C, P4C (4:1)	P3E, P2E, P1E, P0E (5:1)	
:	P3C, P2C (4:1)		
P0C (4:1)	P1C, P0C (4:1)		
P7D (4:1)	P7D, P6D (4:1)		
P6D (4:1)	P5D, P4D (4:1)		
:	P3D, P2D (4:1)		
P0D (4:1)	P1D, P0D (4:1)		
P7E (5:1)	P7E, P6E (5:1)		
P6E (5:1)	P5E, P4E (5:1)		
:	P3E, P2E (5:1)		
P0E (5:1)	P1E, P0E (5:1)		

Each line represents one pixel clock cycle. A column represents one LD* cycle loading new P0–P7 data. All entries with "4:1" descriptor are also valid for 5:1 mode.

Table 3. Block Mode Operation (RA = Color Palette RAM Address).

Circuit Description *(continued)*

On-Chip Cursor Operation

The Bt459 has an on-chip, three-color, 64 x 64 pixel user-definable cursor. The cursor operates only with a noninterlaced video system.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. The cursor is positioned through the cursor (x,y) register. The Bt459 expects (x) to increase to the right and (y) to increase down, as displayed on the screen. The cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking. (See Figure 5.)

Three-Color 64 x 64 Cursor

The 64 x 64 x 2 cursor RAM provides 2 bits of cursor information every clock cycle during the 64 x 64 cursor window, selecting the appropriate cursor color register as follows:

plane1	plane0	cursor color
0	0	cursor not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

A (0,0) enables the color palette RAM and overlay RAM to be selected as normal. Each plane of cursor information may also be independently enabled or disabled for display via the cursor command register (bits CR47 and CR46).

The cursor pattern and color may be changed by changing the contents of the cursor RAM.

The cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the thirty-first column of the 64 x 64 array (assuming the columns start with 0 for the left-most pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the thirty-first row of the 64 x 64 array (assuming the rows start with 0 for the top-most pixel and increment to 63).

Cross Hair Cursor

The three-color cross hair cursor is also positioned through the cursor (x,y) register. The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than 1 pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, the cursor command register (bits CR45 and CR44) specifies the color of the cross hair cursor.

CR45	CR44	cross hair color
0	0	cross hair not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

The cross hair cursor is displayed only within the cross hair window, which is specified by the window (x,y), window width, and window height registers. Since the cursor (x,y) register must specify a point within the window boundaries, *the software must ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.*

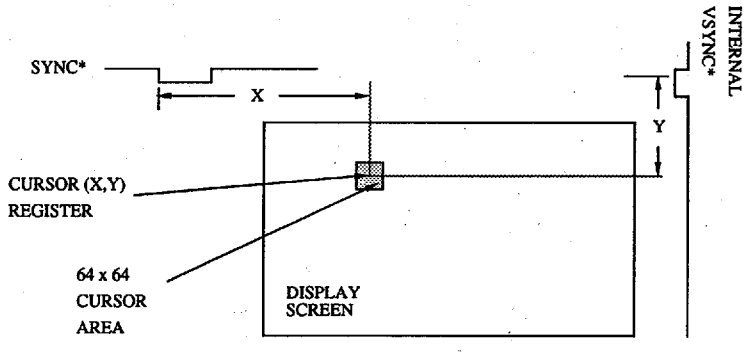


Figure 5. Cursor Positioning.

Circuit Description *(continued)*

If a full-screen cross hair cursor is desired, the window (x,y) registers should contain $0000, and the window width and height registers should contain $0FFF.

Again, the cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking. (See Figure 6.)

Dual-Cursor Positioning

Both the user-definable cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors.

The cursor (x,y) register specifies the location of bit (31, 31) of the cursor RAM. As the user-definable cursor contains an even number of pixels in the horizontal and vertical direction, it will be 1 pixel off from being truly centered about the cross hair cursor.

Figure 7 illustrates dual-cursor display.

In the 64 x 64 pixel area in which the user-definable cursor is displayed, each plane of the 64 x 64 cursor may be individually logically ORed or exclusive-ORed with the cross hair cursor information. Thus, the color of the displayed cursor will depend on the cursor pattern, whether it is logically ORed or XORed, and the individual cursor display enable and blink enable bits.

Figure 8 shows the equivalent cursor generation circuitry.

X Windows Cursor Mode

In the X Windows mode, plane1 of the cursor RAM is a cursor display enable and plane0 of the cursor RAM selects either cursor color 2 or 3. The operation is as follows:

plane1	plane0	Selection
0	0	no cursor
0	1	no cursor
1	0	cursor color 2
1	1	cursor color 3

Figure 12 in the Internal Registers section shows the organization of the cursor RAM while in the X Windows mode.

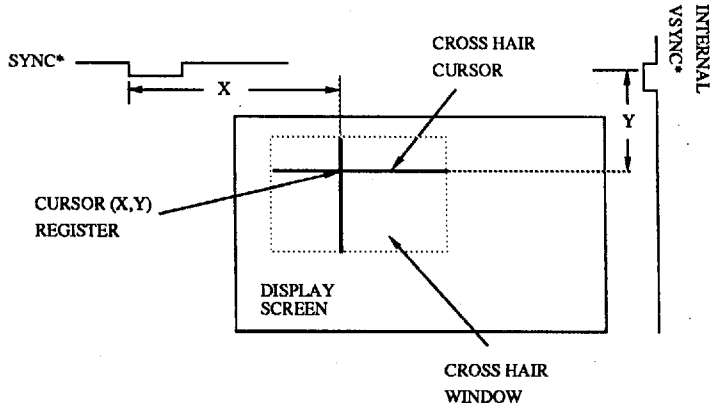


Figure 6. Cross Hair Cursor Positioning.

Circuit Description *(continued)*

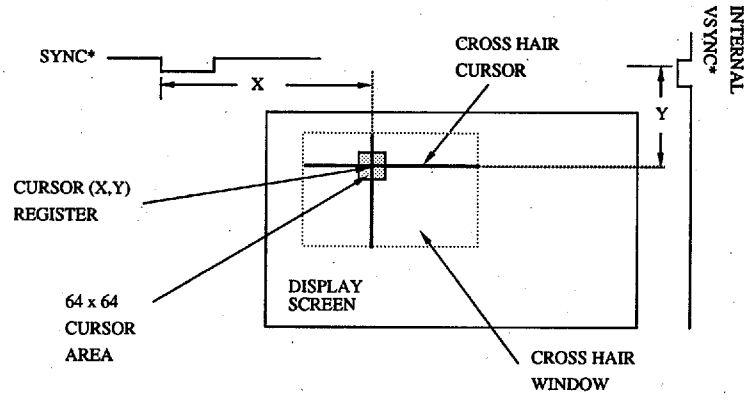


Figure 7. Dual-Cursor Positioning.

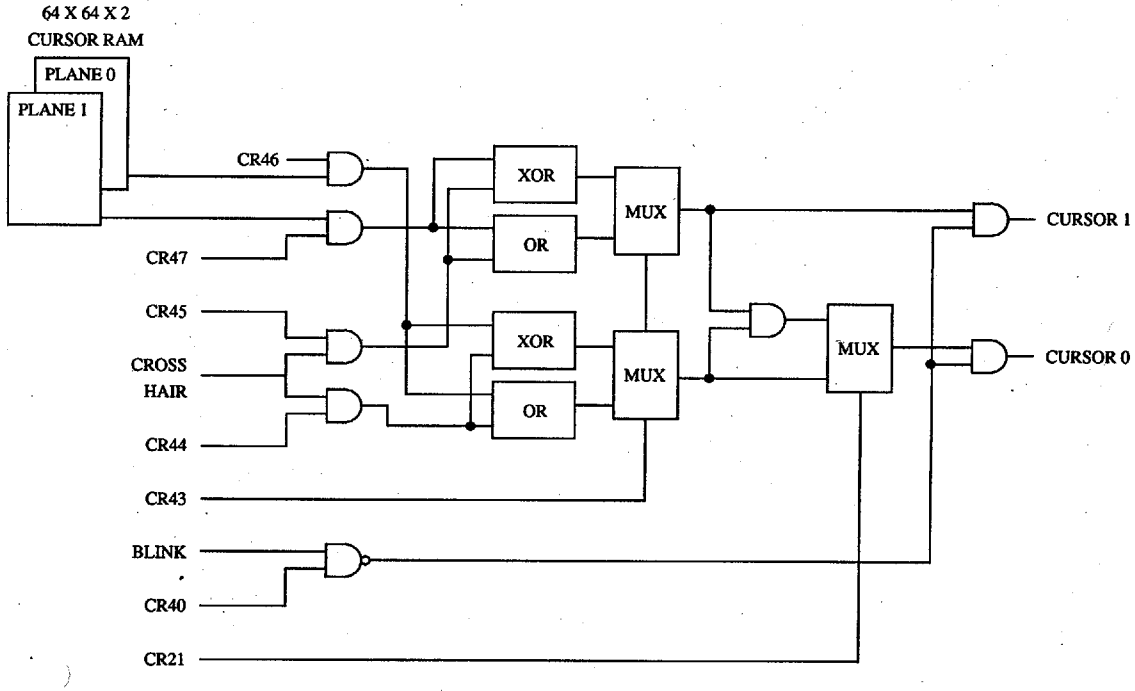


Figure 8. Cursor Control Circuitry.

Circuit Description *(continued)*

Overlay/Underlay Operation

The overlay inputs (OL0–OL3 and OLE) may operate in three modes: normal overlays, X Windows overlays, or an underlay, as specified in Tables 4 and 5.

Overlay and underlay information may be displayed on a pixel basis. Overlays and underlay may both be used. If X Windows overlays are used, the underlay is not available.

The priority of display operation is:

1. Cursor
2. Overlays
3. Pixel Data
4. Underlays

The Bt459 must be reset to an eight-cycle pipeline delay for proper cursor pixel alignment.

Cursor1, Cursor0	CR30	CR22	OLE	CR05	OL0–OL3	P0–P7	Addressed by frame buffer	Overlay Mode
11	x	x	x	x	$x	$xx	cursor color 3	
10	x	x	x	x	$x	$xx	cursor color 2	
01	x	x	x	x	$x	$xx	cursor color 1	
00	0	0	x	x	$F	$xx	overlay color 15	normal
:	:	:	:	:	:	:	:	
00	0	0	x	x	$1	$xx	overlay color 1	
00	0	0	x	1	$0	$xx	overlay color 0	
00	0	0	x	0	$0	$00	RAM location $00	
00	0	0	x	0	$0	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	0	0	x	0	$0	$FF	RAM location $FF	
00	x	1	1	x	$F	$xx	overlay color 15	X Windows
:	:	:	:	:	:	:	:	
00	x	1	1	x	$1	$xx	overlay color 1	
00	x	1	1	x	$0	$xx	overlay color 0	
00	x	1	0	0	$x	$00	RAM location $00	
00	x	1	0	0	$x	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	x	1	0	0	$x	$FF	RAM location $FF	
00	1	0	x	x	$F	$xx	overlay color 15	underlay
:	:	:	:	:	:	:	:	
00	1	0	x	x	$1	$xx	overlay color 1	
00	1	0	1	x	$0	$00	overlay color 0 (underlay)	
00	1	0	0	0	$x	$00	RAM location $00	
00	1	0	x	0	$x	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	1	0	x	0	$x	$FF	RAM location $FF	

Figure 8 shows generation of Cursor1 and Cursor0 control bits.

Table 4. Palette and Overlay Select Truth Table.

Circuit Description *(continued)*

In normal overlay mode, the overlay enable inputs OLE {A–E} are ignored. Typically, only 15 overlays are available. Graphics information (P0–P7) is displayed only when no overlay information is present (OL0–OL3 = 0000).

In the X Windows overlay mode, the overlay enable inputs specify whether overlay information is present (OLE = 1) or not (OLE = 0). If OLE = 1, overlay information is displayed as determined by OL0–OL3. If OLE = 0, the OL0–OL3 inputs are ignored and P0–P7 pixel data is displayed.

In the underlay mode (CR30 = 1), if OLE = 0, pixel data is displayed. If OLE = 1, the underlay is displayed if P0–P7 = 0; if P0–P7 ≠ 0, pixel data is displayed. Overlay color 0 is used for underlay color information.

	P0–P7 Pixel Inputs						
	1:1 Mux	Block Mode	Interleave	Panning	Zooming	Overlays	Underlay
Block Mode	no	-	yes	yes	n/s	n/a	n/a
Interleave	n/s	yes	-	yes	yes	yes	yes
Panning	n/s	n/s	yes	-	yes	n/a	yes
Zooming	n/s	n/s	yes	yes	-	n/a	n/a
Overlays	yes	yes	yes	n/a	n/a	-	yes
Underlay	yes	yes	yes	yes	n/a	yes	-
Cursor	n/a	n/a	n/a	n/a	n/a	n/a	n/a

yes: fully functional together.
n/s: functions not supported together.
n/a: functions operate together, but do not affect each other.

Table 5. Features and Function Compatibility Table.

Circuit Description *(continued)*

Video Generation

Every clock cycle, the selected 24 bits of color information are presented to the three 8-bit D/A converters.

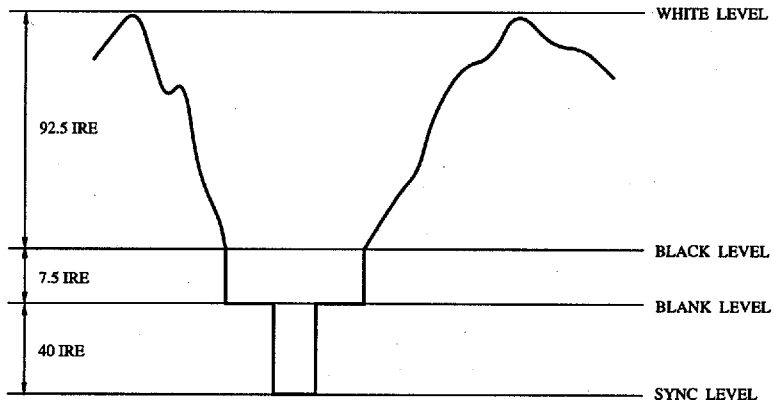
The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 9 and 10. Command Register 2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated and whether sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 6 and 7 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt459 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Circuit Description *(continued)*

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 523 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 9. Composite Video Output Waveform (SETUP = 7.5 IRE).

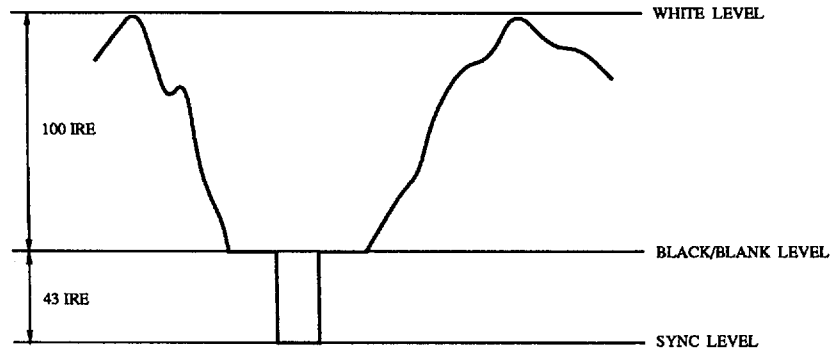
Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET =523 and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*

RED, BLUE		GREEN	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 495 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 10. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 495 Ω and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 7. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07, CR06 — Multiplex select

(00) reserved
(01) 4:1 multiplexing
(10) 1:1 multiplexing
(11) 5:1 multiplexing

These bits specify whether 1:1, 4:1, or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be one fourth the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one fifth the CLOCK rate. If 1:1 is specified, the {B}, {C}, {D}, and {E} inputs are ignored.

In the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running.

It is possible to reset the pipeline delay of the Bt459 to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt459 must again be reset to a fixed pipeline delay.

CR05 — Overlay 0 enable

(0) use color palette RAM
(1) use overlay color 0

When in the normal overlay mode, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information when the overlay inputs are $0. See Table 4.

CR04 — reserved (logical zero)

CR03, CR02 — Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These 2 bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off). The counters that determine the blink rate are reset when command register_0 is written to.

CR01, CR00 — Block mode

(00) 8 bits per pixel
(01) 4 bits per pixel
(10) 2 bits per pixel
(11) 1 bit per pixel

These bits specify whether the pixel data is input as 1, 2, 4, or 8 bits per pixel. Only the P0–P7 inputs are affected.

Internal Registers *(continued)*

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17–CR15 Pan select

(000) 0 pixels {pixel A}
(001) 1 pixel {pixel B}
(010) 2 pixels {pixel C}
(011) 3 pixels {pixel D}
(100) 4 pixels {pixel E}
(101) reserved
(110) reserved
(111) reserved

These bits specify the number of pixels to be panned. These bits are typically modified only during the vertical retrace interval, and should be set to 000 in the 1:1 multiplex mode. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, {pixel C} indicates pixel C will be output first, etc.

Only pixel and underlay information is panned. Overlay and cursor information is not panned.

CR14 reserved (logical zero)

In the 1:1 multiplex mode, 0 pixels should be specified.

CR13–CR10 Zoom factor

(0000) 1x
(0001) 2x
:
(1111) 16x

These bits specify the amount of zooming to implement. For 2x zoom, pixel {A} is output for two clock cycles, followed by pixel {B} for two clock cycles, followed by pixel {C} for two clock cycles, etc. For 3x zoom, pixel {A} is output for three clock cycles, and so on.

In the 1:1 multiplex mode, only the {A} pixels are output, and 1x zoom should be selected.

Only P0–P7 are zoomed.

Internal Registers *(continued)*

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt459 with three write cycles (red, green, and blue), and color data is output with three read cycles (red, green, and blue). Modes (01), (10), and (11) enable the Bt459 to emulate a single-channel RAMDAC using only the green channel. The Bt459 expects color data to be input and output with (red, green, blue) cycles. The exact value indicates during which *one* of the three color cycles it is to load or output color information. The value is loaded into or read from the green color palette RAM.
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses SYNC* or BLANK* to generate PLL information.
CR22	X Windows overlay select (0) normal overlays (1) X Windows overlays	This bit specifies whether the overlays are to operate normally (logical zero) or in an X Windows environment (logical one).
CR21	X Windows cursor select (0) normal cursor (1) X Windows cursor	This bit specifies whether the cursor is to operate normally (logical zero) or in an X Windows-compatible mode (logical one).
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers *(continued)*

Interleave Register

This register may be written to or read by the MPU at any time and is not initialized. CR30 corresponds to data bus bit D0. The interleave register is for support of frame buffer systems configured for interleave operation.

CR37–CR35 Interleave select

(000) 0 pixels
(001) 1 pixel
(010) 2 pixels
(011) 3 pixels
(100) 4 pixels
(101) reserved
(110) reserved
(111) reserved

These bits specify the order in which the pixels are to be output, as listed in Table 8. The order is repeated every LD* cycle for a given scan line. Thus, if the output sequence is DABC, it is that sequence for all pixels on that scan line.

The phrase "repeats every x" in Table 8 means that the output sequence repeats every x scan lines. Thus, for 4:1 multiplexing and a 1-pixel interleave select, ABCD would be repeated every fourth scan line.

When the Bt459 is in the 1:1 input multiplex mode, a value of 0 pixels(000) must be specified.

CR34–CR32 First pixel select

(000) pixel {A}
(001) pixel {B}
(010) pixel {C}
(011) pixel {D}
(100) pixel {E}
(101) reserved
(110) reserved
(111) reserved

These bits are used to support panning in the Y direction with an interleaved frame buffer. Because of the interleave capability, the value of the first pixel must be specified on the first scan line following a vertical retrace. The pixel {E} selection is only used in the 5:1 multiplex mode.

These bits are ignored when the Bt459 is in the 1:1 multiplex mode.

CR31 Overlay interleave enable

(0) interleaving disabled
(1) interleave enabled

This bit specifies whether OL0–OL3 and OLE are to be interleaved. If interleaving is enabled, the interleave factor and first pixel selection are the same as that for P0–P7. If interleaving is disabled, pixel {A} is output first, and no interleaving occurs.

CR30 Underlay enable

(0) underlay disabled
(1) underlay enabled

If command bit CR22 is a logical zero, this bit enables or disables the underlay display. If CR22 is a logical one, this bit is ignored.

If the underlay is enabled (and CR22 is a logical zero), the OLE inputs function as follows: If OLE = 0, P0–P7 data is displayed. If OLE = 1, the underlay is displayed if P0–P7 = 0, if P0–P7 ≠ 0, normal pixel data is displayed. The underlay uses overlay color 0 to provide underlay color information.

Internal Registers *(continued)*

Interleave Register (continued)

	5:1 multiplexing		4:1 multiplexing	
interleave select	**output sequence**	**scan line number**	**output sequence**	**scan line number**
0	ABCDE	each line	ABCD	each line
1	ABCDE BCDEA CDEAB DEABC EABCD	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD BCDA CDAB DABC	n n + 1 n + 2 n + 3 (repeats every 4)
2	ABCDE CDEAB EABCD BCDEA DEABC	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD CDAB ABCD CDAB	n n + 1 n + 2 n + 3 (repeats every 2)
3	ABCDE DEABC BCDEA EABCD CDEAB	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD DABC CDAB BCDA	n n + 1 n + 2 n + 3 (repeats every 4)
4	ABCDE EABCD DEABC CDEAB BCDEA	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	invalid	invalid

Table 8. Interleave Operation (First Pixel Select = Pixel A).

Internal Registers *(continued)*

Interleave Zoom Enable

If zooming while interleaving, the IZE* input pin indicates when to change the interleave sequence.

For example, while interleaving with 3x zoom, the IZE* pin should be a logical zero during the blanking interval of every third scan line (as shown in Figure 11). IZE* may be asserted coincident with the falling edge of BLANK* but must remain low at least 16 LD* cycles after the falling edge of BLANK*.

If zooming is not required (1x zoom), the IZE* should be a logical zero or be connected directly to GND.

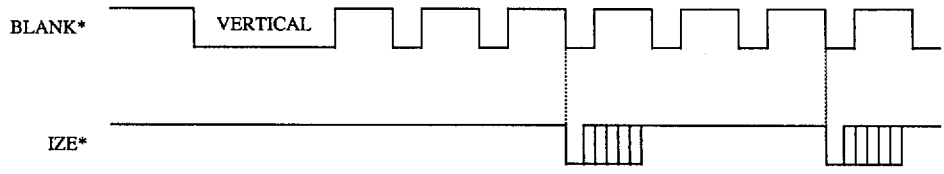


Figure 11. Interleave and Zoom Operation (3x Zoom Example).

Internal Registers *(continued)*

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt459, the value read by the MPU will be $4A. Data written to this register is ignored.

Pixel Read Mask Register

The 8-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P0.

Pixel Blink Mask Register

The 8-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. D0 corresponds to P0.

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–E}), and D3 corresponds to overlay plane 3 (OL3 {A–E}). Bits D0–D3 are logically ANDed with the corresponding overlay plane input. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register_0. D0 corresponds to overlay plane 0 (OL0 {A–E}), and D3 corresponds to overlay plane 3 (OL3 {A–E}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

Revision Register (Revision B only)

This 8-bit register is a read-only register, specifying the revision of the Bt459. The 4 most significant bits signify the revision letter B in hexidecimal form. The 4 least significant bits do not represent any value and should be ignored. Data written to this register is ignored.

Since the Revision A device does not have a revision register, address $0220 will contain the last data read to or written from the internal bus.

Internal Registers *(continued)*

Red, Green, and Blue Signature Registers

Signature Operation

These three 8-bit signature registers (one each for red, green, and blue) may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the three registers are concatenated and a 24-bit signature is acquired. The MPU may read from or write to the signature registers while BLANK* is a logical zero to load the seed value.

By loading a test display into the frame buffer, a deterministic value for the red, green, and blue signature registers will be read from these registers if all circuitry is working properly. The Application Information, Test Register section contains more information.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–E) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–E) is to be captured.

Internal Registers *(continued)*

Test Register

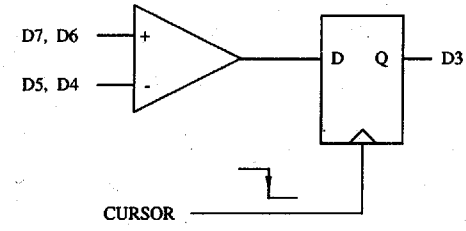
This 8-bit register is used to test the Bt459. If 1:1 pixel multiplexing is specified, signature analysis is performed on every pixel; if 4:1 pixel multiplexing is specified, signature analysis is performed on every fourth pixel; if 5:1 pixel multiplexing is specified, signature analysis is performed on every fifth pixel. D0–D2 are used for 4:1 and 5:1 multiplexing to specify whether to use the A, B, C, D, or E pixel inputs, as follows:

D2–D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0–D2 should select pixel A.

D3–D7 are used to compare the analog RGB outputs to each other and to a 150 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result



D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 150 mV reference	red > 150 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 150 mV reference	green > 150 mV	green < 145 mV

The above table lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The comparison result is strobed into D3 on the left edge of the 64 x 64 cursor area. The output levels of the DACs should be constant for 5 µs before the left edge of the cursor.

For normal operation, D3–D7 must be a logical zero.

Internal Registers *(continued)*

Cursor Command Register

This command register is used to control various cursor functions of the Bt459. It is not initialized, and may be written to or read by the MPU at any time. CR40 corresponds to data bus bit D0.

CR47	64 x 64 cursor plane1 display enable (0) disable plane1 (1) enable plane1	This bit specifies whether plane1 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR46	64 x 64 cursor plane0 display enable (0) disable plane0 (1) enable plane0	This bit specifies whether plane0 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR45	Cross hair cursor plane1 display enable (0) disable plane1 (1) enable plane1	This bit specifies whether plane1 of the cross hair cursor is to be displayed (logical one) or not (logical zero).
CR44	Cross hair cursor plane0 display enable (0) disable plane0 (1) enable plane0	This bit specifies whether plane0 of the cross hair cursor is to be displayed (logical one) or not (logical zero). Plane0 and plane1 contain the same information.
CR43	Cursor format (0) XOR (1) OR	If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.
CR42, CR41	Cross hair thickness (00) 1 pixel (01) 3 pixels (10) 5 pixels (11) 7 pixels	This bit specifies whether the vertical and horizontal thickness of the cross hair is 1, 3, 5, or 7 pixels. The segments are centered about the value in the cursor (x,y) register.
CR40	Cursor blink enable (0) blinking disabled (1) blinking enabled	This bit specifies whether the cursor is to blink (logical one) or not (logical zero). If both cursors are displayed, both will blink. The blink rate and duty cycle are as specified by command register_0.

Internal Registers *(continued)*

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window or the intersection of the cross hair cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). They are not initialized, and may be written to or read by the MPU at any time. The cursor position is not updated until the vertical retrace interval after CYHR has been written to by the MPU.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always a logical zero.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + H–P

where

P = 37 if 1:1 input multiplexing, 52 if 4:1 input multiplexing, 57 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of SYNC* to active video

Values from $0000 to $0FFF may be written into the cursor (x) register.

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V–32

where

V = number of scan lines from the second sync pulse during vertical blanking to active video

Values from $0FC0 (–64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used in situations where V < 32, and the cursor must be moved off the top of the screen.

Internal Registers *(continued)*

Window (x,y) Registers

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the window (x) low register (WXLR) and the window (x) high register (WXHR); the window (y) register is made up of the window (y) low register (WYLR) and the window (y) high register (WYHR). They are not initialized, and may be written to or read by the MPU at any time. The window position is not updated until the vertical retrace interval after WYHR has been written to by the MPU. WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4–D7 of WXHR and WYHR are always a logical zero.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + H–P

where

P = 5 if 1:1 input multiplexing, 20 if 4:1 input multiplexing, 25 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of HSYNC* to active video

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where

V = number of scan lines from the second sync pulse during vertical blanking to active video

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full-screen cross hair is implemented by loading the window (x,y) registers with $0000, and the window width and height registers with $0FFF.

Internal Registers *(continued)*

Window Width and Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window width register is made up of the window width low register (WWLR) and the window width high register (WWHR); the window height register is made up of the window height low register (WHLR) and the window height high register (WHHR). They are not initialized, and may be written to or read by the MPU at any time. The window width and height are not updated until the vertical retrace interval after WHHR has been written to by the MPU.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window height register. Bits D4–D7 of WWHR and WHHR are always a logical zero.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 2, 8, or 10 pixels more than the value specified by the window width register, depending on whether 1:1, 4:1, or 5:1 input multiplexing is specified. The actual window height is 2 pixels more than the value specified by the window height register. Therefore, the minimum window width is 2, 8, or 10 pixels for 1:1, 4:1, and 5:1 multiplexing, respectively. The minimum window height is 2 pixels.

Values from $0000 to $0FFF may be written to the window width and height registers.

Internal Registers *(continued)*

Cursor RAM

This 64 x 64 x 2 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window and is not initialized.

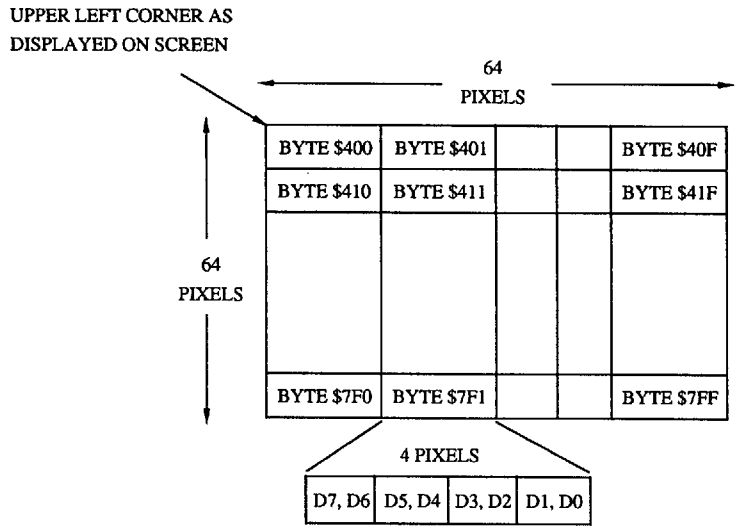
For Revision A, the cursor RAM should not be written to by the MPU during the horizontal sync time and for the two LD* cycles after the end of the horizontal sync. The cursor RAM may otherwise be written to or read by the MPU at any time without contention. If writing to the cursor RAM asynchronously to horizontal sync, it is recommended that the user position the cursor offscreen in the Y direction [i.e., write to the cursor (y) registers and wait for the vertical sync interval to move the cursor offscreen], write to the cursor RAM, then reposition the cursor back to the original position. An alternative is to perform a write-then-read sequence, and if the correct cursor RAM data was not written, perform another write then read sequence. Since the contention occurs only during horizontal sync at the Y locations coincident with the cursor, the second write/read sequence bypasses the window of time when cursor RAM is in contention.

For Revision B, cursor contention has been eliminated. The cursor RAM may be written to or read by the MPU at any time without contention.

During MPU accesses to the cursor RAM, the address register is used to address the cursor RAM. Figure 12 illustrates the internal format of the cursor RAM as it appears on the display screen. Addressing starts at location $400 as specified in Table 1.

In the X Windows mode, plane1 serves as a cursor display enable while plane0 selects one of two cursor colors (if enabled).

In both modes of operation, plane1 = D7, D5, D3, D1; and plane0 = D6, D4, D2, D0.



Normal Mode:

00 = color palette or overlay RAM
01 = cursor color 1
10 = cursor color 2
11 = cursor color 3

X-Windows Mode:

00 = color palette or overlay RAM
01 = color palette or overlay RAM
10 = cursor color 2
11 = cursor color 3

Figure 12. Cursor RAM as Displayed on the Screen.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as specified in Tables 6 and 7. BLANK* is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 9 and 10). SYNC* does not override any other control or data input, as shown in Tables 6 and 7; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P7 {A–E}, OL0–OL3 {A–E}, OLE {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is the output clock (1:1 multiplex mode) or while LD* is one fourth or one fifth of CLOCK, LD* may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.
P0–P7 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information (see Table 4). Either 1, 4, or 5 consecutive pixels (up to 8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Typically, the {A} pixel is output first, followed by the {B} pixel, followed by the {C} pixel, etc., until all pixels (1, 4, or 5) have been output, at which point the cycle repeats.
OL0– OL3 {A–E}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD* and, in conjunction with CR05 in command register_0, specify which palette is to be used for color information, as detailed in Table 4. When the overlay palette RAM is being accessed, the P0–P7 {A–E} inputs are ignored. Overlay information (up to 4 bits per pixel) for either 1, 4, or 5 consecutive pixels is input through this port. Unused inputs should be connected to GND.
OLE {A–E}	Overlay enable inputs (TTL compatible). In the X Windows mode for overlays, a logical one indicates overlay information is to be displayed. A logical zero indicates P0–P7 information is to be displayed. In the normal mode for overlays, these inputs are ignored. They are latched on the rising edge of LD*. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 13). All outputs, whether used or not, should have the same output load.
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt459s to be synchronized with subpixel resolution when used with an external PLL. A logical one for SYNC* or BLANK* (as specified by CR23 in command register_2) results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If subpixel synchronization of multiple devices is not required, this output should be connected to GND either directly or through a resistor of up to 150 Ω.
IZE*	Interleave zoom enable input (TTL compatible). This input should be a logical zero for a minimum of 16 LD* cycles after the falling edge of BLANK* during scan lines that require an interleave shift. If zoom while interleaving is not supported, this pin may be connected directly to GND.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions *(continued)*

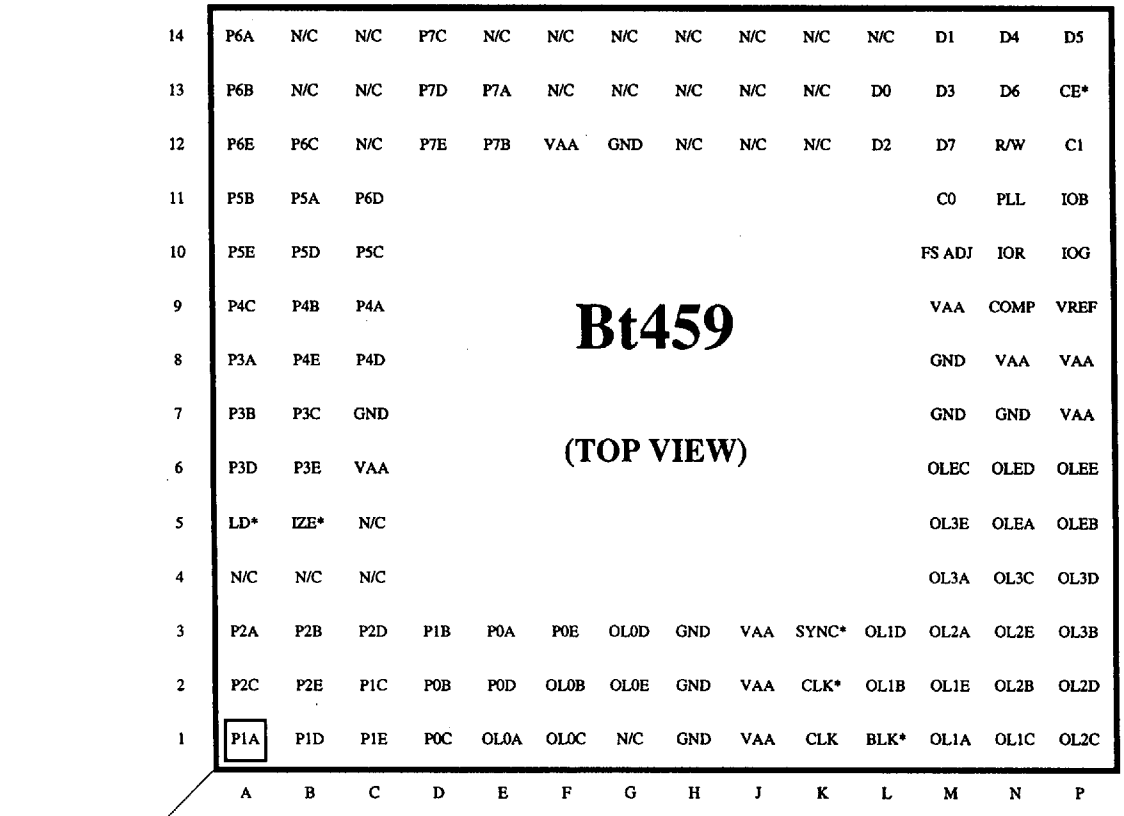
Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 13). When the capacitor is connected to VAA rather than to GND, the highest possible power supply noise rejection is provided. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. *The PC Board Layout Considerations section contains critical layout criteria.*
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 13). The IRE relationships in Figures 9 and 10 are maintained regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = K1 * VREF (V) / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω) where K1 and K2 are defined as:
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 13, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 13. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as specified in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Setup	IOG	IOR, IOB
7.5 IRE	K1 = 11,294	K2 = 8,067
0 IRE	K1 = 10,684	K2 = 7,457

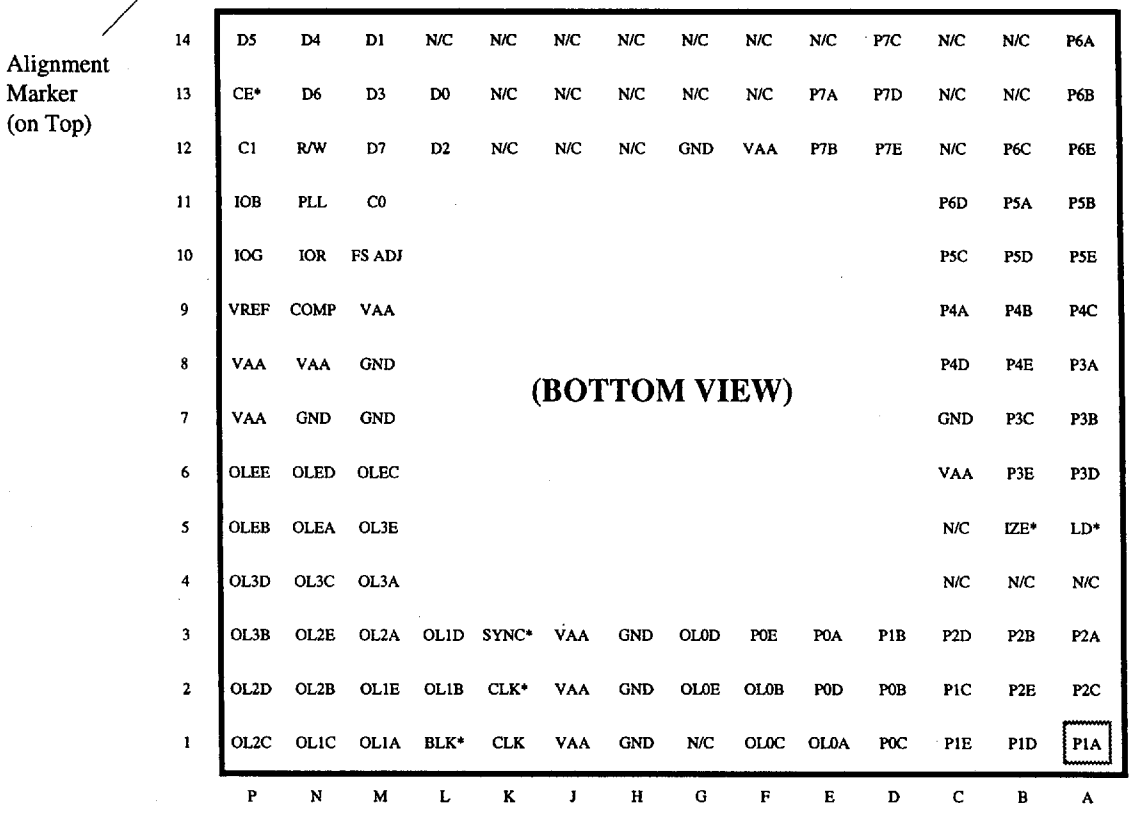
Pin Descriptions *(continued)*—132-pin PGA Package

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	L1	OL0A	E1	GND	H1
SYNC*	K3	OL0B	F2	GND	H2
LD*	A5	OL0C	F1	GND	H3
CLOCK	K1	OL0D	G3	GND	C7
CLOCK*	K2	OL0E	G2	GND	G12
IZE*	B5			GND	M8
		OL1A	M1	GND	M7
P0A	E3	OL1B	L2	GND	N7
P0B	D2	OL1C	N1		
P0C	D1	OL1D	L3	COMP	N9
P0D	E2	OL1E	M2	FS ADJUST	M10
P0E	F3			VREF	P9
		OL2A	M3		
P1A	A1	OL2B	N2	CE*	P13
P1B	D3	OL2C	P1	R/W	N12
P1C	C2	OL2D	P2	C1	P12
P1D	B1	OL2E	N3	C0	M11
P1E	C1				
		OL3A	M4	D0	L13
P2A	A3	OL3B	P3	D1	M14
P2B	B3	OL3C	N4	D2	L12
P2C	A2	OL3D	P4	D3	M13
P2D	C3	OL3E	M5	D4	N14
P2E	B2			D5	P14
		OLEA	N5	D6	N13
P3A	A8	OLEB	P5	D7	M12
P3B	A7	OLEC	M6		
P3C	B7	OLED	N6	reserved	G14
P3D	A6	OLEE	P6	reserved	G13
P3E	B6			reserved	F14
		IOG	P10	reserved	F13
P4A	C9	IOB	P11	reserved	E14
P4B	B9	IOR	N10	reserved	J13
P4C	A9	PLL	N11	reserved	J14
P4D	C8			reserved	H12
P4E	B8	VAA	J1	reserved	H13
		VAA	J2	reserved	H14
P5A	B11	VAA	J3	reserved	C5
P5B	A11	VAA	C6	reserved	A4
P5C	C10	VAA	F12	reserved	B4
P5D	B10	VAA	M9	reserved	C4
P5E	A10	VAA	P7	reserved	C14
		VAA	P8	reserved	C13
P6A	A14	VAA	N8	reserved	B14
P6B	A13			reserved	C12
P6C	B12			reserved	B13
P6D	C11			reserved	L14
P6E	A12			reserved	K12
				reserved	J12
P7A	E13			reserved	K14
P7B	E12			reserved	K13
P7C	D14				
P7D	D13				
P7E	D12				

Pin Descriptions *(continued)*—132-pin PGA Package



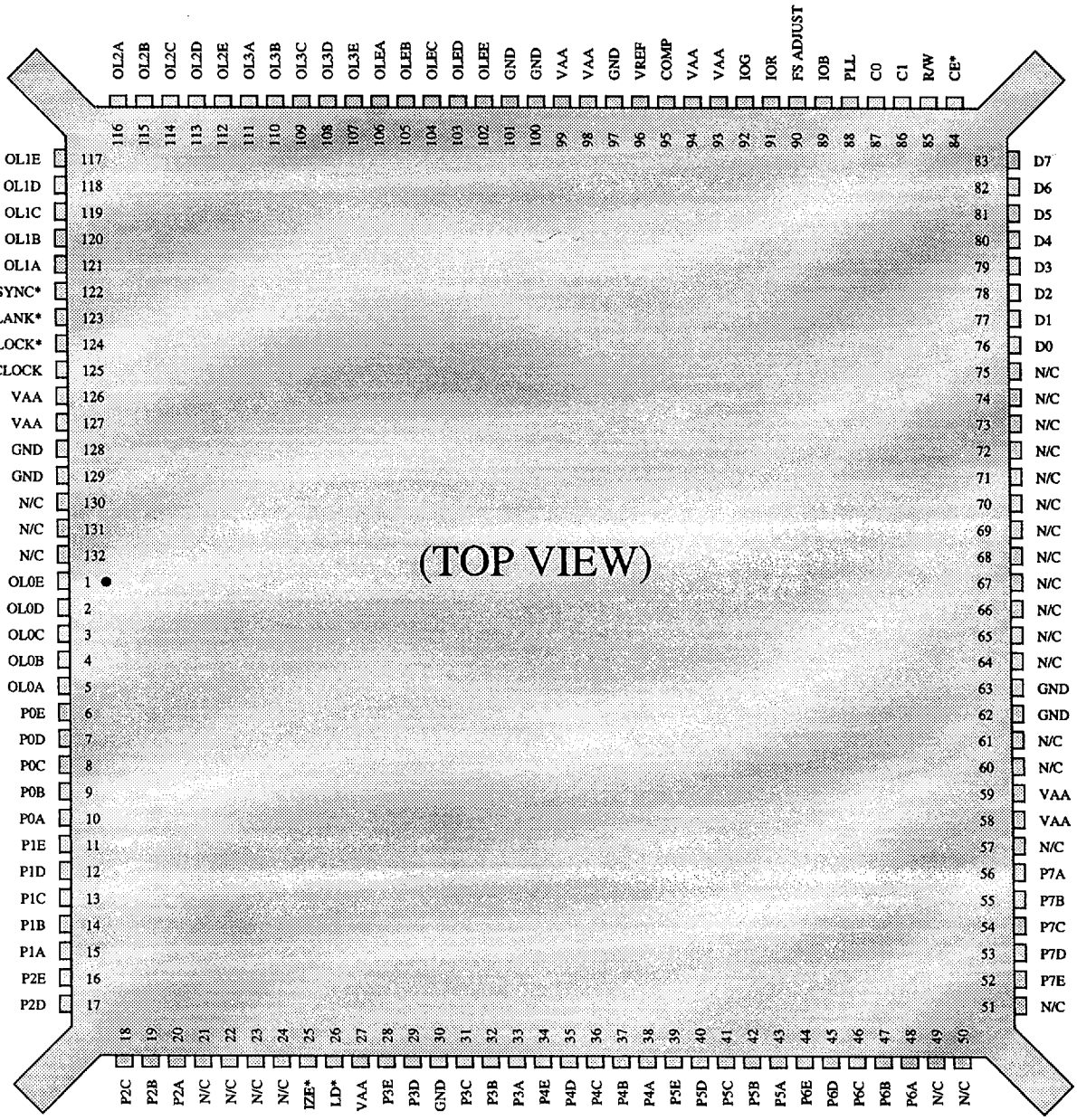
Alignment Marker (on Top)



Pin Descriptions *(continued)*—132-pin PQFP Package

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	OL0E	44	P6E	88	PLL
2	OL0D	45	P6D	89	IOB
3	OL0C	46	P6C		
4	OL0B	47	P6B	90	FS ADJUST
5	OL0A	48	P6A	91	IOR
				92	IOG
6	P0E	49	reserved	93	VAA
7	P0D	50	reserved	94	VAA
8	P0C	51	reserved	95	COMP
9	P0B			96	VREF
10	P0A	52	P7E	97	GND
		53	P7D	98	VAA
11	P1E	54	P7C	99	VAA
12	P1D	55	P7B	100	GND
13	P1C	56	P7A	101	GND
14	P1B				
15	P1A	57	reserved	102	OLEE
		58	VAA	103	OLED
16	P2E	59	VAA	104	OLEC
17	P2D	60	reserved	105	OLEB
18	P2C	61	reserved	106	OLEA
19	P2B	62	GND		
20	P2A	63	GND	107	OL3E
		64	reserved	108	OL3D
21	reserved	65	reserved	109	OL3C
22	reserved			110	OL3B
23	reserved	66	reserved	111	OL3A
24	reserved	67	reserved		
25	IZE*	68	reserved	112	OL2E
		69	reserved	113	OL2D
26	LD*	70	reserved	114	OL2C
27	VAA			115	OL2B
		71	reserved	116	OL2A
28	P3E	72	reserved		
29	P3D	73	reserved	117	OL1E
30	GND	74	reserved	118	OL1D
31	P3C	75	reserved	119	OL1C
32	P3B			120	OL1B
33	P3A	76	D0	121	OL1A
		77	D1		
34	P4E	78	D2	122	SYNC*
35	P4D	79	D3	123	BLANK*
36	P4C	80	D4	124	CLOCK*
37	P4B	81	D5	125	CLOCK
38	P4A	82	D6		
		83	D7	126	VAA
39	P5E			127	VAA
40	P5D	84	CE*	128	GND
41	P5C	85	R/W	129	GND
42	P5B	86	C1		
43	P5A	87	C0	130	reserved
				131	reserved
				132	reserved

Pin Descriptions *(continued)*—132-pin PQFP Package



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt459, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt459 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be a shield to isolate noise from the analog traces with layer 1 (top) for the analog traces, layer 2 for the ground plane, layer 3 for the analog power plane, and the remaining layers used for digital traces and digital power supplies.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt459 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt459 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 13. This bead should be located within 3 inches of the Bt459. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device and should use the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor, decoupling each of the four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins, and should be connected with short, wide traces.

The 33 µF capacitor shown in Figure 13 is for low-frequency power supply ripple. The 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1-µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

PC Board Layout Considerations *(continued)*

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. Alternate PCB pads (one to VAA and one to GND) are recommended for the VREF decoupling capacitor.

Digital Signal Interconnect

The digital inputs to the Bt459 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt459 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt459 to minimize reflections. Unused analog outputs should be connected to GND.

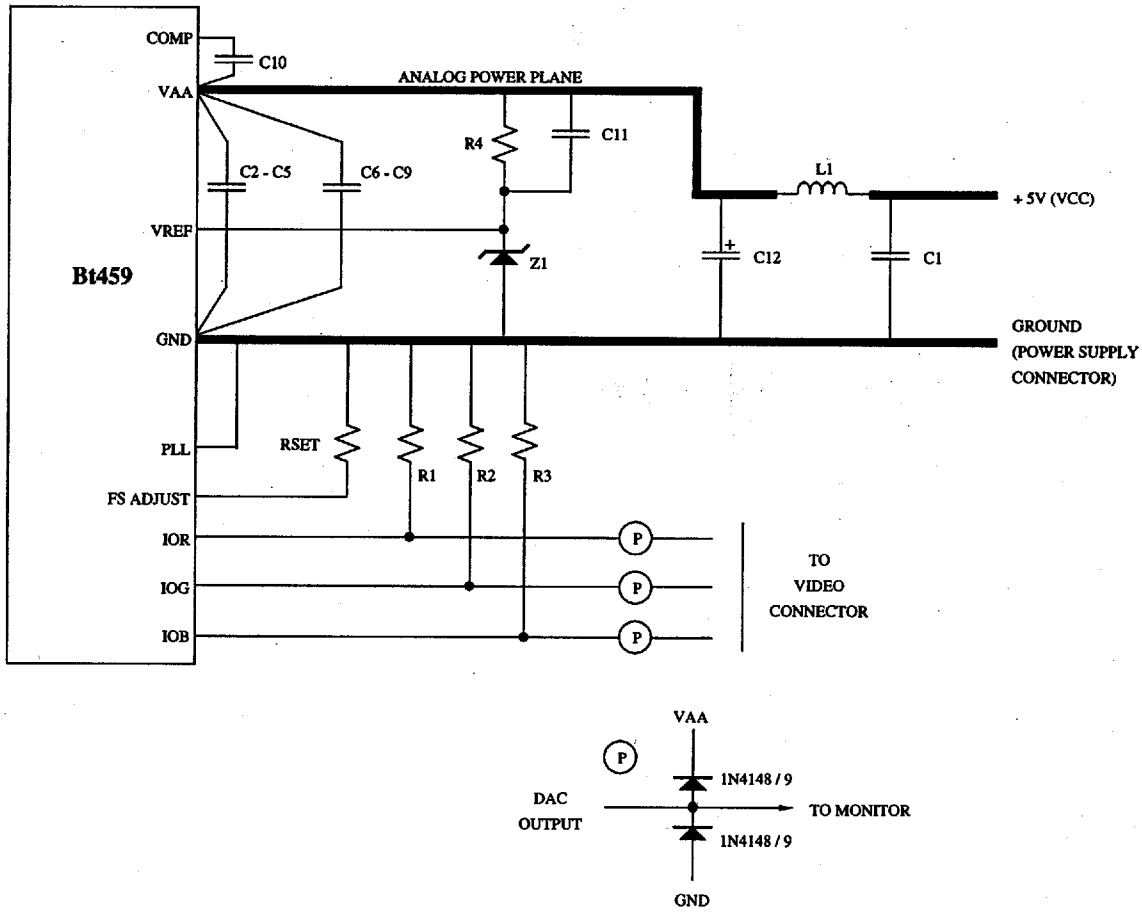
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt459 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 13 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt459.

Figure 13. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Because of the high clock rates at which the Bt459 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. (See Figure 14.)

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak because of the noise margins of the CMOS process. The Bt459 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by four or five (depending on whether 4:1 or 5:1 multiplexing was specified), and translating the result to TTL levels. As LD* may be phase shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt459 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt459, and will optionally set the pipeline delay of the Bt459 to eight clock cycles. The Bt438 may also be used to interface the Bt459 to a TTL clock. Figure 14 illustrates the Bt438 used with the Bt459.

When using a single Bt459, the PLL output is ignored and should be connected to GND (either directly or through a resistor of up to 150 Ω).

Using Multiple Bt459s

For display applications where up to four Bt459s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt459, synchronizes them to subpixel resolution and sets the pipeline delay of the Bt459 to eight clock cycles. The Bt439 may also be used to interface the Bt459 to a TTL clock. Figure 15 illustrates the Bt439 used with the Bt459.

Subpixel synchronization is supported by the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt459, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt459s, and adjusts the delay of each of the CLOCK and CLOCK* signals to the Bt459s to minimize the PLL delay difference. There should be minimal layout skew in the CLOCK and PLL trace paths to ensure proper clock alignment.

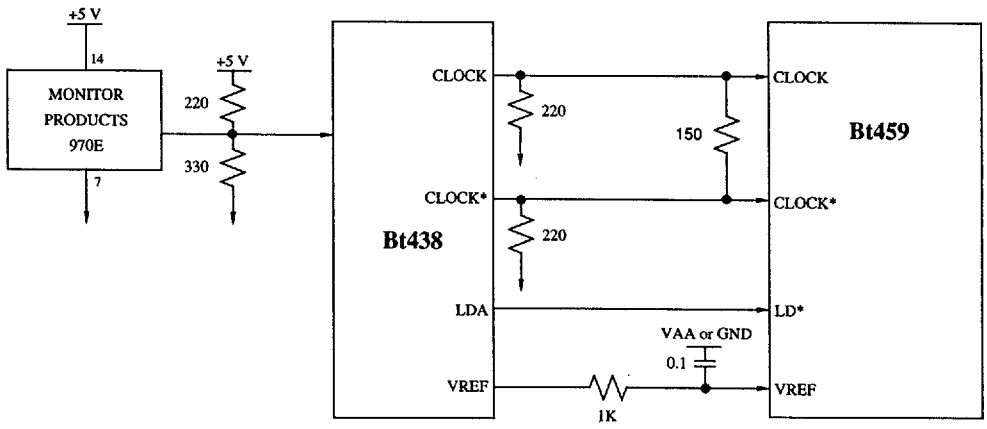


Figure 14. Generating the Bt459 Clock Signals.

Application Information *(continued)*

If subpixel synchronization of multiple Bt459s is not necessary, the Bt438 Clock Generator Chip may be used rather than the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt459s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt459s must still have a 0.1 µF bypass capacitor to VAA, and individual voltage references. The designer must minimize skew on the CLOCK and CLOCK* lines. The PLL outputs of the Bt459s will not be used and should be connected to GND (either directly or through a resistor of up to 150 Ω).

When multiple Bt459s are used, each Bt459 should have its own power plane ferrite bead and voltage reference. Each Bt459 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

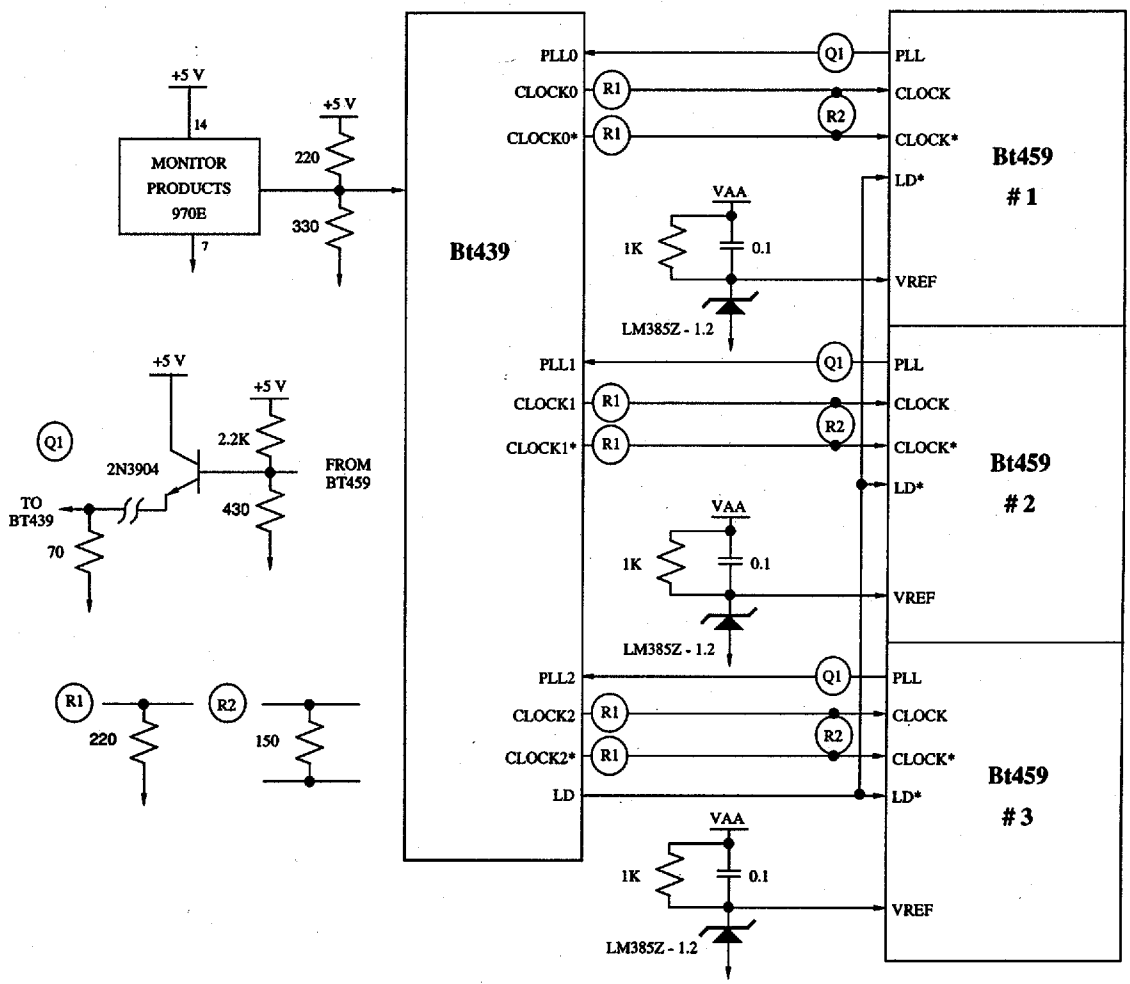


Figure 15. Generating the Clock Signals for Multiple Bt459s.

Application Information *(continued)*

Setting the Pipeline Delay

The pipeline delay of the Bt459, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt459 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438, Bt439, and Bt440 Clock Generator Chips support this mode of operation when used with the Bt459. It is strongly recommended that the Bt438, Bt439, or Bt440 be used for clock generation when multiple Bt459s are used or when a fixed pipeline of eight clock cycles is necessary.

To reset the Bt459, it should be powered up with LD*, CLOCK, and CLOCK* running. The CLOCK and CLOCK* signals should be stopped with CLOCK high and CLOCK* low for *at least* three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

CLOCK and CLOCK* should be restarted so that the first edge of the signals is as close as possible to the rising edge of LD*. (The falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles.) When the clocks are restarted, the minimum clock pulse width must not be violated.

To ensure that the Bt459 has the proper configuration, all the command registers must be initialized prior to a fixed pipeline reset. Because of this requirement, the power-up that occurs prior to initialization of the command registers cannot be used to assume the fixed pipeline. An additional reset is required after command register writes.

When the Bt459 is reset to an eight-clock-cycle pipeline delay, the blink counter circuitry is not reset. Therefore, if the multiple Bt459s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control through the read mask register and overlay display enable bits.

The Bt459 must be reset to an eight-clock-cycle pipeline delay for proper cursor pixel alignment.

Interleave Operation

To support interleaved frame buffers, the Bt459 may be configured for various interleave factors, as shown in Table 8. Table 9 is an example of interleave operation for 4:1 multiplexing, an interleave select of 3, and starting with pixel {A}. Table 10 is an example of the same operation with pixel {B} selected as the starting pixel (with the display panned down three scan lines).

Scan line number 0 corresponds to the top of the display screen and is the first displayed scan line after a vertical blanking interval. The output sequence is shown starting at the left-most displayed pixel.

Scan Line	Output Sequence
0	ABCDABCD...
1	DABCDABC...
2	CDABCDAB...
3	BCDABCDA...
4	ABCDABCD...
5	DABCDABC...
6	CDABCDAB...
7	BCDABCDA...
:	:

Table 9. Interleave Example.

Scan Line	Output Sequence
0	BCDABCDA...
1	ABCDABCD...
2	DABCDABC...
3	CDABCDAB...
4	BCDABCDA...
5	ABCDABCD...
6	DABCDABC...
7	CDABCDAB...
:	:

Table 10. Interleave Example.

Application Information *(continued)*

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Test Features of the Bt459

The Bt459 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section explains the operating use of these test features.

Signature Register (Signature Mode)

The signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color. They are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as to the three on-chip DACs.

The SARs act as a 24-bit wide linear feedback shift register on each succeeding pixel that is latched. It is important to note that in either the 4:1 or 5:1 multiplexed mode the SARs latch only 1 pixel per load group. Thus, the SARs are operating on only every fourth or fifth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, D, or E) is latched to generate new signatures by setting bits D0–D2 in the test register.

In 1:1 mux mode, the SARs will generate signatures truly on each succeeding pixel in the input stream. In this case, the user should always select pixel "A" (Test Register D0, D1, and D2 = 000) when in the 1:1 mode, since the "A" pixel pins are the only active pixel inputs.

The Bt459 will only generate signatures while it is in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt459 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 24-bit seed value into the SARs. Then, a known pixel stream, e.g., one scan line or one frame buffer of pixels, will be input to the chip. At the succeeding blank state, the resultant 24-bit signature can be read by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested with the signature registers.

Assuming the chip is running 4:1 or 5:1 mux modes, the above process would be repeated with all different pixel phases (A, B, C, etc.) selected.

The linear feedback configuration is shown in Figure 16. Each register internally uses XORs at each input bit (D_n) with the output (result) by 1 least significant bit (Q_{n-1}).

Experienced users have developed tables of specific seeds and pixel streams, and recorded the signatures that result from those inputs applied to known-good parts. A good signature from one given pixel stream can by used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed, and the succeeding pixel stream is fed to the SARs.

Signature Register (Data-Strobe Mode)

Setting command bit CR20 to "1" puts the SARs into data-strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the generation of signatures by the SARs. Instead, the SARs capture and hold the respective pixel phase that is selected.

Any MPU data written to the SARs is ignored. However, each pixel color value that is strobed into the SARs can be directly checked. To read out a captured color in the middle of a pixel stream, the user should first freeze all inputs to the Bt459. The levels of most inputs do not matter *except* that CLOCK should be high and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively.

Application Information *(continued)*

In general, the color read out will correspond to a pixel latched on the previous load. However, because the data path is pipelined, the color may come from an earlier load cycle. To read successive pixels:

1. Toggle LD*.
2. Pulse the CLOCK pins according to the mux state (one, four, or five periods).
3. Hold all pixel-related inputs.
4. Perform the three MPU reads as described.

This process is best done on a sophisticated VLSI semiconductor tester.

Analog Comparator

The other dedicated test structure in the Bt459, the analog output comparator, allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected through the test register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the test register on each of the 64 scan lines of the 64 x 64 user-defined cursor block. (The 64 x 64 cursor must be enabled for display.) On each of these 64 scan lines, the capture occurs over one LD* period that corresponds to the cursor (x) position, set by the 12-bit cursor (x) register.

To obtain a meaningful comparison, the cursor should be located on the visible screen. There is no significance to the cursor pattern data in the cursor RAM. For a visual reference, the capture point occurs over the left-most edge of the 64 x 64 cursor block.

Because the comparator is a simple design, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. In this case, the cursor (x) position should be set to well over 500 pixels to ensure an adequate supply of pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, until capture.

Typically, users will create screen-wide test bands of various colors. Various comparison cases are set up by moving the cursor up and down (by changing the 12-bit cursor (y) register) over these bands. For each test, the result is obtained by reading test register bit D3.

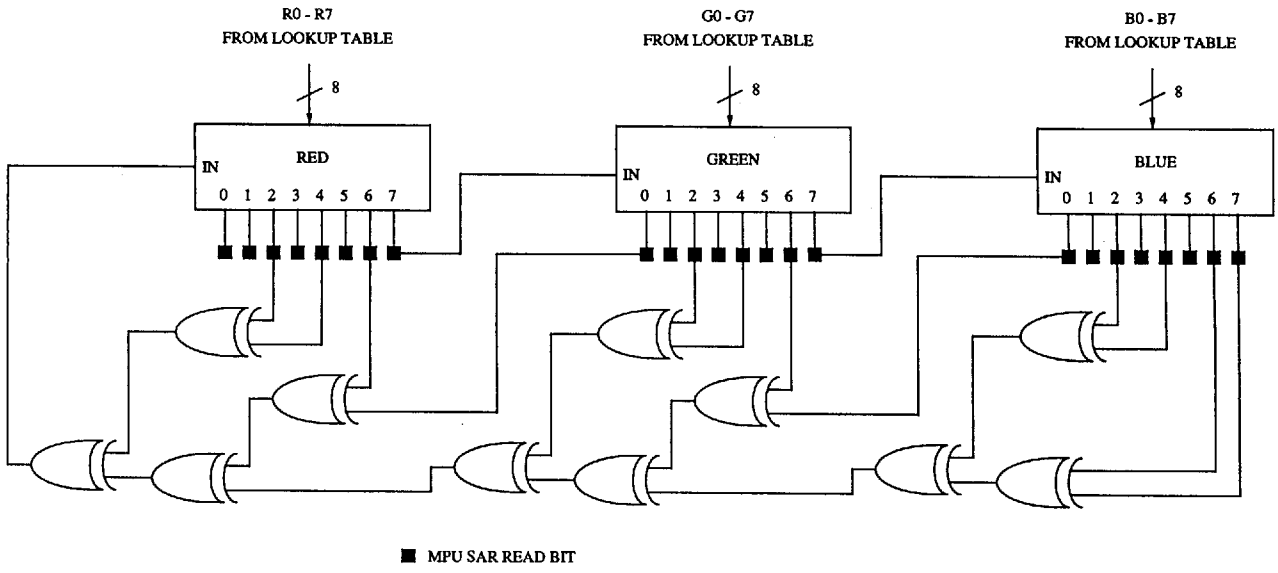


Figure 16. Signature Analysis Register Circuit.

Application Information *(continued)*

Initializing the Bt459

Following a power-on sequence, the Bt459 must be initialized. This sequence will configure the Bt459 as follows:

- 4:1 multiplexed operation
- no overlays, no blinking, and no interleave
- 64 x 64 block cursor and no cross hair cursor
- 8 bits per pixel, no panning, and no zoom
- sync enabled on IOG and a 7.5 IRE blanking pedestal

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $00 to command register_1	10
Write $C0 to command register_2	10
Write $FF to pixel read mask register	10
Write $00 to reserved location	10
Write $00 to pixel blink mask register	10
Write $00 to reserved location	10
Write $00 to overlay read mask register	10
Write $00 to overlay blink mask register	10
Write $00 to interleave register	10
Write $00 to test register	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $C0 to cursor command register	10
Write $00 to cursor (x) low register	10
Write $00 to cursor (x) high register	10
Write $00 to cursor (y) low register	10
Write $00 to cursor (y) high register	10
Write $00 to window (x) low register	10
Write $00 to window (x) high register	10
Write $00 to window (y) low register	10
Write $00 to window (y) high register	10
Write $00 to window width low register	10
Write $00 to window width high register	10
Write $00 to window height low register	10
Write $00 to window height high register	10

Load Cursor RAM Pattern

Write $00 to address register low	00
Write $04 to address register high	01
Write $FF to cursor RAM (location $000)	10
Write $FF to cursor RAM (location $001)	10
:	:
Write $FF to cursor RAM (location $3FF)	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $00)	11
Write green data to RAM (location $00)	11
Write blue data to RAM (location $00)	11
Write red data to RAM (location $01)	11
Write green data to RAM (location $01)	11
Write blue data to RAM (location $01)	11
:	:
Write red data to RAM (location $FF)	11
Write green data to RAM (location $FF)	11
Write blue data to RAM (location $FF)	11

Overlay Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to overlay (location $0)	10
Write green data to overlay (location $0)	10
Write blue data to overlay (location $0)	10
Write red data to overlay (location $1)	10
Write green data to overlay (location $1)	10
Write blue data to overlay (location $1)	10
:	:
Write red data to overlay (location $F)	10
Write green data to overlay (location $F)	10
Write blue data to overlay (location $F)	10

Cursor Color Palette Initialization

Write $81 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10
Write green data to cursor (location $2)	10
Write blue data to cursor (location $2)	10

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω
Air Flow (Note 1)		50			l.f.p.m.

Note 1: Required for Bt459KPF150 only.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
PQFP	TJ			+150	°C
PGA	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = -400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance	CAOUT		13	20	pF
(f = 1 MHz, IOUT = 0 mA)					
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6.00	7.62	9.00	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		–0.5		+2.5	Volts
Output Impedance			50		kΩ
Output Capacitance			8	15	pF
(f = 1 MHz, PLL = 0 mA)					
Voltage Reference Input Current	IREF				
Rev. A			500		µA
Rev. B			10		µA
Power Supply Rejection Ratio	PSRR		0.5		% / % ΔVAA
(COMP = 0.1 µF, f = 1 kHz)					

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min/Typ/ Max	150 MHz	135 MHz	110 MHz	80 MHz	Units
Clock Rate	Fmax	max	150	135	110	80	MHz
LD* Rate	LDmax						
1:1 multiplexing		max	50	50	50	50	MHz
4:1 multiplexing		max	37.50	33.75	27.5	20	MHz
5:1 multiplexing		max	30	27	22	16	MHz
R/W, C0, C1 Setup Time	1	min	0	0	0	0	ns
R/W, C0, C1 Hold Time	2	min	10	10	10	10	ns
CE* Low Time	3	min	40	40	40	40	ns
CE* High Time	4	min	20	20	20	20	ns
CE* Asserted to Data Bus Driven	5	min	10	10	10	10	ns
CE* Asserted to Data Valid	6	max	75	75	75	75	ns
CE* Negated to Data Bus 3-Stated	7	max	15	15	15	15	ns
Write Data Setup Time	8	min	15	15	15	15	ns
Write Data Hold Time	9	min	2	2	2	2	ns
Pixel and Control Setup Time	10	min	3	3	3	3	ns
Pixel and Control Hold Time	11	min	2	2	2	2	ns
Clock Cycle Time	12	min	6.67	7.4	9.09	12.5	ns
Clock Pulse Width High Time	13	min	2.7	3.2	4	5	ns
Clock Pulse Width Low Time	14	min	2.7	3.2	4	5	ns
LD* Cycle Time	15						
1:1 multiplexing		min	20	20	20	20	ns
4:1 multiplexing		min	26.67	29.63	36.36	50	ns
5:1 multiplexing		min	33.33	37.04	45.45	62.5	ns
LD* Pulse Width High Time	16						
1:1 multiplexing		min	7	7	7	7	ns
4:1 or 5:1 multiplexing		min	11	12	15	20	ns
LD* Pulse Width Low Time	17						
1:1 multiplexing		min	7	7	7	7	ns
4:1 or 5:1 multiplexing		min	11	12	15	20	ns

See test conditions on next page.

AC Characteristics *(continued)*

Parameter	Symbol	Min/Typ/ Max	150 MHz	135 MHz	110 MHz	80 MHz	Units
Analog Output Delay	18	typ	12	12	12	12	ns
Analog Output Rise/Fall Time	19	typ	1.5	1.5	1.5	2	ns
Analog Output Settling Time	20	max	8	8	8	12	ns
Clock and Data Feedthrough (Note 1)		typ	–28	–28	–28	–28	dB
Glitch Impulse (Note 1)		typ	50	50	50	50	pV - sec
Analog Output Skew		typ	0	0	0	0	ns
		max	2	2	2	2	ns
Pipeline Delay		min	6	6	6	6	Clocks
		max	10	10	10	10	Clocks
VAA Supply Current (Note 2)	IAA	typ	260	240	220	200	mA
		max	385	360	335	300	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing notes in Figure 18. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Signature Analysis Register (SAR) functionality is not guaranteed at 150 MHz.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough; and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

Timing Waveforms

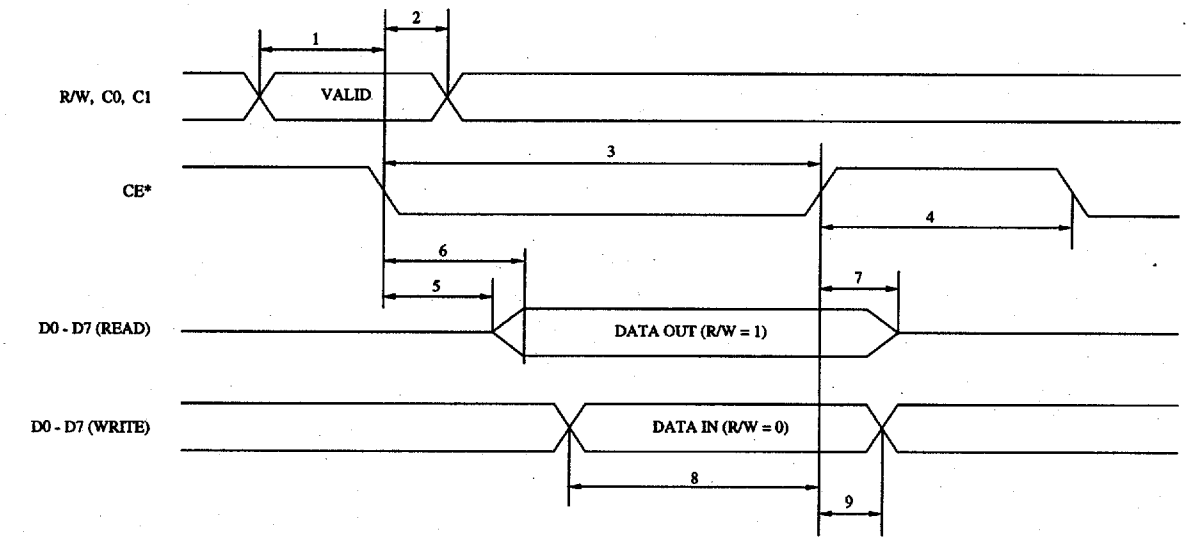
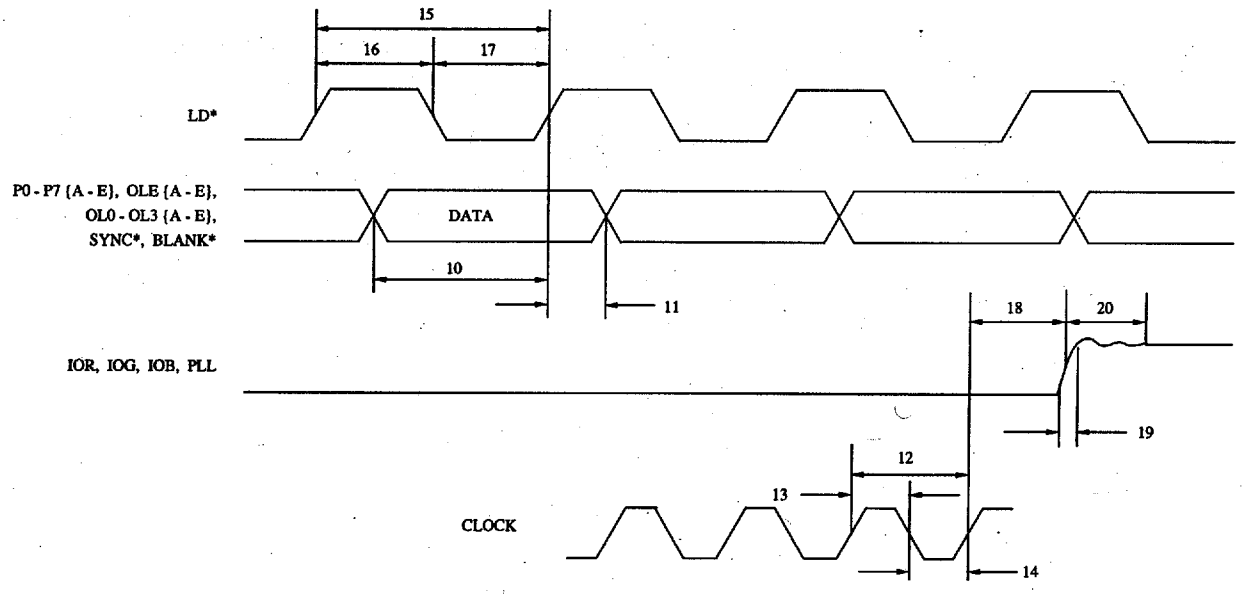


Figure 17. MPU Read/Write Timing Dimensions.



Note 1: Output delay time is measured from 50-percent point of the rising clock edge to 50-percent point of full-scale transition.

Note 2: Output settling time is measured from 50-percent point of full-scale transition to output settling within ±1 LSB.

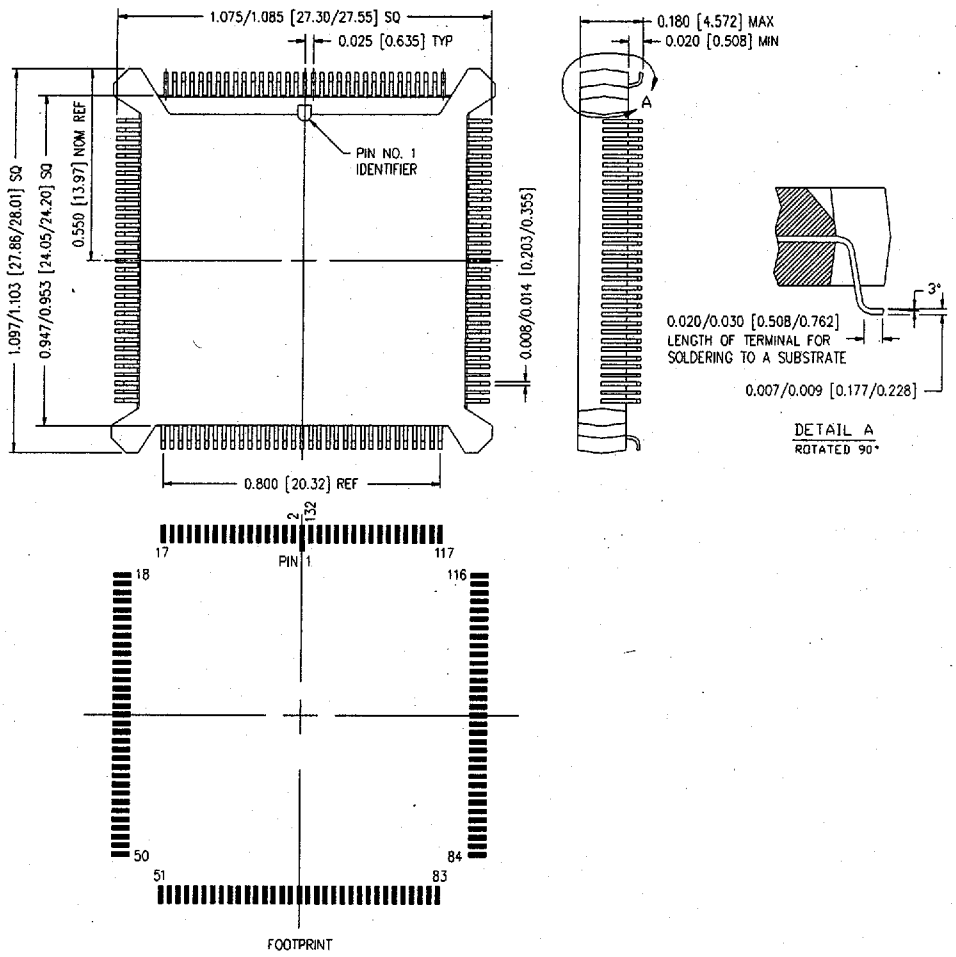
Note 3: Output rise/fall timeis measured between 10-percent and 90-percent points of full-scale transition.

Figure 18. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt459KG150	150 MHz	132-pin Ceramic PGA	0° to +70° C
Bt459KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt459KG110	110 MHz	132-pin CeramicPGA	0° to +70° C
Bt459KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C
Bt459KPF150	150 MHz	132-pin Plastic Quad Flatpack	0° to +70° C with 50 LFPM Airflow
Bt459KPF135	135 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt459KPF110	110 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt459KPF80	80 MHz	132-pin Plastic Quad Flatpack	0° to +70° C

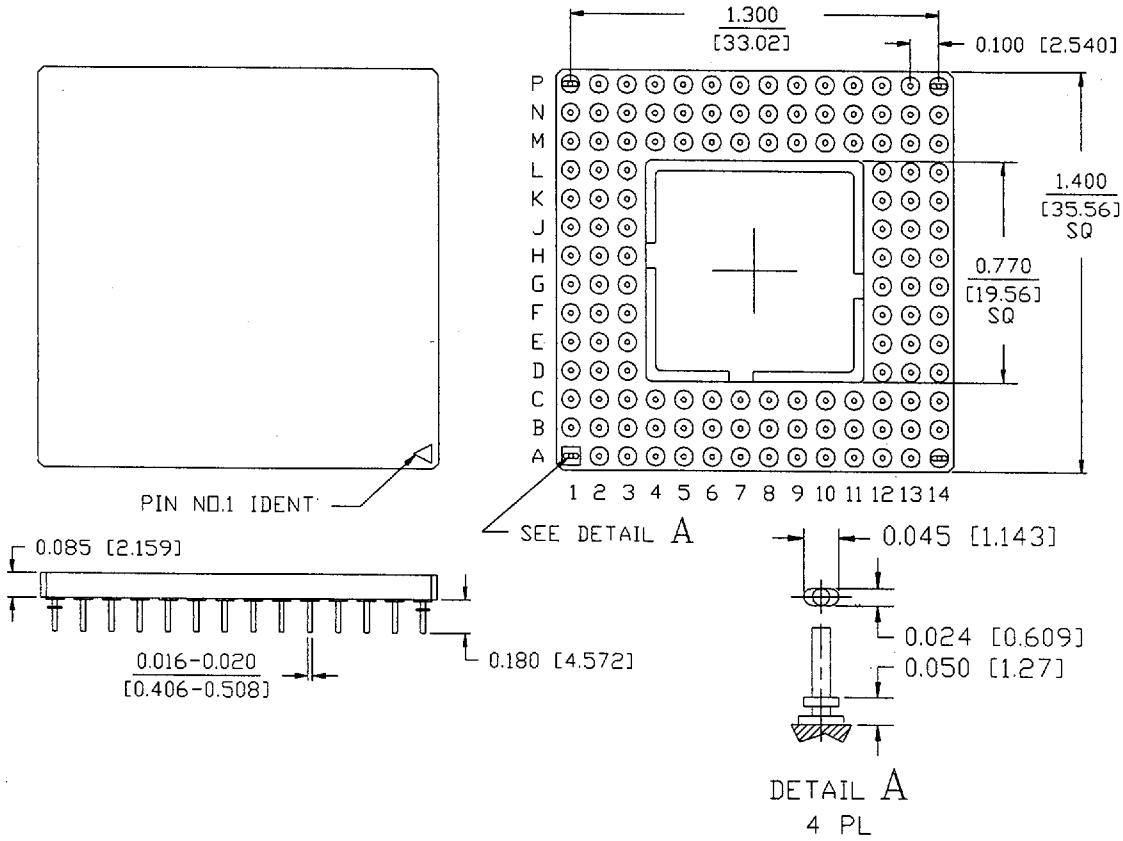
Package Drawing—132-pin Plastic Quad Flatpack (PQFP)



Notes: Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. PQFP packages are intended for surface mounting on solder lands on 0.025 [0.635] centers.

Package Drawing—132-pin Ceramic PGA



Notes: Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. Pins are intended for insertion in hole rows on 0.100" [2.54] centers.

Revision History

Datasheet Revision	*Change from Previous Revision*
G	Revised Figures 14 and 15.
H	Revised Figures 14 and 15.
I	Added 132-pin PQFP package, expanded PC Board Layout Considerations section, added use of test features to Application Information section, added Figure 16 and associated text in Application Information section, and revised Figure 15.
J	Clarified MPU contention with cursor RAM in Cursor RAM subsection of Internal Registers section.
K	Added double reset, modified PLL feedback circuitry, added Revision Register section, reduced IREF, and eliminated write contention for revision B devices.
L	Added 150 MHz speed grade.
M	Changed slow port timing parameters and revised PC Board Layout Considerations section.
N	Datasheet changed from Preliminary to Final status.

Device Revision	
B	Reduced IREF, eliminated write contention, enhanced CE* noise immunity, and added revision register.