T-77-21

LR37632 1-Chip Signal Processing LSI for CD

Description

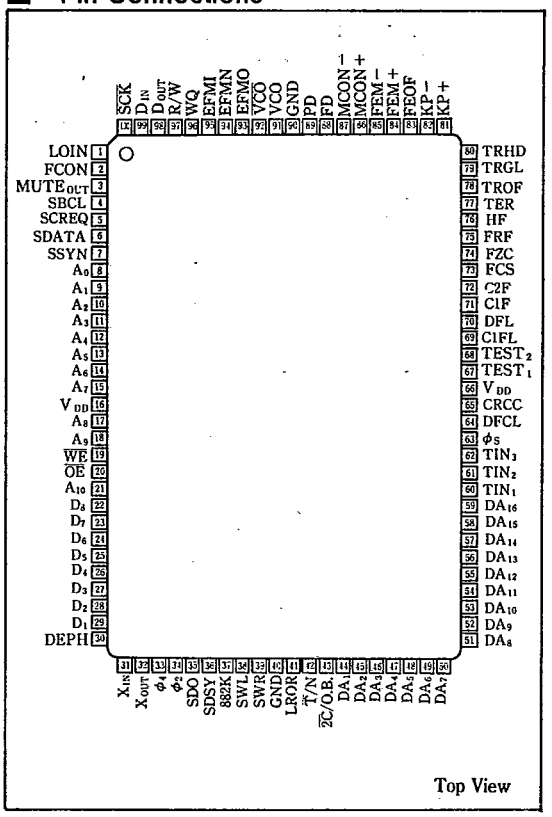
The LR37632 is a CMOS LSI for signal processing and servo control in DAD (Digital Audio Disc) system of CD (Compact Disc) unit.

This LSI provides functions of signal processing such as modulation of EFM signal being output from photoelectric pick-up, address generation of external RAM for de-interleave, detection and correction of error and digital filtering of double oversampling, and servo controls are executed with 1 chip.

Features

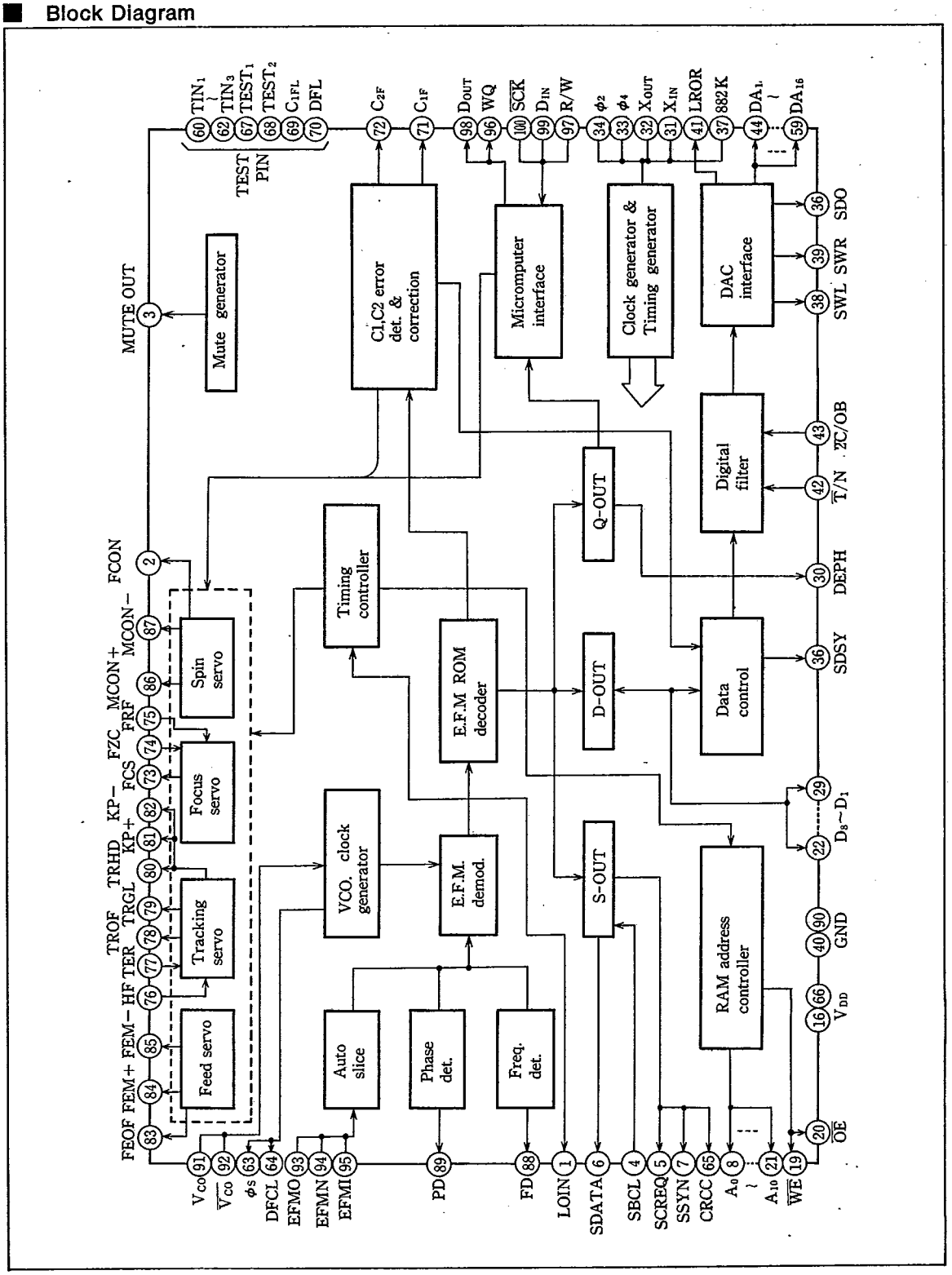
1. Effective frame signal detection and protection function with a couple of synchronizing protection circuits
2. Automatic sequential control function which enables spin motor control by Start/Stop signal alone
3. Improvement of addressing efficiency of externally mounted RAM and realization of ±4.5 frame jitter absorption margin
4. Smooth muting output without click sound
5. High accuracy and high-speed feed system capable of counting number of tracks
6. Heading function which enables designation by total time alone
7. 16-bit serial/parallel output
8. Double oversampling digital filter
9. Low power consumption
10. Single power supply : +5V
11. 100-pin quad flat package

Pin Connections



Top View

Block Diagram



Pin Connection

Pin No.	Pin name	I/O	Name	Pin No.	Pin name	I/O	Name
1	LOIN	O	Synchronization coincidence signal	67-68	$TEST_{1\text{-}2}$	I	Test pin (with pull-up resister)
2	FCON	O	Focus ON output	69	C_{1FL}	O	Test pin
3	$MUTE_{OUT}$	O	Mute output	70	D_{FL}	O	Test pin
4	SBCL	I	Subcode clock input	71	C_{1F}	O	C_1 correction error monitor output
5	SCREQ	O	Subcode request output	72	C_{2F}	O	C_2 correction error monitor output
6	SDATA	O	Subcode data output	73	FCS	O	Focus start output
7	SSYN	O	Subcode synchronizing signal	74	FZC	I	Focus zero cross point input
8-15	A_0-A_7	O	Address output for external RAM	75	FRF	I	Disc reflection signal input
16	V_{DD}	—	Power supply	76	HF	I	HF envelope signal input
17-18	A_8-A_9	O	Address output for external RAM	77	TER	I	Tracking error signal input
19	$\overline{WE}$	O	Write enable signal for external RAM	78	TROF	O	Tracking off signal output
20	$\overline{OE}$	O	Output enable signal for external RAM	79	TRGL	O	Tracking gain signal output
21	A_{10}	O	Address output for external RAM	80	TRHD	O	Tracking hold signal output
22-29	D_8-D_1	I/O	Data input/output for external RAM	81	KP+	O	Positive direction kick pulse output
30	DEPH	O	De-emphasis control signal	82	KP−	O	Negative direction kick pulse output
31	X_{IN}	I	Crystal input	83	FEOF	O	Feed off signal output
32	X_{OUT}	O	Crystal output	84	FEM+	O	Positive direction feed signal output
33	ϕ_4	O	4.3218 MHz output	85	FEM−	O	Negative direction feed signal output
34	ϕ_2	O	2.1609 MHz output	86	MCON+	O	Positive direction spin motor output
35	SDO	O	Music data serial output	87	MCON−	O	Negative direction spin motor output
36	SDSY	O	DAC control signal	88	FD	O	Frequency comparison output
37	882K	O	DAC control signal	89	PD	O	Phase comparison output
38	SWL	O	Deglitch signal	90	GND	—	GND
39	SWR	O	Deglitch signal	91	VCO	I	VCO input
40	GND	—	GND	92	$\overline{VCO}$	O	VCO output
41	LROR	O	Data latch signal for DAC	93	EFMO	O	EFM signal automatic level slice
42	$\overline{T}$/N	I	True/Double sampling switch input	94	FEMN	I/O	EFM signal automatic level slice
43	$\overline{2.C}$/O.B	I	Music data output format switch input	95	EFMI	I	EFM signal automatic level slice
44-59	DA_1-DA_{16}	O	Music data parallel output	96	WQ	O	Q code write request output
60-62	TIN_1-TIN_3	O	Test pin	97	R/W	I	Q code read/write selection input
63	ϕ_S	O	VCO system clock output	98	D_{OUT}	O	Q code data output
64	DFCL	O	VCO system frame synchronizing signal	99	D_{IN}	I	Command input
65	CRSS	O	CRSS error detection result signal	100	$\overline{SCK}$	I	D_{OUT}·D_{IN} clock input
66	V_{DD}	—	Power supply				

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	−0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}	−55 to +150	℃

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	4.	5.0	5.5	V
Operating temperature	T_{opr}	−10		70	℃
Oscillation frequency	f_{OSC}		8.6436		MHz

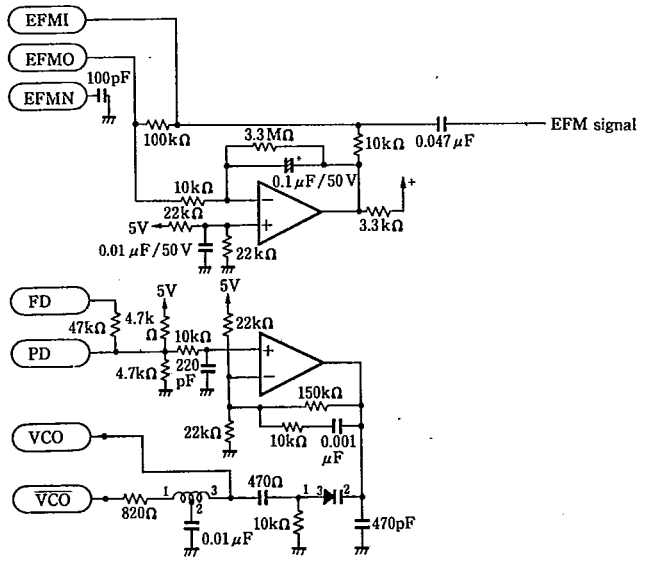
DC Characteristics

(V_{DD}=5.0V±10%, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Operating current	I_{op}			25	50	mA	1
Input voltage	V_{IH}		0.7V_{DD}		V_{DD}	V	
	V_{IL}		GND		0.3V_{DD}		
Output voltage	V_{OH}	I_{OH}=1 mA	V_{DD}−0.5			V	
	V_{OL}	I_{OL}=−1 mA			0.5		
Input leakage current (1)	I_L	V_I="High" or "Low"			1.0	μA	2
Input leakage current (2)	I_{LH}	V_I="High"			1.0	μA	3
	I_{LL}	V_I="Low"		60	120		

Note 1 : Circuits as shown below are connected to VCO system pins and EFM system pins.
CMOS 2K byte SRAM is connected to RAM pin. Measurement is taken when in crystal oscillation.
Output pins other than the above, $TEST_1$ and $TEST_2$ pins are in open state, and input pins other than the above are in "Low" state during measurement.
Note 2 : Applied to input pins other than $TEST_1$ and $TEST_2$ pins.
Note 3 : Applied to $TEST_1$ and $TEST_2$ pins.

Test Circuit



AC Characteristics

(V_{DD}=5.0V±10%, Ta=25℃)

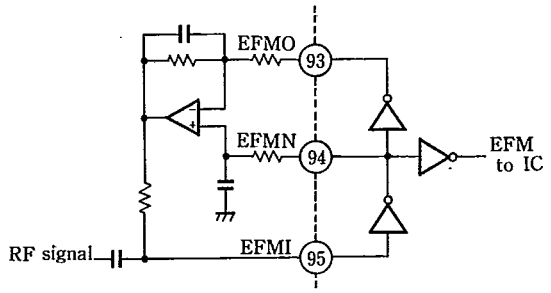
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
VCO	t_r, t_f	C_L=50pF		25	50	ns	
ϕ_4	t_r, t_f	C_L=20pF			35	ns	
	t_x			231			
ϕ_2	t_r, t_f	C_L=20pF			35	ns	
	t_x			463			
LROR	t_r, t_f	C_L=20pF			35	ns	
	t_x			5.8		μs	
882K	t_r, t_f	C_L=20pF			35	ns	
	t_x			11.3		μs	
Output pins other than above	t_r, t_f	C_L=20pF		75	150	ns	
ϕ_4, ϕ_2-SDO	t_{SD}	C_L=20pF		20	60	ns	1
Parallel output timing	t_{DAL}	C_L=20pF	250			ns	2
	t_{DAR}		250				
Q code output timing	t_{DOUT}	C_L=20pF		25	60	ns	
	t_{SCK}		1			μs	
Subcode output timing	t_{SEC}	C_L=20pF	1			μs	
	t_{SDA}			25	60	ns	
	t_{SCR}			20			
Write cycle timing	t_{RWC}	C_L=30pF		231		ns	
	t_{AW}			58			
	t_{WE}			126			
	t_{WS}		10				
	t_{WH}		10				
Read cycle timing	t_{RWC}	C_L=50pF		231		ns	
	t_{DS}		30				
	t_{DH}		0				
	t_{OEO}			57.8			

Note 1 : ϕ_4 when $\overline{T}/N$= "Low", ϕ_2 when $\overline{T}/N$= "High"
Note 2 : ϕ_4 when $\overline{T}/N$= "Low"

Functional Description

(1) Slice level control

Three pins of EFMI (input), EFMN (input/output) and EFMO (output) are provided to control the level slice of RF signal coming from the laser pick-up. Automatic level slice is realized with the following configuration.

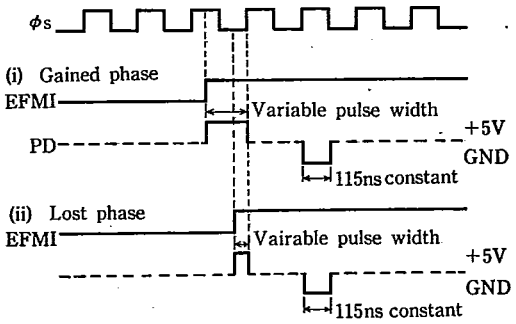


(2) Clock regeneration

PD is the output from phase comparator. When PD output is HZ (high impedance), it has the following output format with respect to EFMI and ϕ_S (4.3218 MHz standard). It becomes HZ for others.

When EFMI input signal is reversed, its phase is compared with ϕ_S at the reversed point of change. The result is output from PD pin as the change in pulse width of "High" level. This is converted into DC level and input into VCO circuit. Thus clock ϕ_S phase synchronized with EFM signal is generated.

By connecting LC resonance circuit between VCO and $\overline{VCO}$, clock oscillation (standard 8.6436 MHz) is carried out. It is possible to make a PLL system together with PD. This clock oscillation generates ϕ_S by means of internal divider (1/2).



The FD pin is an output pin to synchronize PLL of VCO system much faster at spin motor rough servo.

(3) Synchronization coincidence signal, system clock output and frame synchronizing signal output

The LOIN pin is used to output the coincidence of self-running synchronizing signal (by internal counter) with frame synchronizing signal. This will not be output when synchronizing signal is missing or start-stop is deviated.

This signal is continued for one frame length.

LOIN	Content
1	Synchronizing period
0	Asynchronizing period

ϕ_S is the output of VCO system clock standard (4.3218MHz).

DFCL is the output pin of VCO system synchronizing signal standard (7.35kHz; duty 50-50).

(4) Transmission of subcode

Pins related to subcode are provided for future expansion of the system.

When subcode synchronizing signals S_0 or S_1 is detected, "High" signal is output from SSYN pin at the point of S_1 for one frame length.

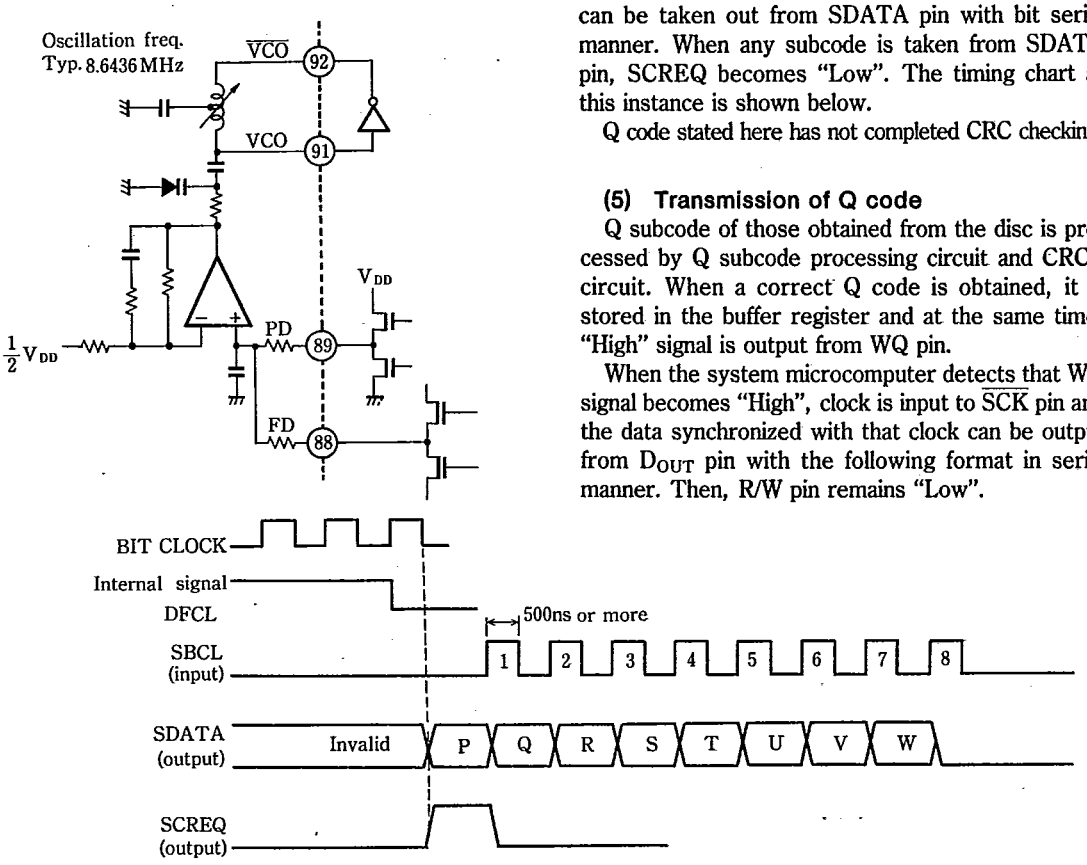
When all subcodes are taken into internal register of SDATA, SCREQ pin output becomes "High". When clock S_{BCL} is given from the system microcomputer after receiving this, subcodes P through W can be taken out from SDATA pin with bit serial manner. When any subcode is taken from SDATA pin, SCREQ becomes "Low". The timing chart at this instance is shown below.

Q code stated here has not completed CRC checking.

(5) Transmission of Q code

Q subcode of those obtained from the disc is processed by Q subcode processing circuit and CRCC circuit. When a correct Q code is obtained, it is stored in the buffer register and at the same time, "High" signal is output from WQ pin.

When the system microcomputer detects that WQ signal becomes "High", clock is input to $\overline{SCK}$ pin and the data synchronized with that clock can be output from D_{OUT} pin with the following format in serial manner. Then, R/W pin remains "Low".



Subcode transmission timing

Result of CRCC error detection is output from CRCC pin. When no error is detected, "Low" level signal is output. If an error is detected, "High" level signal is output.

Content of D_{OUT} output

1	Internal STATE		← Internal STATE is shown below
2	CONT	ADR	← CONT(4)00∗0 2ch, 10∗0 4ch } without emphasis; 00∗1 2ch, 10∗1 4ch } with emphasis; 01∗0 Date, Track
3	Track number		
4	Index		
5	MIN.		Time from the start of music data
6	SEC.		
7	FRAME		
8	ALL"0"		Total time from the start of DISK
9	AMIN.		
10	ASEC.		
11	AFRAMC		

Content of internal state of D_{OUT} output

SIGN	S_2	S_1	8F	4F	MZ	FCO	NQ

MSB LSB

SIGN : Search polarity
S_2, S_1 : Search mode
8F, 4F : Frame error
MZ : Disk motor stop
FC_O : Focus out
NQ : Q code detection

WQ signal becomes "High" when MZ and FCO flags are changed or when NQ code is set.

As long as LSB (NQ) of the first one byte is being set when Q code is read out, subsequent 80 bits are read out continuously.

(6) Real time set

The head position in automatic search mode is controlled by "A" time (total time) instead of the time for every music.

As for this total time, "A" time data at Q code reading is stored into internal register. It is therefore necessary to read out all Q code data prior to SEARCH command execution and to renew real time in the internal register.

(7) Receiving of commands

When a command is written from system control microcomputer, "High" signal is applied to R/W pin and serial 8-bit data is written to DIN pin synchronizing with the clock being entered into $\overline{SCK}$ pin.

		Command	TEST						
1	Command	→	M_4	M_3	M_2	M_1	T_4	T_3	T_2	T_1
2	AMIN.									
3	ASEC.	} Target time (SEARCH command)								
4	AFRAME									

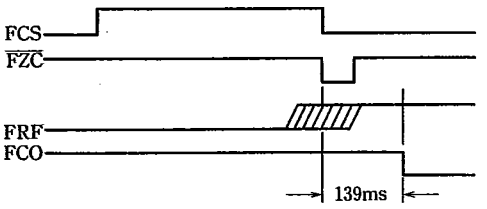
〈List of M_4 through M_1 commonds〉

Content of command	M_4	M_3	M_2	M_1
STOP	0	0	0	0
	0	0	0	1
FEED FOR.	0	0	1	0
FEED RET.	0	0	1	1
FOCUS START	0	1	0	0
	0	1	0	1
DISC START	0	1	1	0
DISC BRAKE	0	1	1	1
PLAY	1	0	0	0
PLAY MUTE	1	0	0	1
FF	1	0	1	0
FR	1	0	1	1
FFF	1	1	0	0
FFR	1	1	0	1
SEARCH	1	1	1	0
	1	1	1	1

(8) Focus servo control

Upon receiving FOCUS START command from system microcomputer, focus servo initial pull-in signal is "High" output with from FCS pin. By generating potential in the external integration circuit to drive the focus coil, the focus moves. When focus point index signal is entered from $\overline{FZC}$ pin, pull-in by FCS is turned OFF.

When it is checked 139 ms later that FRF pin input became "High", internal state FCO (Focus OFF) flag is turned zero and write request signal WQ is output. Thus system microcomputer realizes completion of focus.



(9) Spin servo control

When DISC START is entered by the command from system microcomputer, spin servo control signal is output from MCON+, MCON− output pin while spin motor rotational speed is judged automatically. Upon receiving STOP command, brake is applied suddenly to the spin motor and a signal is output to stop it immediately.

Laser Light ON (H)/OFF (L) timing of a laser pick-up is output from FCON pin depending on spin servo condition.

(10) Tracking servo control

Normally, an analog loop is created by amplifying a tracking error signal to execute tracking hold.

This circuit is not driven in normal state but actuated in manual or automatic search.

When in operation, KP+, KP− is output to execute tracking. "TRHD" is output during operation to hold the tracking error signal.

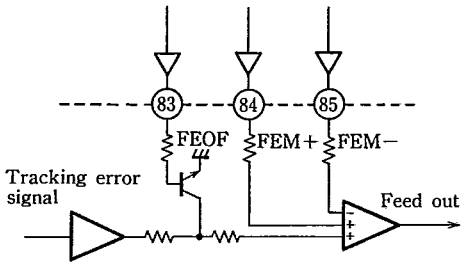
"TRGL" output is used to improve the tracking gain after kick pulse is output.

Change in amplitude of "HF" signal generated by track crossing is sampled at zero cross point of tracking error signal "TER", HFS signal is created as an internal signal, "TROF" signal is output by the logic of internal circuit as shown above. Servo circuit is turned ON/OFF by this change in signal level so that the track can easily be caught.

(11) Feed servo control

Feed servo control mode is initiated during high speed searching by FEED FOR and FEED RET command or SEARCH command. Feed servo loop is discontinued by the signal output from FEOF pin, and field pulse signal for pick-up movement is output from FEM+ pin and FEM− pin. The pickup moves to the intended direction by this operation.

〈Feed servo control〉



(12) Muting output

Signal output from $MUTE_{OUT}$ pin may be utilized as muting signal of PCM data output signal (16-bit music signal). $MUTE_{OUT}$ signal is output when frame synchronizing/asynchronizing is in the following states :

i) Frame asynchronizing state continued for more than 6 ms.

ii) When cumulative value exceeds 6 ms while asynchronizing time is added and synchronizing time is subtracted for the case where frame synchronization is unstable.

Muting signal is released 15 ms after frame synchronization is reset.

(13) Music signal output

DA_1-DA_{16} are 16-bit music signal parallel output pins, and SDO is serial output pin.

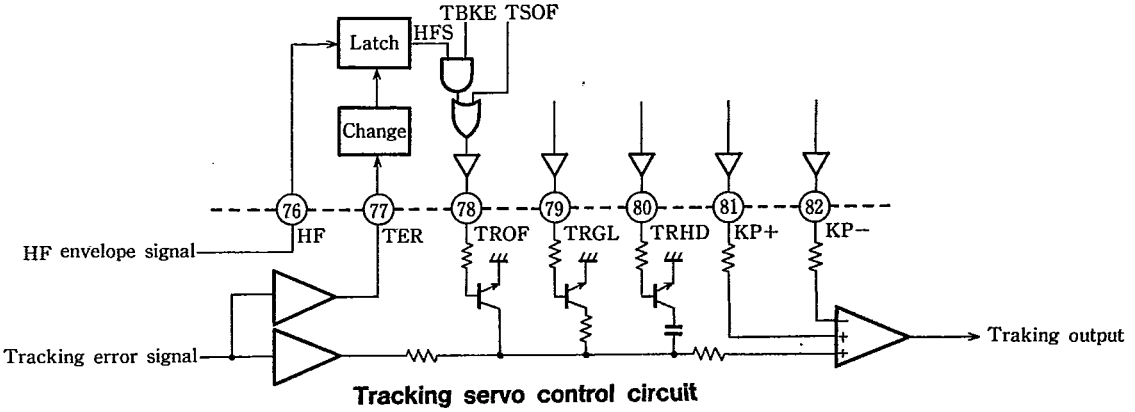
Music signal format is depending on $\overline{2C}$/OB and $\overline{T}$/N pin input state.

Pin name	"High" or "Low"	Function
$\overline{2C}$/OB	"High"	Offset binary output
	"Low"	2's complement output
$\overline{T}$/N	"High"	Pre-filtering is output (44.1kHz)
	"Low"	Post-filtering is output (88.2kHz)

Furthermore, signals SWR and SWL for DAC deglitching showing RIGHT signal and LEFT signal are output together with the data.

SDSY pin outputs a synchronizing signal that becomes "Low" when SDO is RIGHT signal and outputs a synchronizing signal that becomes "High" when SDO is LEFT signal. Data latch signal for DAC is output from LROR pin.

In the case music signal data that requires deemphasis operation is being output, "High" signal is output from DEPH pin.



Tracking servo control circuit

(14) Error correction

A signal is output from C_{1F} pin and C_{2F} pins depending on error states at C_1 correction and C_2 correction.

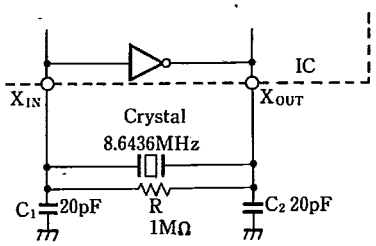
Relation between error state and output is shown below. This is normally used with open state.

Error state at C_1 correction	C_{1F}
0	"Low"
1	"Low"
More than 2	"High"

LR error state after C_2 correction		C_{2F}
L	R	
ERROR	ERROR	"Low"
ERROR	○	"High"
○	ERROR	"High"
○	○	"High"

(15) System clock oscillation circuit

X_{IN} and X_{OUT} are crystal oscillation pins for 8.6436 (MHz).



Its external circuit is shown right. Constants shown here are for reference only.

(16) RAM address generation

RAM address generation circuit generates external 2K-byte RAM address and executes the following CIRC modulation using external RAM.

1. Jitter absorption of symbol data and one frame delay
2. De-interleave of symbol data is executed.
3. De-scramble of symbol data and two frame delay

A_0-A_{10}, $\overline{WE}$, $\overline{OE}$, and D_1-D_8 pins are address signal, data signal and input/output control signal to be connected to external RAM.

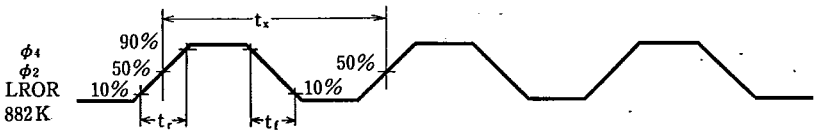
(17) Test pins

TIN_1-TIN_3, $TEST_1$, $TEST_2$, C_{1FL}, D_{FL}

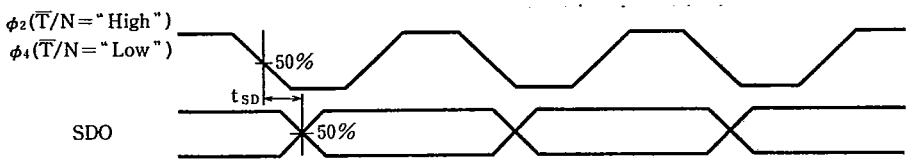
All these pins are used for test. $TEST_1$, $TEST_2$ and C_{1FL} are used with "High" sate. Other pins are used with open state.

■ Timing Diagram

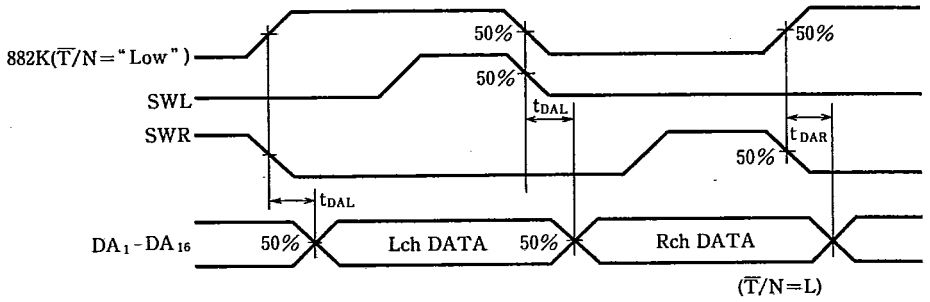
(1) Clock timing



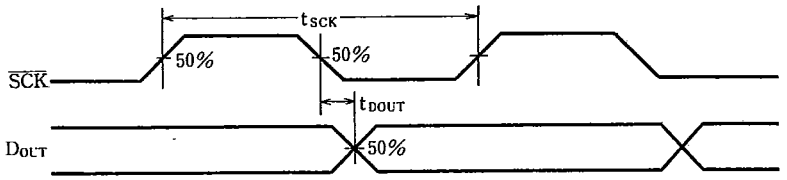
(2) Serial bit output timing



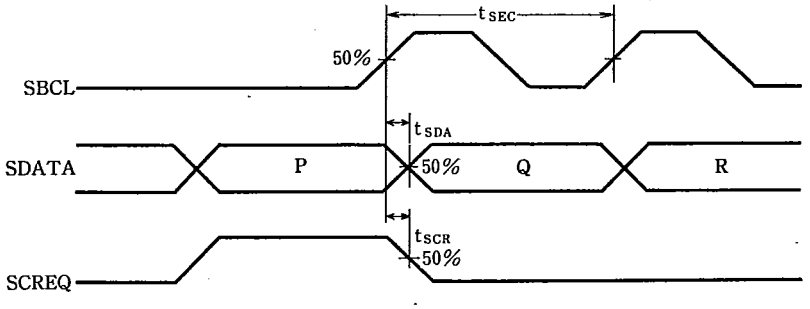
(3) Parallel bit output timing



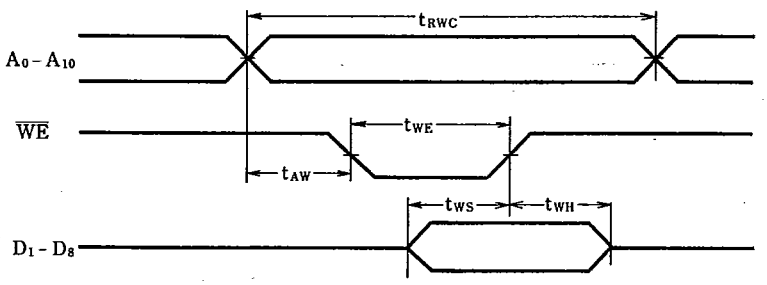
(4) Q code output timing



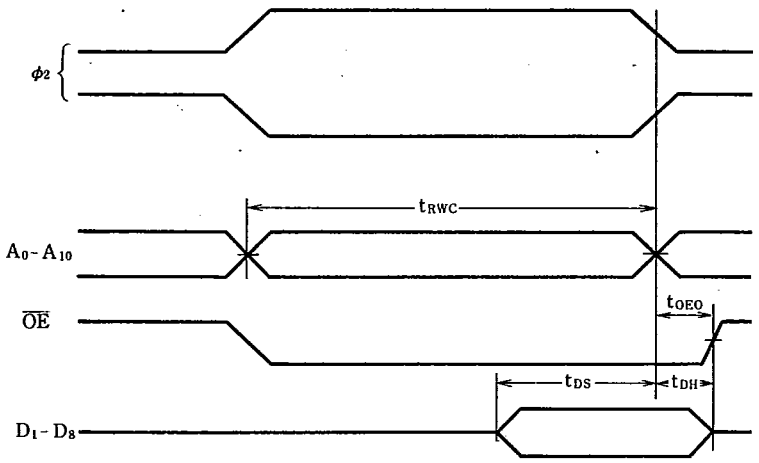
(5) Subcode output timing

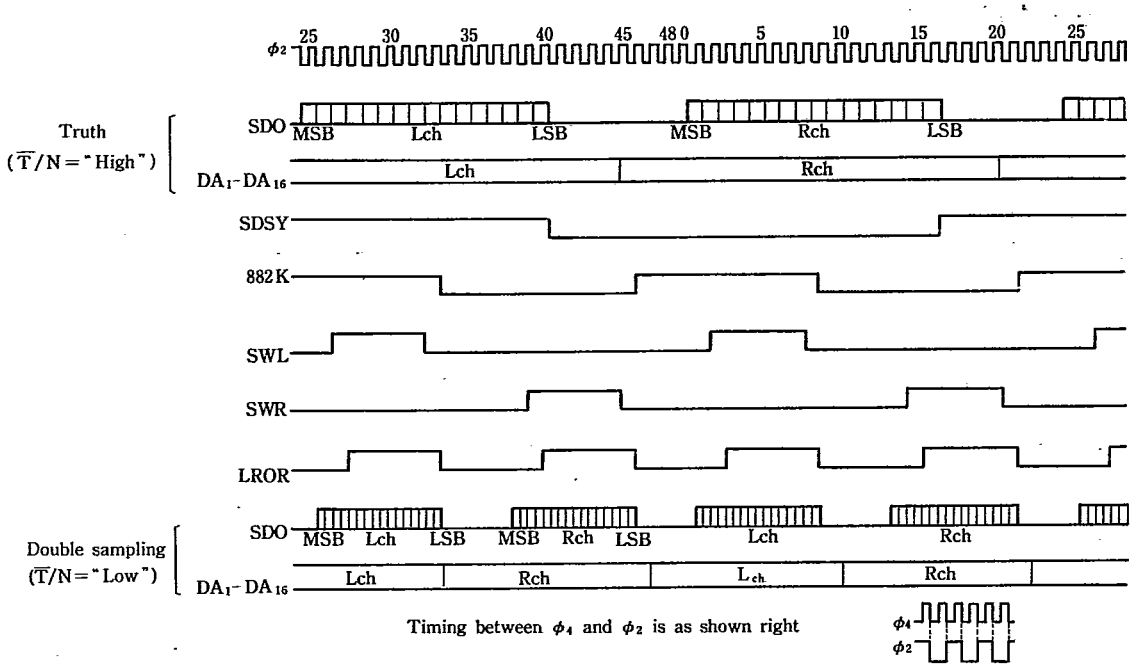


(6) Write cycle timing



(7) Read cycle timing





System Configuration Example