TMX4C1024, TMX4C1025, TMX4C1026, TMX4C1027, TMX4C1029
1,048,576-BIT DYNAMIC RANDOM-ACCESS MEMORIES

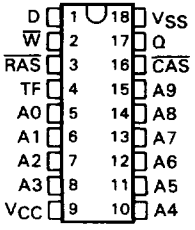
NOVEMBER 1985

- 1,048,576 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- Pinout to Proposed JEDEC Standard
- Performance Ranges:

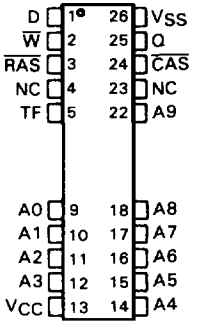
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMX4C102_-10	100 ns	50 ns	200 ns
TMX4C102_-12	120 ns	60 ns	230 ns
TMX4C102_-15	150 ns	75 ns	260 ns

- Multiple Operations Options:
  - TMX4C1024 — Page Mode/Enhanced Page Mode
  - TMX4C1025 — 4-Bit Nibble Mode
  - TMX4C1026 — 8-Bit Nibble (Byte)
  - TMX4C1027 — Static Column Mode
  - TMX4C1029 — 1024-Bit Nibble Mode (Serial Mode)
- Long Refresh Period
  512-Cycle Refresh in 8 ms (Max)
- Three-State Unlatched Output
- Lower Power Dissipation
- New Scaled-CMOS Technology
- All Inputs and Clocks Are TTL Compatible
- Low Standby Power with CMOS-Level Inputs
- High-Reliability Plastic 18-Pin 300-Mil-Wide DIP or Surface-Mount Packages

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The Megabit DRAM devices are high-speed, 1,048,576-bit dynamic random-access memories organized as 1,048,576 words of one bit each. They employ state-of-the-art TIC-MOS (Scaled CMOS) technology for high performance, reliability and lower power at a low cost.

TEXAS INSTRUMENTS
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