HARRIS Semiconductor

CD74FCT16501T, CD74FCT162501T, CD74FCT162H501T

October 1997

Fast CMOS 18-Bit Registered Transceivers

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16501T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162501T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162H501T**
  - **Bus Hold Retains Last Active Bus State During Three-State**
  - **Eliminates the Need for External Pull-Up Resistors**

Description

These devices are 18-bit are registered bus transceivers designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and $\overline{OEBA}$, Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using $\overline{OEBA}$, LEBA and CLKBA. These high-speed, low power devices offer a flow-through organization for ease of board layout.

The CD74FCT16501T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162501T has 24mA balanced output divers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

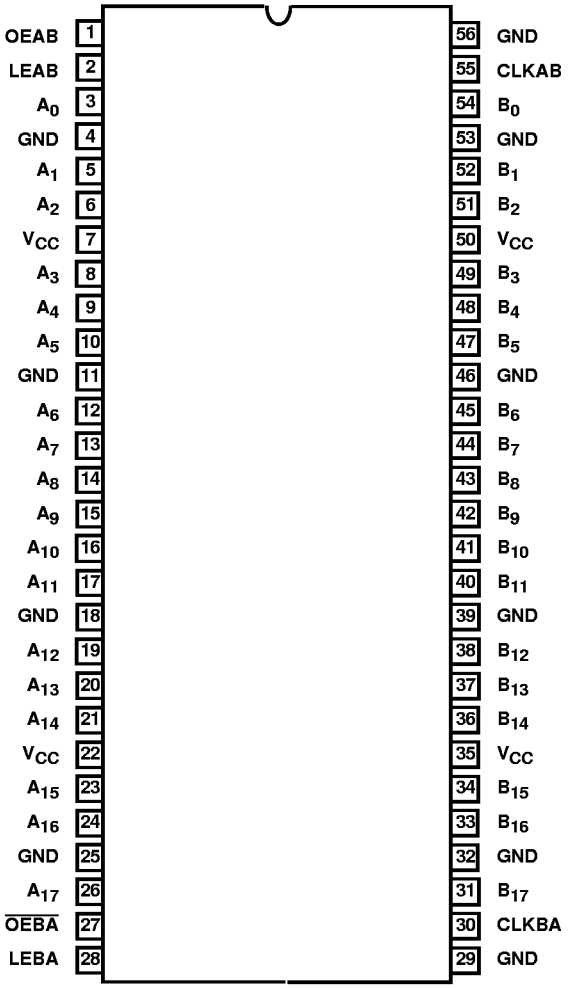
The CD74FCT162H501T has "Bus Hold" which retains the inputs last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Ordering Information

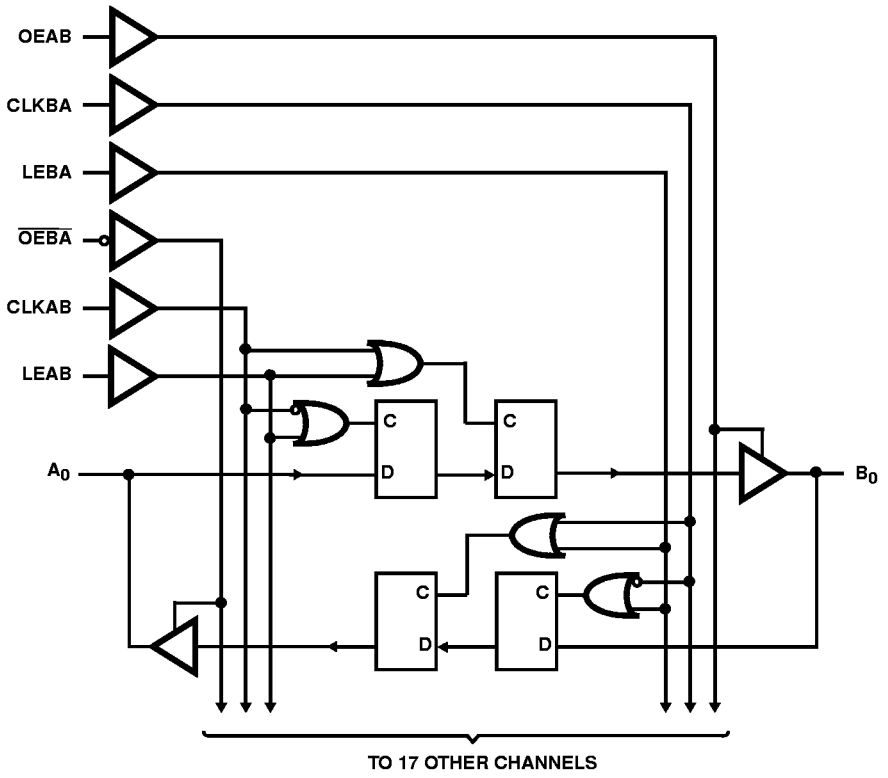
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16501ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16501ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16501CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16501CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16501DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16501DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16501ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16501ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162501ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162501ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162501CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162501CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162501DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162501DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162501ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162501ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H501ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H501ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H501CTMT	-40 to 85	56 Ld TSSOP	M56.300-P
CD74FCT162H501CTSM	-40 to 85	56 Ld SSOP	M56.240-P
CD74FCT162H501DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H501DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H501ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H501ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162H501TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162H501TSM	-40 to 85	56 Ld SSOP	M56.300-P

Pinout

CD74FCT16501T, CD74FCT162501T, CD74FCT162H501T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTES 1, 4)

INPUTS				OUTPUTS
OEAB	LEAB	CLKAB	A_X	B_X
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B (Note 2)
H	L	H	X	B (Note 3)

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.
4. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A_X	A-to-B Data Inputs or B-to-A Three-State Outputs (Note 5)
B_X	B-to-A Data Inputs or A-to-B Three-State Outputs (Note 5)
GND	Ground
V_{CC}	Power

NOTE:

5. For the CD74FCT162H501T, these pins have “Bus Hold”. All other pins are standard, outputs, or I/Os.

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 6)	θ_{JA} ($^oC/W$)
SOIC Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

6. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 7) TEST CONDITIONS		MIN	(NOTE 8) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^oC$ to 85^oC, $V_{CC} = 5.0V \pm 10\%$							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 10) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O, (Note 10) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 10) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O, (Note 10) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH} I_{BHL}	Bus Hold Input (Note 10) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
			V_{IN} = 0.8V	-50	-	-	µA
High Impedance Output Current (Three-State) (Note 11)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 8), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 8), V_{OUT} = GND		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16501T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 7) TEST CONDITIONS		MIN	(NOTE 8) TYP	MAX	UNITS
CD74FCT162501T, CD74FCT162H501T, OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 12)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 12)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 12)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 12)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 13)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 14)	I_{CCD}	V_{CC} = Max, Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 16)	I_C	V_{CC} = Max, Output Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND One Bit Toggling f_I = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.8	1.7 (Note 15)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	4.2 (Note 15)	mA
		V_{CC} = Max, Output Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND 18 Bits Toggling f_I = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	6.5 (Note 15)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	8.5	20.8 (Note 15)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 17) TEST CONDITIONS	AT (NOTE 18) MIN	AT MAX	CT (NOTE 18) MIN	CT MAX	DT (NOTE 18) MIN	DT MAX	ET (NOTE 18) MIN	ET MAX	UNITS
CLKAB or CLKBA Frequency	f_{MAX}	C_L = 50pF R_L = 500Ω	-	150	-	150	-	150	-	150	MHz
Propagation Delay A_X to B_X or B_X to A_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	5.1	1.5	4.6	1.5	4.1	1.5	3.8	ns
Propagation Delay LEBA to A_X, LEAB to B_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
Propagation Delay CLKBA to A_X, CLKAB to B_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns

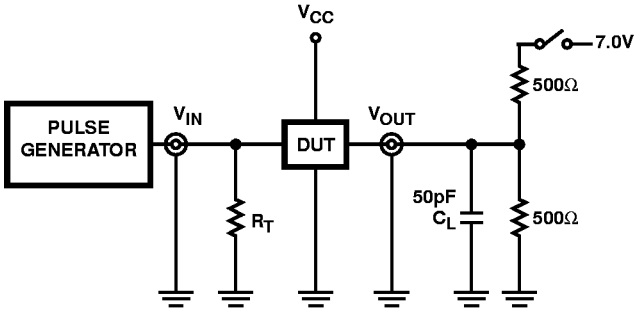
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 17) TEST CONDITIONS	AT (NOTE 18) MIN	AT MAX	CT (NOTE 18) MIN	CT MAX	DT (NOTE 18) MIN	DT MAX	ET (NOTE 18) MIN	ET MAX	UNITS
Output Enable Time $\overline{OEBA}$ to A_X, OEAB to Bx	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	5.6	1.5	5.2	1.5	4.8	ns
Output Disable Time (Note 14) $\overline{OEBA}$ to A_X, OEAB to B_X	t_{PHZ} t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	5.6	1.5	5.2	1.5	5.2	1.5	5.2	ns
Setup Time HIGH or LOW A_X to CLKAB, B_X to CLKBA	t_{SU}	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	3.0	-	2.4	-	ns
Hold Time HIGH or LOW A_X to CLKAB, B_X to CLKBA	t_H	C_L = 50pF R_L = 500Ω	0	-	0	-	0	-	0	-	ns
Setup Time HIGH or LOW, A_X to LEAB, B_X to LEBA, Clock HIGH	t_{SU}	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	3.0	-	2.0	-	ns
Setup Time HIGH or LOW, A_X to LEAB, B_X to LEBA, Clock LOW	t_{SU}	C_L = 50pF R_L = 500Ω	1.5	-	1.5	-	1.5	-	1.5	-	ns
Hold Time HIGH or LOW, Ax to LEAB, Bx to LEBA	t_H	C_L = 50pF R_L = 500Ω	1.5	-	1.5	-	1.5	-	0.5	-	ns
LEAB or LEBA Pulse Width HIGH (Note 19)	t_W	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	3.0	-	3.0	-	ns
CLKAB or CLKBA Pulse Width HIGH or LOW (Note 19)	t_W	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	3.0	-	3.0	-	ns
Output Skew (Note 20)	$t_{SK(O)}$	C_L = 50pF R_L = 500Ω	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

7. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
8. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
9. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
10. Pins with Bus Hold are identified in the Pin Description.
11. This specification does not apply to bidirectional functionalities with Bus Hold.
12. This parameter is determined by device characterization but is not production tested.
13. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
15. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
16. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
17. See test circuit and wave forms.
18. Minimum limits are guaranteed but not tested on Propagation Delays.
19. This parameter is guaranteed but not production tested.
20. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

21. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

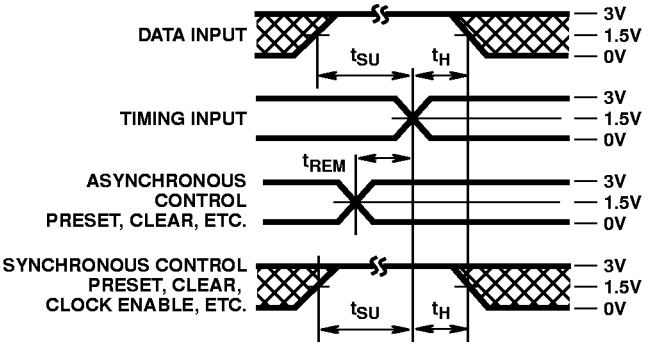


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

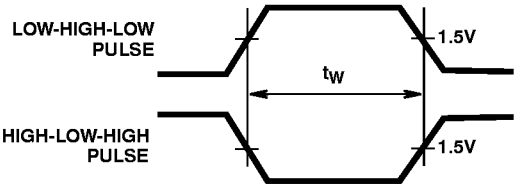


FIGURE 3. PULSE WIDTH

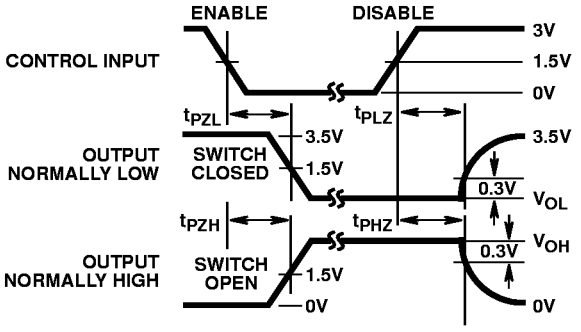


FIGURE 4. ENABLE AND DISABLE TIMING

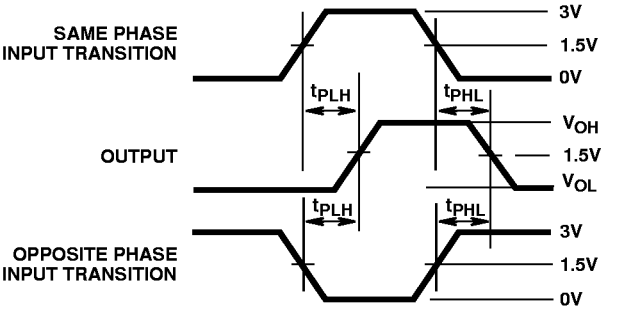


FIGURE 5. PROPAGATION DELAY