APPENDIX A
ELECTRICAL CHARACTERISTICS

Table A-1 Operating Conditions

Symbol	Definition	Conditions	Min	Typ	Max	Units
V_{BATT}	Voltage at battery pin during transmit operation	Rs = 20 Ω max. (protection circuit)	7.0	12.0	26.5	V
	Voltage at battery pin during receive operation	Rs = 20 Ω max. (protection circuit)	4.9	12.0	26.5	V
V_{CC}, V_{DD}	Transceiver, logic supplies	—	4.75	5.0	5.25	V
PC_{MAX}	Maximum continuous power dissipation	7.8 kHz bus waveform (50% duty cycle); 4.00 MHz resonator; 16-volt battery	—	—	333	mW
I_{BATT}, standby	Battery standby current	DLC in standby mode	—	3	5	µA
I_{BATT}, draw	Battery current draw	7.8 kHz bus waveform (50% duty cycle); 4.00 MHz resonator; 16-volt battery	—	3.5	50	mA
I_{DD}, draw	Logic current draw	100% bus utilization 4.00 MHz resonator	—	1.5	4	mA
I_{DD}, draw, slp[1]	Logic current draw, standby mode	DLC in sleep mode	—	3	5	µA
I_{CC}, draw	Transceiver current draw	100% bus utilization 4.00 MHz resonator	—	0.3	1	mA
I_{CC}, draw, slp	Transceiver current draw, standby mode	DLC in sleep mode	—	40	55	µA
I_{PSEN}, source	PSEN pin max source	V_{BATT} = 9 V Rseries = 33 kΩ	10	—	500	µA
I_{OLPSEN}	PSEN leakage	Standby mode, power supply off	–5	—	5	µA
V_{PSEN}	PSEN pin output voltage	V_{BATT} = 9 V Rseries = 33 kΩ	8.3	—	—	V
V_{LH}	Input range on all logic pins	—	–0.5	—	5.75	V
T_{ST}	Storage temperature range	—	–65	—	150	°C
T_J	Maximum junction temperature	—	—	—	150	°C
T_A	Operating temperature range	—	–40	—	125	°C
I_{BAT}, sleep	Battery sleep current	DLC in sleep mode	—	—	5	mA

NOTES:
1. Measured with no activity on the host /DLC interface lines.

Table A-2 Electrical Characteristics

Symbol	Description	Conditions	Min	Max	Units
V_{OH}[1]	Minimum guaranteed output high voltage	I_{OH}= −200 µA	V_{DD} − 0.8V	—	V
V_{OL}	Maximum guaranteed output low voltage	I_{OL} = 1.6 mA	—	0.4	V
V_{IH}	Minimum guaranteed input high voltage	I_{IN} = 10 µA	V_{DD} x 0.7V	—	V
V_{IL}	Maximum guaranteed input low voltage	I_{IN} = 10 µA	—	0.8	V
I_{IN} (except OSC1, $\overline{CS}$)	Input current limits	—	−10	10	µA
$I_{IH, OSC1}$	Maximum guaranteed input high current	V_{DD} = 4.75 to 5.25 V	0.525	10.50	µA
$I_{IL, OSC1}$	Maximum guaranteed input low current	V_{DD} = 4.75 to 5.25 V	−10.50	−0.525	µA
$I_{IN\overline{CS}}$	Chip select input current limit	—	−650	50	µA
I_{OZ} (except OSC1)	Output leakage high-Z	V_{OUT} to GND	−10	10	µA
C_I	Digital input capacitance	—	—	8	pF
C_{IO}	Digital input/output capacitance	—	—	10	pF
C_{LOAD}	Maximum load capacitance	—	—	100	pF

NOTES:
1. Interrupt request line is an open drain output; therefore, V_{OH} is not applicable.

Table A-3 Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{BATT}	Supply voltage	−0.5	26.5	V
V_{BATT}	Supply voltage (t ≤ 1 ms)	—	40.0	V
V_{CC},V_{DD}	Supply voltage	−0.5	5.75	V
T_{STG}	Storage temperature range	−65	+150.0	°C
T_J	Maximum junction temperature	—	+150.0	°C

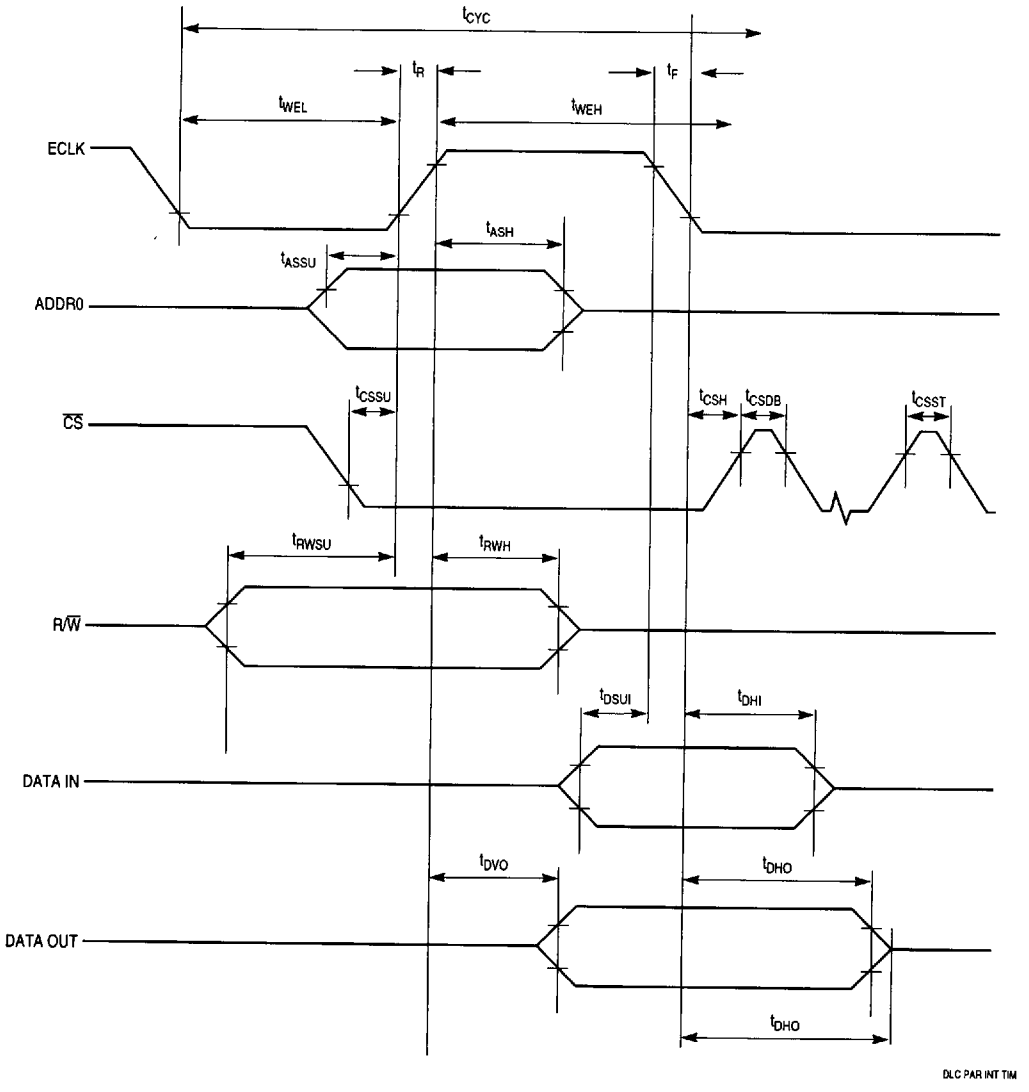


Figure A-1 Parallel Interface Timing

Table A-4 Parallel Interface Parameters

Symbol	Description	Pin	Min	Max	Units
t_{CYC}	E-clock cycle time	EC	238	—	ns
t_{WEL}	E-clock pulse width low	EC	105	—	ns
t_{WEH}	E-clock pulse width high	EC	100	—	ns
$t_{R,F}$	E-clock rise and fall time	EC	0	20	ns
t_{ASSU}	Address select setup time	A0	20	—	ns
t_{ASH}	Address select hold time	A0	20	—	ns
t_{CSSU}	Chip-select setup time	$\overline{CS}$	5	—	ns
t_{CSH}	Chip-select hold time	$\overline{CS}$	5	—	ns
t_{CSDB}	Chip-select double[1]	$\overline{CS}$	0	60	ns
t_{CSST}	Chip-select status time[2, 3]	$\overline{CS}$	3	—	µs
t_{RWSU}	R/$\overline{W}$ setup time	R/$\overline{W}$	25	—	ns
t_{RWH}	R/$\overline{W}$ hold time	R/$\overline{W}$	20	—	ns
t_{DSUI}	Data in setup time	D0–D7	45	—	ns
t_{DHI}	Data in hold time	D0–D7	15	—	ns
t_{DVO}	Data out valid time	D0–D7	—	75	ns
t_{DHO}	Data out hold time	D0–D7	5	—	ns
t_{DTO}	Data out three-state time	D0–D7	—	40	ns

NOTES:

1. Within double-byte reads and writes.
2. Between successive commands; also between consecutive "auto-finishes" of data in DLC parallel mode.
3. Needed between successive status byte reads to properly update status.

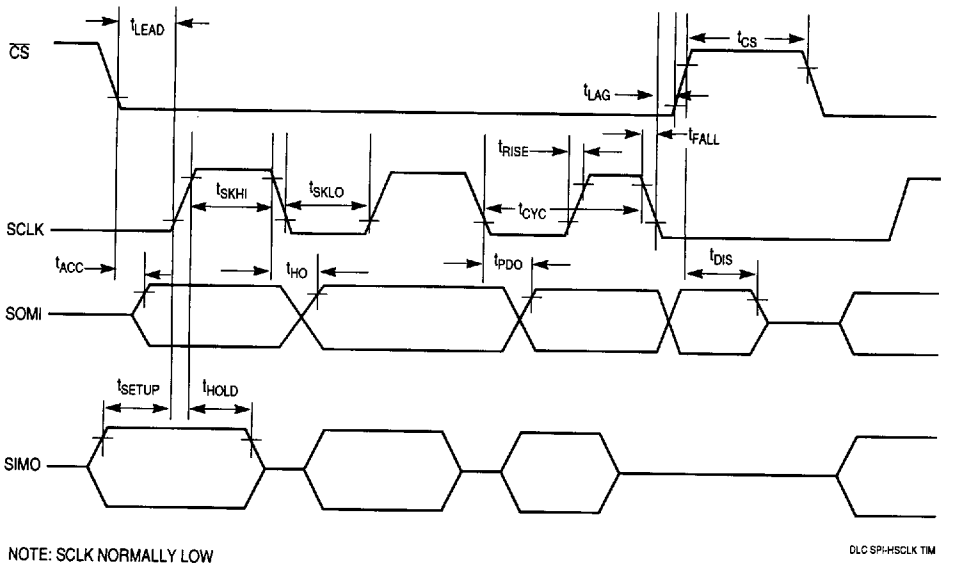


Figure A-2 SPI Timing — Active High SCLK

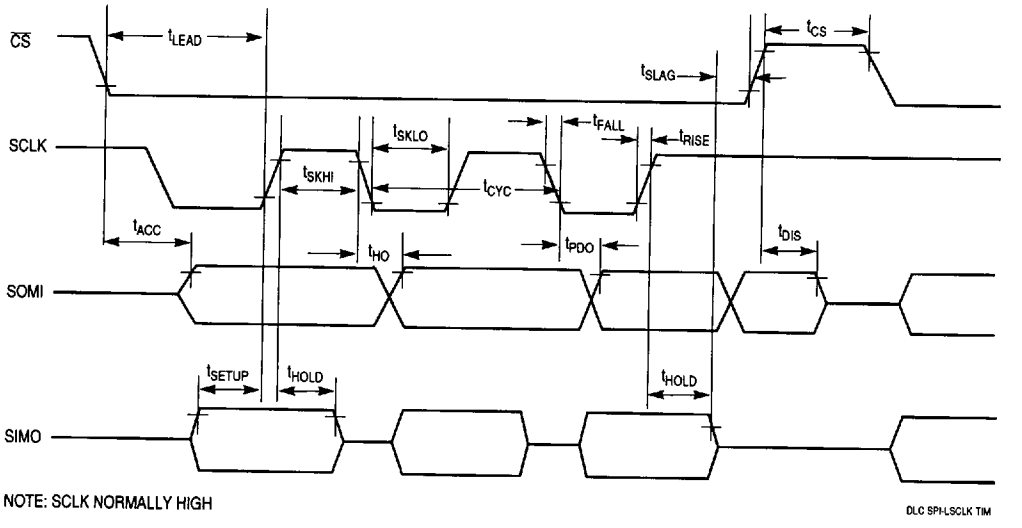


Figure A-3 SPI Timing — Active Low SCLK

Table A-5 Serial Interface Parameters

Symbol	Description	Min	Max	Units
t_{CS}	Minimum time between consecutive $\overline{CS}$ assertions	3.0	—	µs
t_{CYC}	Minimum SCK cycle time[1]	238	—	ns
t_{SKHI}	Minimum clock high time	80	—	ns
t_{SKLO}	Minimum clock low time	80	—	ns
t_{LEAD}	Minimum enable lead time	100	—	ns
t_{LAG}	Minimum enable lag time	100	—	ns
t_{ACC}	Access time	—	60	ns
t_{PDO}	Maximum data out delay time	—	59	ns
t_{HO}	Minimum data out hold time	0	—	ns
t_{DIS}	Maximum data out disable time	—	240	ns
t_{SETUP}	Minimum data setup time	30	—	ns
t_{HOLD}	Minimum data hold time	30	—	ns
t_{RISE}	Maximum time for input to go from V_{OL} to V_{OH}	—	25	ns
t_{FALL}	Maximum time for input to go from V_{OH} to V_{OL}	—	25	ns
t_{SLAG}	Minimum time after data hold time that $\overline{CS}$ may be negated	100	—	ns

NOTES:
1. Maximum SPI frequency is 4.2 MHz.

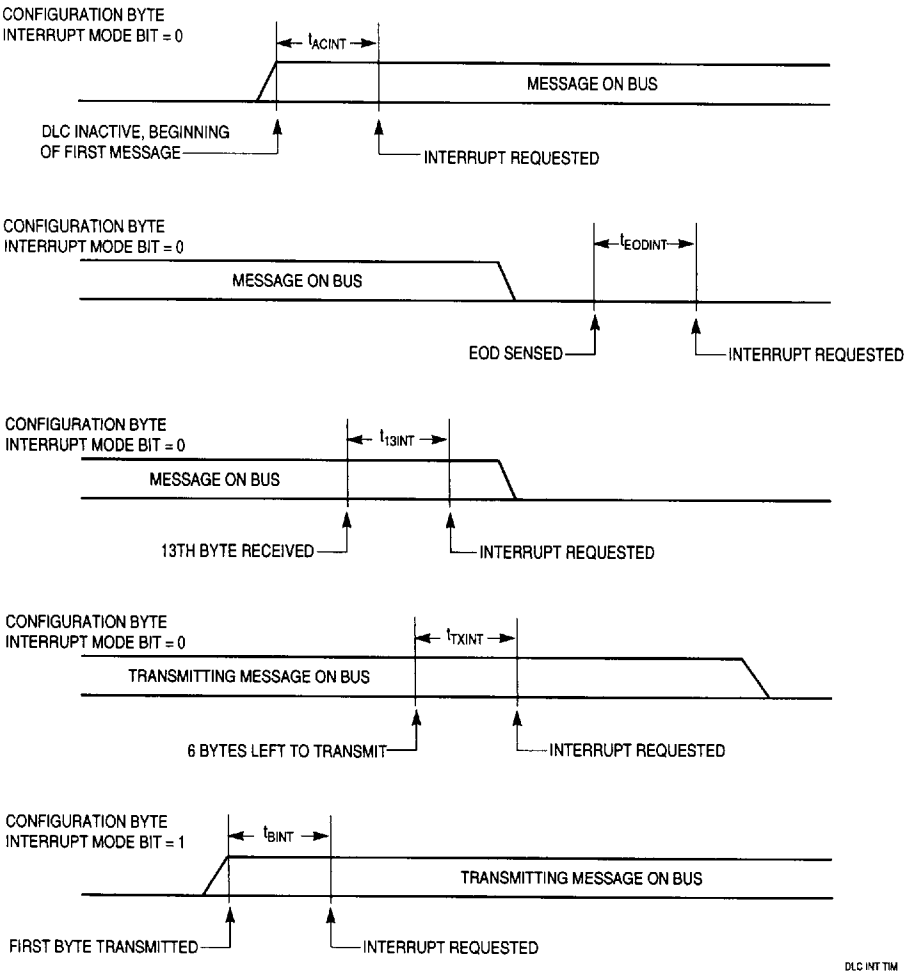


Figure A-4 DLC Interrupt Timing

Table A-6 Standby and Interrupt Timing

Symbol	Description	Min	Max	Units
t_{ACDLY}	Period from detection of bus activity until assertion of PSEN, or period from application of 5 Vdc until assertion of PSEN	—	5	µs
t_{ACINT}	Period from detection of bus activity by a DLC in standby condition until $\overline{INT}$ assertion	—	105	µs
t_{EODINT}	Period from detection of EOD on the bus until $\overline{INT}$ assertion	—	5	µs
t_{13INT}	Period from receipt of 13th byte until $\overline{INT}$ assertion	—	5	µs
t_{TXINT}	Period from when there are six bytes left to transmit until $\overline{INT}$ assertion	—	5	µs
t_{BINT}	Period from receipt of first byte until $\overline{INT}$ assertion	—	5	µs

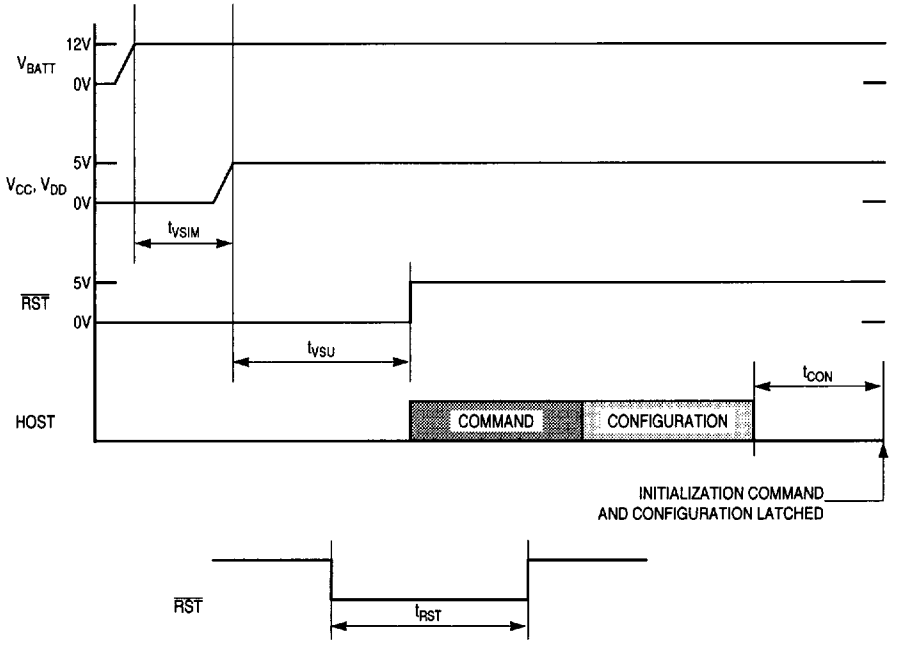


Figure A-5 Reset Timing

Table A-7 Reset Timing

Symbol	Description	Min	Max	Units
t_{VSIM}	V_{DD}, V_{SS} simultaneous switch delay	6	10	ms
t_{VSU}	V_{DD}, V_{SS} set up time	50	100	ms
t_{CON}	Immediate configuration time	300	1200	µs
t_{RST}	Reset pulse width	1	—	µs

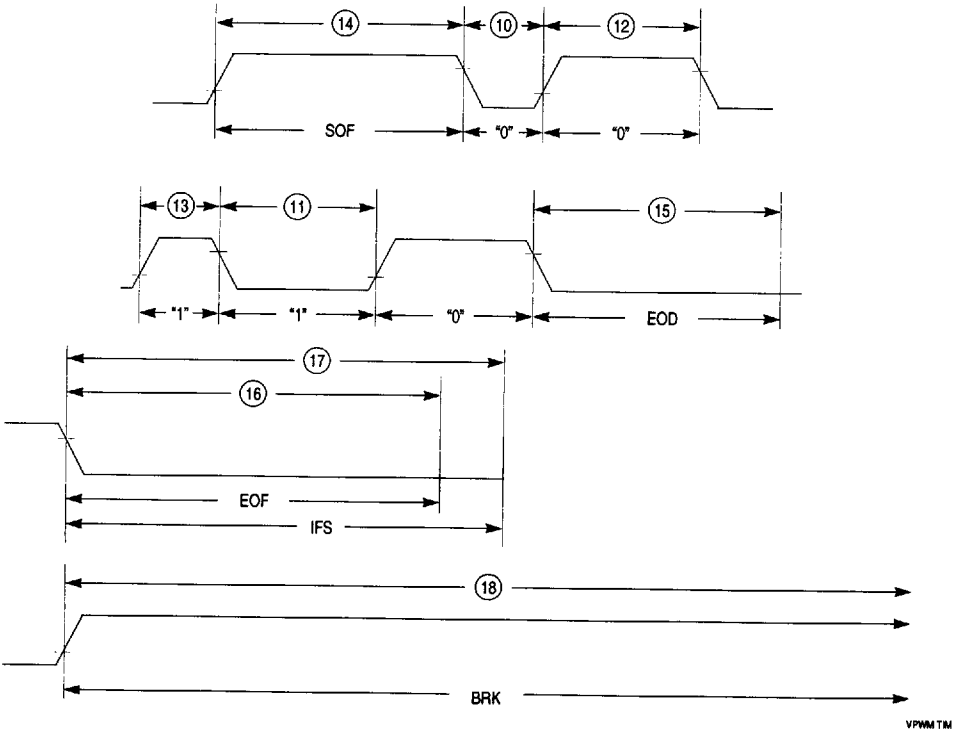


Figure A-6 Variable Pulse-Width Modulation (VPW) Symbol Timings

Table A-8 Transceiver Requirements (DC)

Symbol	Description	Conditions	Min	Max	Units
V_{OH}	Guaranteed output high voltage	100% bus utilization, 4 MHz (V_{BATT} = 9 to 26.5V)	6.25	8.0	V
		100% bus utilization, 4 MHz (V_{BATT} = 7 to 9V)	5.25	8.0	
$V_{OL, MAX}$	Maximum guaranteed output low voltage	100% bus utilization, 4 MHz	—	1.5	V
$V_{IL, MAX}$	Maximum input low voltage	V_{CC} = 4.75 to 5.25 V	—	3.5	V
$V_{IH, MIN}$	Minimum input high voltage	V_{CC} = 4.75 to 5.25 V	4.25	—	V
V_T	Nominal receiver trip point	–	3.875	—	V

Table A-9 Transmitter VPW Symbol Timings

(V_{BATT} = 12V, V_{CC} = 5.0V, V_{SS} = 0V, T_A = 25°C, unless otherwise noted.)

Characteristic	Number	Symbol	Min	Typical	Max	Unit
Passive logic 0	10	t_{TVP1}	58.0	64.0	70.0	µs
Passive logic 1	11	t_{TVP2}	122.0	128.0	134.0	µs
Active logic 0	12	t_{TVA1}	122.0	128.0	134.0	µs
Active logic 1	13	t_{TVA2}	58.0	64.0	70.0	µs
Start of frame (SOF)	14	t_{TVA3}	193.0	200.00	207.0	µs
End of data (EOD)	15	t_{TVP3}	193.0	200.0	207.0	µs
End of frame	16	t_{TV4}	271.0	280.0	289.0	µs
Inter-frame separator (IFS)	17	t_{TV6}	300.0	—	—	µs
Break (BRK)	18	t_{TV7}	—	1200	—	µs

Table A-10 Receiver VPW Symbol Timings

(V_{BATT} = 12V, V_{CC} = 5.0V, V_{SS} = 0V, T_A = 25°C, unless otherwise noted.)

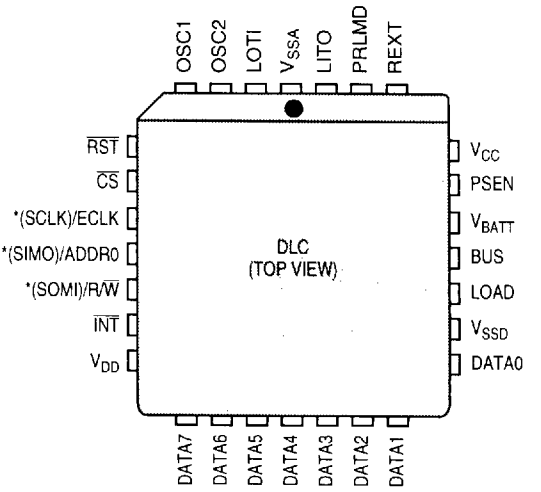
Characteristic	Number	Symbol[1]	Min	Typical	Max	Unit
Passive logic 0	10	t_{RVP1}	34.0	64.0	96.0	µs
Passive logic 1	11	t_{RVP2}	96.0	128.0	163.0	µs
Active logic 0	12	t_{RVA1}	96.0	128.0	163.0	µs
Active logic 1	13	t_{RVA2}	34.0	64.0	96.0	µs
Start of frame (SOF)	14	t_{RVA3}	163.0	200.0	239.0	µs
End of data (EOD)	15	t_{RVP3}	163.0	200.0	239.0	µs
End of frame	16	t_{RV4}	239.0	280.0	320.0	µs
Break	18	t_{RV7}	768.0	–	–	µs

NOTES:
1. The receiver symbol timing boundaries are subject to an uncertainty of ± 1µs due to sampling considerations.

APPENDIX B
MECHANICAL DATA AND ORDERING INFORMATION

The MC68HC58 is available in two package options, a 28-pin PLCC (plastic leaded chip carrier) and a 28-pin SOIC (small outline integrated circuit). Refer to **Figures B-1** and **B-2**. **Figures B-3** and **B-4** show the corresponding dimensional drawings. Ordering information is available in **Table B-1**.

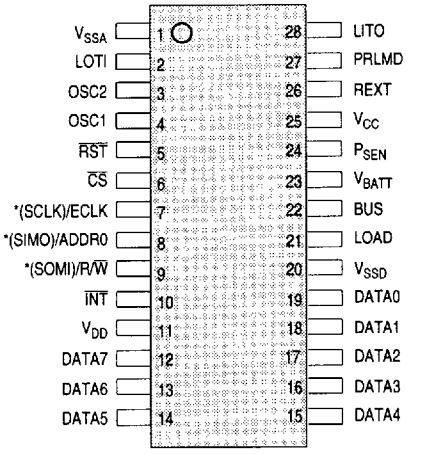
B.1 Pin Assignments



* ( ) INDICATES PIN ASSIGNMENTS FOR SERIAL MODE OPERATION

DLC PIN ASSIGNMENT

Figure B-1 MC68HC58 28-Pin PLCC

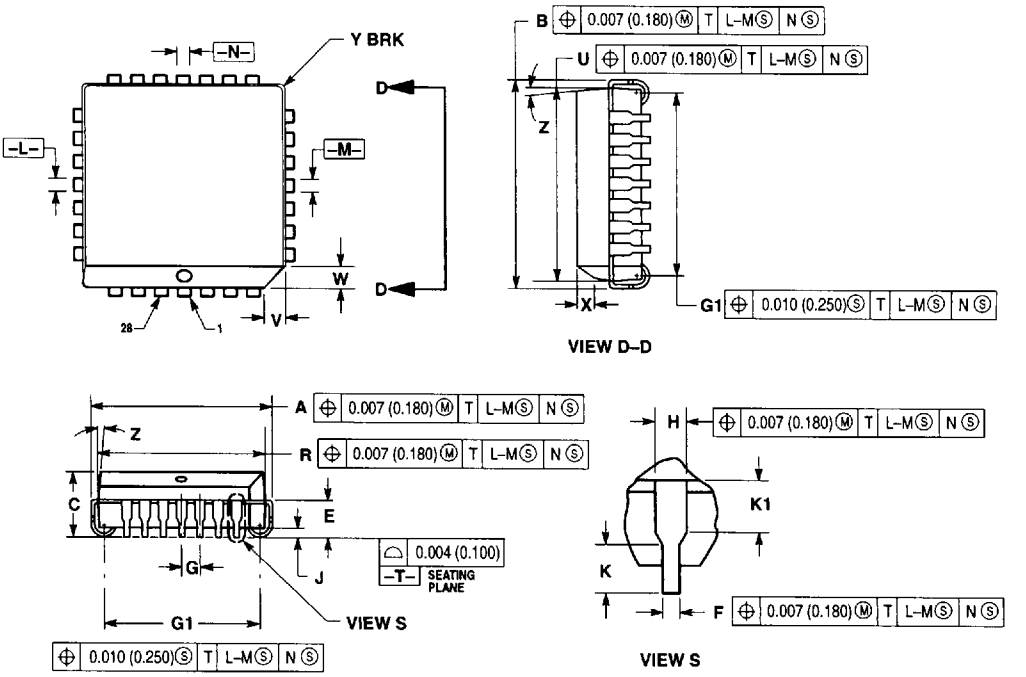


* ( ) INDICATES PIN ASSIGNMENTS FOR SERIAL MODE OPERATION

DLCP 28-PIN SOIC

Figure B-2 MC68HC58 28-Pin SOIC

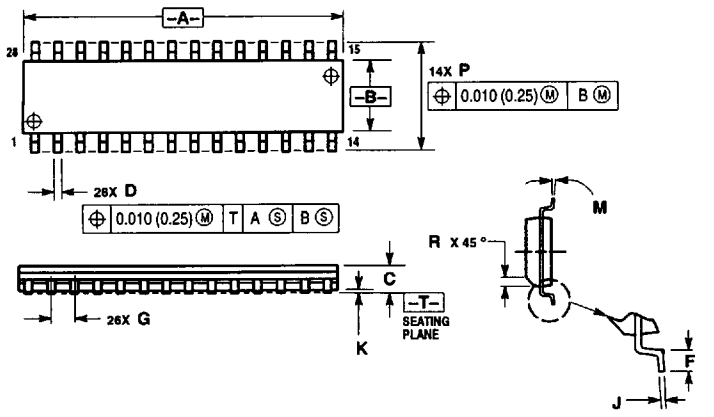
5.5 Package Dimensions



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

Figure B-3 Case Outline #776-02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.01	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Figure B-4 Case Outline #751F-04

B.2 Obtaining Updated MC68HC58 Mechanical Information

Although all devices manufactured by Motorola conform to current JEDEC standards, complete mechanical information regarding MC68HC58 data link controller is available through Motorola's Design-Net.

To download updated package specifications, perform the following steps:

1. Visit the Design-Net case outline database search engine at http://design-net.com/cgi-bin/cases.
2. Enter the case outline number, located in **Figures B-3** and **B-4** without the revision code (for example, 864A, not 864A-03) in the field next to the search button.
3. Download the file with the new package diagram.

B.3 Ordering Information

Table B-1 MC68HC58 Ordering Information

MC Order Information	Package	Description
MC68HC58	776-02	28-pin PLCC
	751F -04	28-pin SOIC