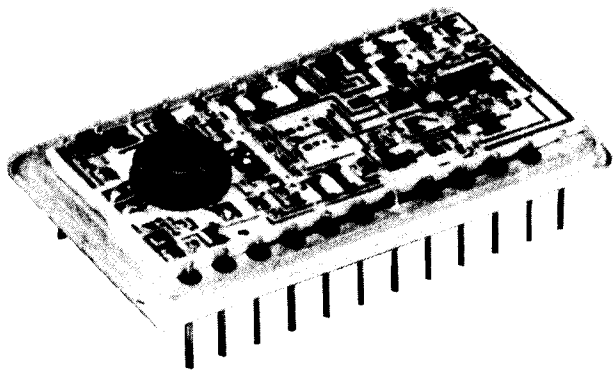
HYBRID VIDEO/PULSE SAMPLE/HOLD
30 ns Acquisition Time; 20 MHz Sampling Rate



FEATURES

- *20 pS APETURE TIME UNCERTAINTY (JITTER)*
- *0.2 mV/μs DROOP*
- *20 ns SETTLING TIME TO 0.1%*
- *0.05% LINEARITY ERROR*
- *INPUT BUFFER AMPLIFIER*

DESCRIPTION

The SH-8518 video/pulse sample and hold amplifier is the smallest video sample and hold module available, complete in a 24-pin double DIP hermetically sealed metal package. The module includes all necessary components, including the holding capacitor, FET amplifiers to buffer the input and output signals, and a TTL compatible gate control. It is a highly reliability device manufactured and processed to meet the requirements of MIL-STD-883.

APPLICATIONS

The SH-8518 is well suited for a variety of video processing applications in communications, radar, and television systems. It can be used very effectively in pulse processing and pulse stretching applications, as in radar systems or transient analyzers. With a maximum sampling rate of 20MHz, the SH-8518 is ideal for multiplexed A/D converter systems, and for use with high speed A/D converters such as DDC's 8-bit hybrid ADH-8512.

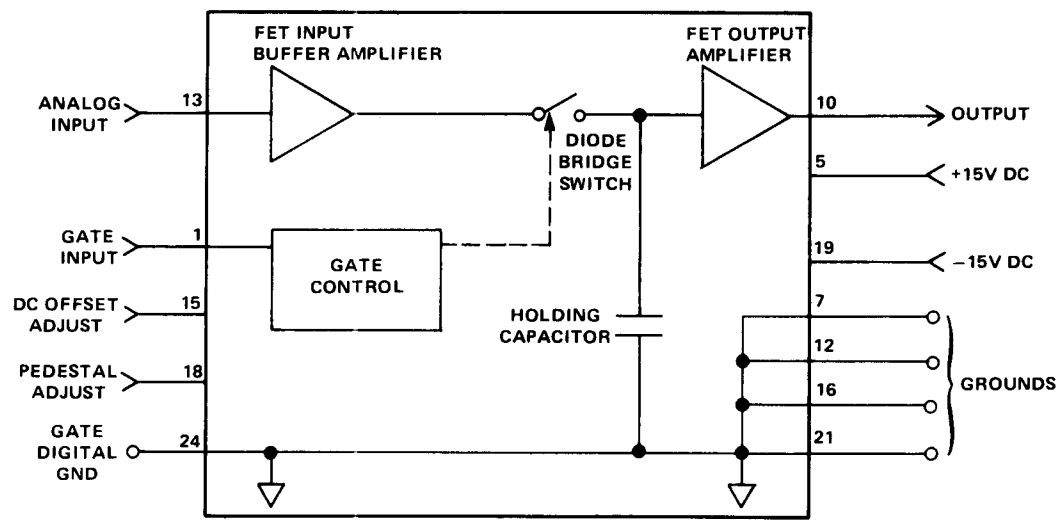


FIGURE 1. SH-8518, BLOCK DIAGRAM

SH-8518 SPECIFICATIONS

At 25° C case temperature and rated supplies

PARAMETER	UNIT	VALUE
ACCURACY		
Gain		+0.975 no load: +0.96 typ with 500-ohm rated road
Gain Tempco	PPM/°C	25 typ; 50 max
Linearity Error:		
For ±2.5V Input	% of F.S.	< 0.05 typ; 0.1 max
For ±3.5V Input	% of F.S.	0.2 max with ±5V max sample-to-sample change
Linearity Tempco	PPM/°C	5 typ; 15 max
DC Offset (trimmable to zero)	mV	20 typ; 100 max
DC Offset Tempco	µV/°C	40 typ; 100 max
Pedestal (trimmable to zero)	mV	100 typ; 300 max
Pedestal Tempco	µV/°C	50 typ; 100 max
DYNAMICS		
Small-Signal Bandwidth (f_t)	MHz	100 typ; 80 min
Slew Rate	V/µs	600 typ; 400 min
Update Change	V	±5 max
Max Sampling Rate	MHz	15 min; 20 typ
Min Cycle Time	ns	66.7 max; 50 typ
Duty Cycle (Ratio of Sample Time to Cycle Time)	%	< 80
Max Sample Time	ns	100
Acquisition Turn-On Delay	ns	8 typ; 10 max
Acquisition Time (T_A) to 0.1% of Final Value (Includes Delay):		
±5V Input Change	ns	30 typ; 35 max
±1V Input Change	ns	25 typ; 30 max
Aperture Time Delay (T_a)	ns	5 typ; 8 max
Aperture Time Delay Uncertainty (Jitter) (ΔT_a)	ps	20 typ; 35 max
Feedthrough Attenuation in Hold Mode	db	66 typ; 60 min, DC through 10 MHz
Settling Time (To within ±0.1% of Final Value):		
For ±5V Input Change	ns	30 max
For ±1V Input Change	ns	20 max
Droop Rate at 25°C (Case)	mV/µs	0.2 typ; 5 max
Droop Rate Temperature Dependence		Doubles every 10°C

PARAMETER	UNIT	VALUE
ANALOG INPUT		
Signal Voltage Range	V	± 2.5 max for full linearity; ± 3.5 max for reduced linearity (see linearity specification)
Impedance		10^{10} Ω min plus 5 pf max
GATE INPUT		
Type		TTL Compatible
Load		2 standard TTL unit loads max
Logic Levels		Logic 1 = sample mode Logic 0 = Hold mode
OUTPUT		
Max Voltage	V	±3.5 min
Max Current	mA	±5 min
Impedance	Ω	10 max
Short Circuit Protection to Ground		Up to max allowable operating case temperature
POWER REQUIREMENTS		
Supply Voltages	VDC	+15±5% / −15 ±5%
Absolute Max Voltage	VDC	+18 / −18
Current Max	mA	55 typ; (1) / 50 typ;
Power Dissipation	W	70 max / 60 max 1.6 average
TEMPERATURE RANGE (CASE)		
Operating:		
−1 Option	°C	-55 to +85
−3 Option	°C	0 to +70
Storage	°C	-55 to +125
Thermal Resistance	°C/W	θCA = 30
PHYSICAL		
Type		24-pin double DIP
Size	inch	1.4 x 0.8 x 0.28 (3.6 x 2.0 x 0.71 cm)
Weight	oz	0.42 (11.9g) typ

NOTES: (1) 55 mA for 10% T/H duty cycle.
125 mA for 50% T/H duty cycle.

TECHNICAL INFORMATION

1. INTRODUCTION

The SH-8518 Sample and Hold (S/H) amplifier (Figure 1) consists basically of a voltage holding capacitor connected to the input signal through a switch. The input signal and output voltage from the holding capacitor are both buffered by FET amplifiers. The switch is controlled by a TTL logic gate signal which determines whether the capacitor and therefore output voltage follows the input signal (switch closed, logic 1) or remains constant, retaining a particular value of the input voltage (switch open, logic 0).

In a S/H amplifier such as the SH-8518 the gate is AC coupled to the switch, so that very short gate pulses are used and the input signal is sampled only briefly. This usually allows shorter acquisition times and greater sampling rates than with a track and hold amplifier in which the gate is DC coupled to the switch. Because of the AC coupling, the SH-8518 sample time must be less than 100ns. For applications requiring longer sample times, consider DDC's track and hold amplifiers, which have no limitation on the tracking time.

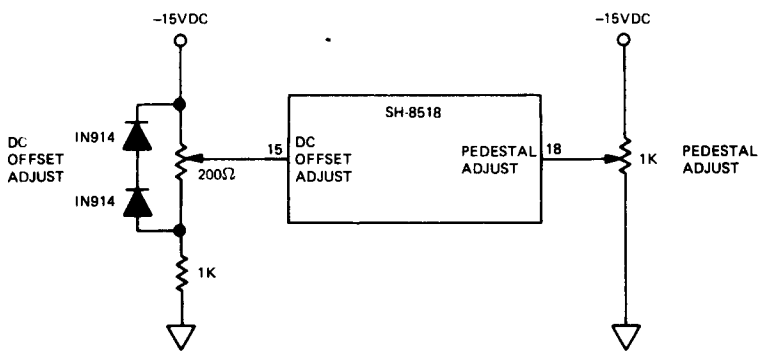


FIGURE 2. TRIM ADJUSTMENT CIRCUITS

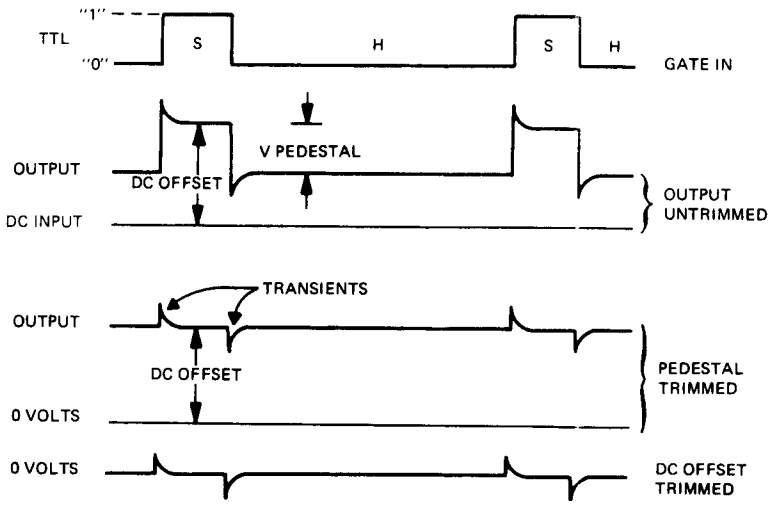
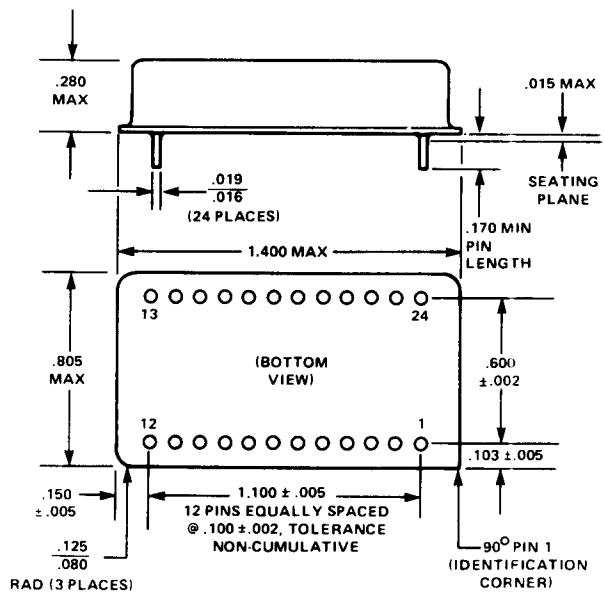


FIGURE 3. SCOPE TRACES DURING OUTPUT TRIM ADJUSTMENTS

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions are shown in inches.
2. Load identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

ORDERING INFORMATION

SH-8518-1 – 883B

Reliability Grade:
- 883B = Fully compliant with MIL-STD-883.
- –B = Screened to MIL-STD-883 but without QCI testing.
- Blank = Screened to MIL-STD-883 but without pre burn-in testing, burn-in, and QCI testing.

Operating Temperature Range (case):
- –1 = 55°C to +85°C
- –3 = 0°C to +70°C

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The terminology, signal relationships, and major design considerations for sample/holds such as the SH-8518 are discussed in the Background Information at the front of the S/H and T/H section of this catalog.

2. GROUND CONNECTIONS

To minimize inadvertent coupling of a gate signal onto an output signal, connect the gate signal between pins 1 and 24 only. Do not connect any other grounds to pin 24. Analog input, output, and supply voltage grounds can be connected to ground pins 7, 12, 16 and 21 as convenient. These four pins should be connected together externally to minimize impedances. All grounds are tied together internally and connected to the case.

3. TRIM ADJUSTMENTS

The DC Offset and Pedestal are trimmed at the factory to within the limits listed in the specifications table. Further adjustments may be made after installation using the trim adjustment circuit shown in Figure 2. Connect the Output (pin 10) to an oscilloscope and ground the Analog Input (pin 13). Apply approximately 30ns positive TTL pulse at a rate of about 1MHz to the Gate Input (pin 1). Vary the Pedestal Adjust potentiometer to minimize the pedestal and the DC Offset potentiometer to trim the offset as depicted in Figure 3.

4. RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All SH-8518 hybrids are built in accordance with requirements of MIL-STD-883.

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Gate Input	13	Analog Input
2	N.C.	14	N.C.
3	N.C.	15	DC Offset Adjust
4	N.C.	16	Ground
5	+15VDC	17	N.C.
6	N.C.	18	Pedestal Adjust
7	Ground	19	-15VDC
8	N.C.	20	N.C.
9	N.C.	21	Ground
10	Output	22	N.C.
11	N.C.	23	N.C.
12	Ground	24	Gate Digital Ground

All grounds are tied to the case.