Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

ICL8052/ICL71C03, ICL8068/ICL71C03

August 1997

Precision $4^1/_2$ Digit, A/D Converter

Features

- Typically Less Than $2\mu V_{P-P}$ Noise (200.00mV Full Scale, ICL8068)
- Accuracy Guaranteed to ±1 Count Over Entire ±20,000 Counts (2.0000V Full Scale)
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero Count for Precise Null Detection
- Single Reference Voltage Required
- Over-Range and Under-Range Signals Available for Auto-Ranging Capability
- All Outputs TTL Compatible
- Medium Quality Reference, 40ppm (Typ) on Board
- Blinking Display Gives Visual Indication of Over Range
- Six Auxiliary Inputs/Outputs are Available for Interfacing to UARTs, Microprocessors or Other Complex Circuitry
- 5pA Input Current (Typ) (8052A)

Description

The ICL8052 or ICL8068/ICL71C03 chip pairs with their multiplexed BCD output and digit drivers are ideally suited for the visual display DVM/DPM market. The outstanding $4^1/_2$ digit accuracy, 200.00mV to 2.0000V full scale capability, auto-zero and auto-polarity combine with true ratiometric operation, almost ideal differential linearity and time-proven dual slope conversion. Use of these chip pairs eliminates clock feedthrough problems, and avoids the critical board layout usually required to minimize charge injection.

When only 2000 counts of resolution are required, the 71C03 can be wired for $3^1/_2$ digits and give up to 30 readings/sec., making it ideally suited for a wide variety of applications.

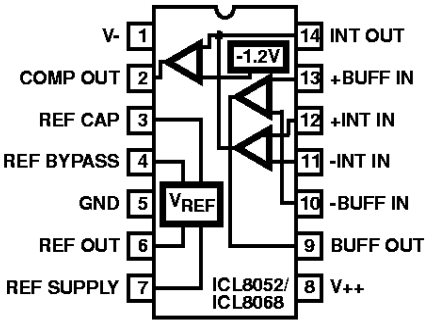
The ICL71C03 is an improved CMOS plug-in replacement for the ICL7103 and should be used in all new designs.

Ordering Information

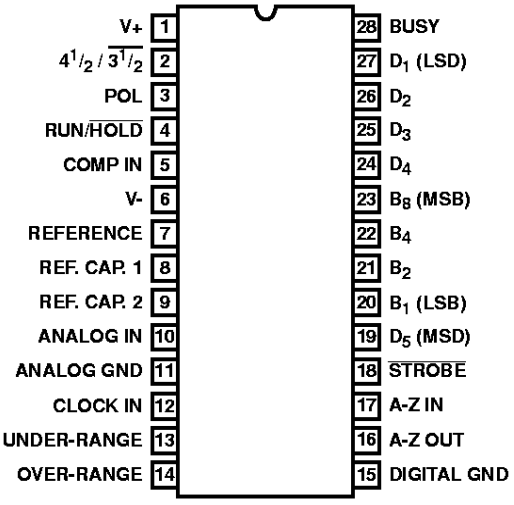
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ICL8052CPD	0 to 70	14 Ld PDIP	E14.3
ICL8052CDD	0 to 70	14 Ld CERDIP	F14.3
ICL8052ACPD	0 to 70	14 Ld PDIP	E14.3
ICL8052ACDD	0 to 70	14 Ld CERDIP	F14.3
ICL8068CDD	0 to 70	14 Ld CERDIP	F14.3
ICL8068ACDD	0 to 70	14 Ld CERDIP	F14.3
ICL8068ACJD	0 to 70	14 Ld CERDIP	F14.3
ICL71C03CPI	0 to 70	28 Ld PDIP	E28.6
ICL71C03ACPI	0 to 70	28 Ld PDIP	E28.6

Pinouts

ICL8052/ICL8068
(CERDIP, PDIP)
TOP VIEW



ICL71C03 (PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3081.1**

Functional Block Diagram

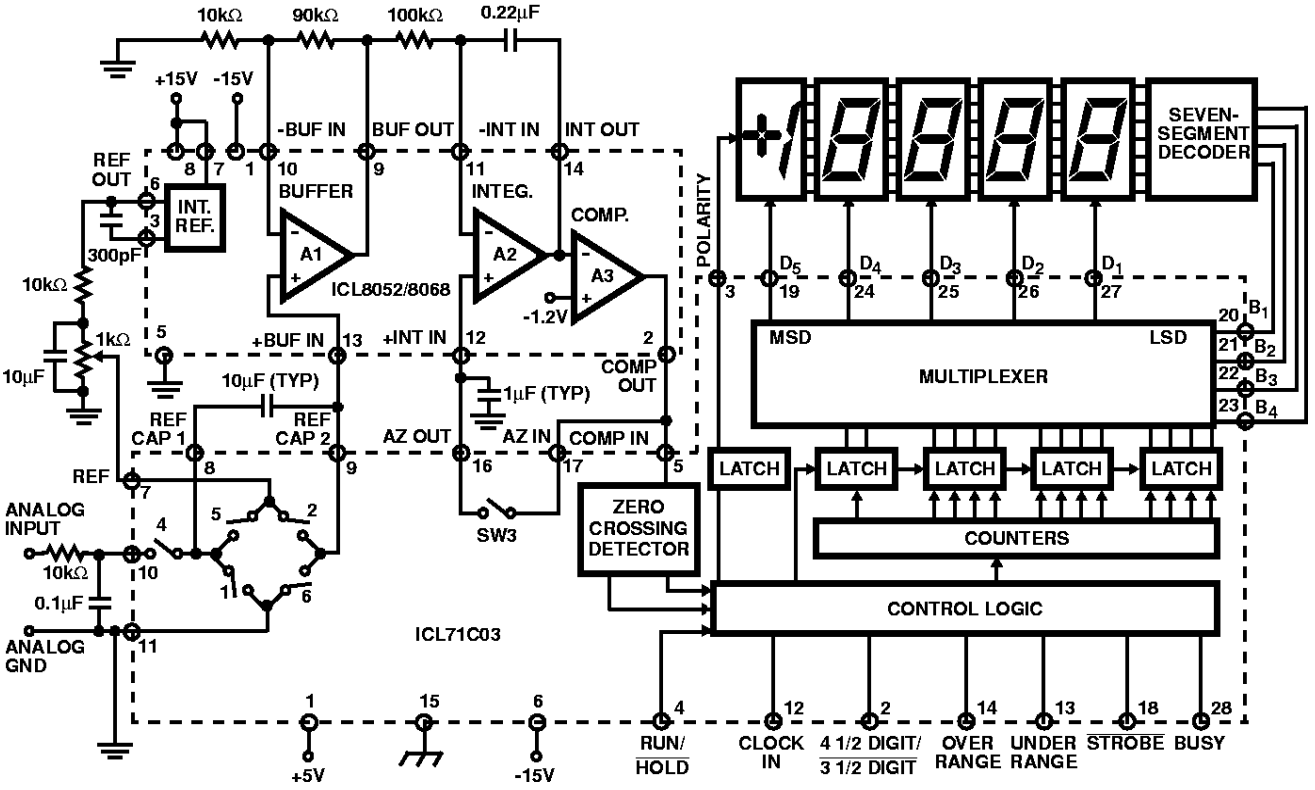


FIGURE 1.

Absolute Maximum Ratings

ICL8052, ICL8068

Supply Voltage . . . . . ±18V
Differential Input Voltage
(8068) . . . . . ±30V
(8052) . . . . . ±6V
Input Voltage (Note 1) . . . . . ±15V
Output Short Circuit Duration All Outputs (Note 2) . . . . . Indefinite

ICL71C03

Power Supply Voltage (GND to V+) 6.5V
Negative Supply Voltage (GND to V-) . . . . . -17V
Analog Input Voltage (Note 3) . . . . . V+ to V-
Digital Input Voltage (Note 4) . . . . . (GND - 0.3V) to (V+ + 0.3V)

Operating Conditions

Temperature Range . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
14 Ld PDIP Package	100	N/A
28 Ld PDIP Package	65	N/A

Maximum Storage Temperature . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply. Rating applies to 70°C ambient temperature.
3. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
4. Connecting any digital inputs or outputs to voltages greater then V+ or less than GND may cause destructive device latchup. For this reason it is recommended that the power supply to the ICL71C03 be established before any inputs from sources not on that supply are applied.
5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Clock In, Run/$\overline{\text{Hold}}$, 4 1/2 / $\overline{\text{3 1/2}}$	I_{INL}	V_{IN} = 0	-	0.2	0.6	mA
	I_{INH}	V_{IN} = +5V	-	0.1	10	µA
Comp. In Current	I_{INL}	V_{IN} = 0	-	0.1	10	µA
	I_{INH}	V_{IN} = +5V	-	0.1	10	µA
Threshold Voltage	V_{INTH}		-	2.5	-	V
All Outputs	V_{OL}	I_{OL} = 1.6mA	-	0.25	0.40	V
B_1, B_2, B_4, B_8, D_1, D_2, D_3, D_4, D_5	V_{OH}	I_{OH} = -1mA	2.4	4.2	-	V
Busy, $\overline{\text{Strobe}}$, Over-Range, Under-Range Polarity	V_{OH}	I_{OH} = -10µA	4.9	4.99	-	V
Switches 1, 3, 4, 5, 6	$r_{DS(ON)}$		-	400	-	Ω
Switch 2	$r_{DS(ON)}$		-	1200	-	Ω
Switch Leakage (All)	$I_{D(OFF)}$		-	2	-	pA
+5V Supply Range	V+		4	5	6	V
-15V Supply Range	V-		-5	-15	-18	V
+5V Supply Current	I+	f_{CLK} = 0	-	1.1	3	mA
-15V Supply Current	I-	f_{CLK} = 0	-	0.8	3	mA
Power Dissipation Capacitance	C_{PD}	vs Clock Frequency	-	40	-	pF
Clock Frequency (Note 6)			DC	2000	1200	kHz

NOTE:

6. This specification relates to the clock frequency range over which the ICL71C03(A) will correctly perform its various functions. See the "Max Clock Frequency" section under Component Value Selection for limitations on the clock frequency range in a system.

ICL8068 Electrical Specifications $V_{SUPPLY} = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	ICL8068			ICL8068A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER									
Input Offset Voltage	V_{OS}	$V_{CM} = 0V$	-	20	65	-	20	65	mV
Input Current (Either Input) (Note 7)	I_{IN}	$V_{CM} = 0V$	-	175	250	-	80	150	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10V$	70	90	-	70	90	-	dB
Non-Linear Component of Common-Mode Rejection Ratio (Note 8)		$V_{CM} = \pm2V$	-	110	-	-	110	-	dB
Large Signal Voltage Gain	A_V	$R_L = 50k\Omega$	20,000	-	-	20,000	-	-	V/V
Slew Rate	SR		-	6	-	-	6	-	V/µs
Unity Gain Bandwidth	GBW		-	2	-	-	2	-	MHz
Output Short-Circuit Current	I_{SC}		-	5	-	-	5	-	mA
COMPARATOR AMPLIFIER									
Small-Signal Voltage Gain	A_{VOL}	$R_L = 30k\Omega$	-	-	4000	-	-	-	V/V
Positive Output Voltage Swing	$+V_O$		12	13	-	12	13	-	V
Negative Output Voltage Swing	$-V_O$		-2.0	-2.6	-	-2.0	-2.6	-	V
VOLTAGE REFERENCE									
Output Voltage	V_O		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance	R_O		-	5	-	-	5	-	Ω
Temperature Coefficient	TC		-	50	-	-	40	-	ppm/^{o}C
Supply Voltage (V++ -V-)	V_{SUPPLY}		±10	-	±16	±10	-	±16	V
Supply Current Total	I_{SUPPLY}		-	-	14	-	8	14	mA

ICL8052 Electrical Specifications $V_{SUPPLY} = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	ICL8052			ICL8052A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER									
Input Offset Voltage	V_{OS}	$V_{CM} = 0V$	-	20	75	-	20	75	mV
Input Current (Either Input) (Note 7)	I_{IN}	$V_{CM} = 0V$	-	5	50	-	2	10	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10V$	70	90	-	70	90	-	dB
Non-Linear Component of Common-Mode Rejection Ratio (Note 8)		$V_{CM} = \pm2V$	-	110	-	-	110	-	dB
Large Signal Voltage Gain	A_V	$R_L = 50k\Omega$	20,000	-	-	20,000	-	-	V/V
Slew Rate	SR		-	6	-	-	6	-	V/µs
Unity Gain Bandwidth	GBW		-	1	-	-	1	-	MHz
Output Short-Circuit Current	I_{SC}		-	20	-	-	20	-	mA

ICL8052 Electrical Specifications $V_{SUPPLY} = \pm 15V$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	ICL8052			ICL8052A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
COMPARATOR AMPLIFIER									
Small-Signal Voltage Gain	A_{VOL}	$R_L = 30k\Omega$	-	4000	-	-	-	-	V/V
Positive Output Voltage Swing	$+V_O$		12	13	-	12	13	-	V
Negative Output Voltage Swing	$-V_O$		-2.0	-2.6	-	-2.0	-2.6	-	V
VOLTAGE REFERENCE									
Output Voltage	V_O		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance	R_O		-	5	-	-	5	-	Ω
Temperature Coefficient	TC		-	50	-	-	40	-	ppm/^{o}C
Supply Voltage (V++ -V-)	V_{SUPPLY}		± 10	-	± 16	± 10	-	± 16	V
Supply Current Total	I_{SUPPLY}		-	6	12	-	6	14	mA

NOTES:

7. The input bias currents are junction leakage currents which approximately double for every 10^{o}C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + R_{\theta JA}P_D$, where $R_{\theta JA}$ is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.
8. This is the only component that causes error in dual-slope converter.

System Electrical Specifications: ICL8068/ICL71C03

V++ = +15V, V+ = +5V, V- = -15V, $T_A = 25^oC$, f_{CLK} Set for 3 Readings/Sec.

PARAMETER	TEST CONDITIONS	ICL8068A/ICL71C03 (NOTE 9)			ICL8068A/ICL71C03 (NOTE 10)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	$V_{IN} = 0V$, Full Scale = 200mV	-000.0	± 000.0	+000.0	-000.0	± 000.0	000.0	Digital Reading
Ratiometric Error (Note 11)	$V_{IN} = V_{REF}$ Full Scale = 2V	0.999	1.000	1.001	0.9999	1.0000	1.0001	Digital Reading
Linearity Over $\pm$ Full Scale (Error of Reading from Best Straight Line)	$-2V \le V_{IN} \le +2V$	-	0.2	1	-	0.5	1	Counts
Differential Linearity (Difference between Worst Case Step of Adjacent Counts and Ideal Step)	$-2V \le V_{IN} \le +2V$	-	0.01	-	-	0.01	-	Counts
Rollover Error (Difference in Reading for Equal Positive & Negative Voltage Near Full Scale)	$-V_{IN} \cong +V_{IN} \approx 2V$	-	0.2	1	-	0.5	1	Counts
Noise (P-P Value Not Exceeded 95% of Time)	$V_{IN} = 0V$, Full Scale = 200mV	-	3	-	-	2	-	μV
Leakage Current at Input	$V_{IN} = 0V$	-	200	300	-	100	200	pA
Zero Reading Drift (Note 12)	$V_{IN} = 0V$, $0^oC \le T_A \le 50^oC$	-	1	5	-	0.5	2	$\mu V/^oC$
Scale Factor Temperature Coefficient (Note 12)	$V_{IN} = 2V$, $0^oC \le T_A \le 50^oC$ Ext. Ref. 0ppm/^{o}C	-	3	15	-	2	5	ppm/^{o}C

System Electrical Specifications: ICL8052/ICL71C03

V++ = +15V, V+ = +5V, V- = -15V, T_A = 25°C, f_{CLK} Set for 3 Reading/Sec.

PARAMETER	TEST CONDITIONS	ICL8068A/ICL71C03 (NOTE 9)			ICL8068A/ICL71C03 (NOTE 10)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{IN} = 0V, Full Scale = 2V	-0.000	±0.000	+0.000	-0.000	±0.000	0.000	Digital Reading
Ratiometric Error (Note 11)	$V_{IN} = V_{REF}$ Full Scale = 2V	0.999	1.000	1.001	0.9999	1.0000	1.0001	Digital Reading
Linearity Over ± Full Scale (Error of Reading from Best Straight Line)	$-2V \le V_{IN} \le +2V$	-	0.2	1	-	0.5	1	Counts
Differential Linearity (Difference between Worst Case Step of Adjacent Counts and Ideal Step)	$-2V \le V_{IN} \le +2V$	-	0.01	-	-	0.01	-	Counts
Rollover Error (Difference in Reading for Equal Positive & Negative Voltage Near Full Scale)	$-V_{IN} \cong +V_{IN} \approx 2V$	-	0.2	1	-	0.5	1	Counts
Noise (Peak-To-Peak Value Not Exceeded 95% of Time)	V_{IN} = 0V, Full Scale = 200mV, Full Scale = 2V	-	20 50	- -	- -	 30	- -	µV
Leakage Current at Input	V_{IN} = 0V	-	5	30	-	3	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C To 70°C	-	1	5	-	0.5	2	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 2V, 0°C To 70°C, Ext. Ref. 0ppm/°C	-	3	15	-	2	5	ppm/°C

NOTES:

9. Tested in $3\frac{1}{2}$ digit (2,000 count) circuit shown in Figure 5, clock frequency 12kHz. Pin 2 71C03 connected to GND.
10. Tested in $4\frac{1}{2}$ digit (20,000 count) circuit shown in Figure 5, clock frequency 120kHz. Pin 2 71C03A open.
11. Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.
12. The temperature range can be extended to 70°C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068.

Detailed Description

ANALOG SECTION

Figure 2 shows the equivalent Circuit of the Analog Section of both the ICL71C03/8052 and the ICL71C03/8068 in the 3 different phases of operation. IF the RUN/$\overline{\text{HOLD}}$ pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 40,0002 at $4\frac{1}{2}$ digit and 4002 at $3\frac{1}{2}$ digit clock periods per cycle (see Figure 3 for details of conversion timing).

Auto-zero Phase I (Figure 2A)

During the Auto-Zero, the input of the buffer is connected to V_{REF} through switch 2, and switch 3 closes a loop around the integrator and comparator, the purpose of which is to charge the auto-zero capacitor until the integrator output does not change with time. Also, switches 1 and 2 recharge the reference capacitor to V_{REF}.

Input Integrate Phase II (Figure 2B)

During Input Integrate the auto-zero loop is opened and the ANALOG INPUT is connected to the BUFFER INPUT through switch 4 and C_{REF}. If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus, the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, and unbalanced condition exists compared to the Auto Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

Deintegrate Phase II (Figures 2C and 2D)

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switch 6 or 5. If the input signal is positive, switch 6 is closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the BUFFER INPUT. Negative Inputs will cause $+2(V_{REF})$ to be applied to the BUFFER INPUT via switch 5. Thus, the reference capacitor generates the equivalent of a (+) or (-) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input Integrate Phase, the input voltage required to give a full scale reading is $2V_{REF}$.

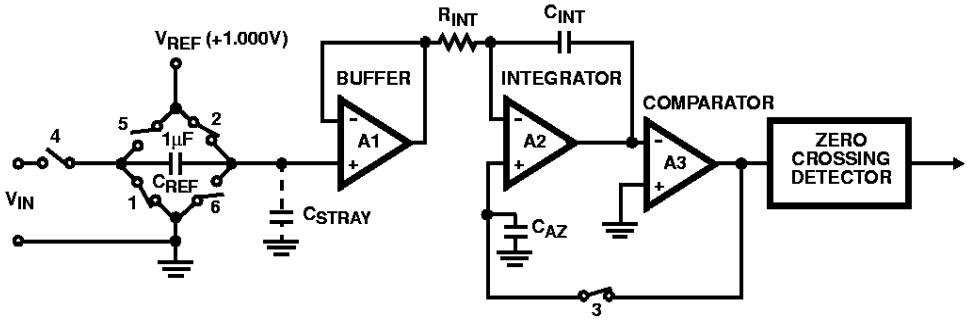


FIGURE 2A. PHASE I AUTO-ZERO

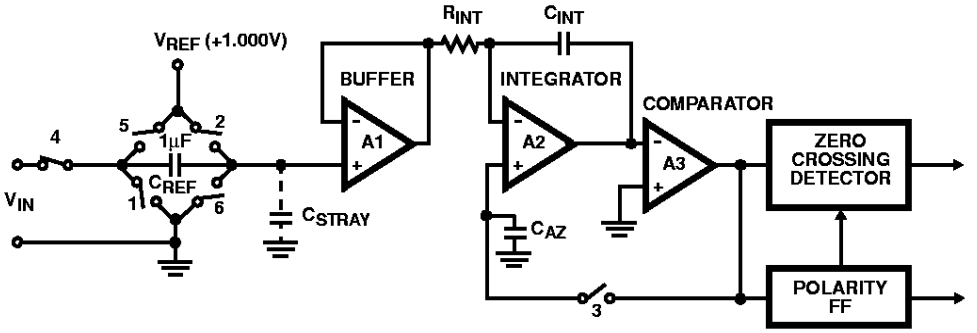


FIGURE 2B. PHASE II INTEGRATE INPUT

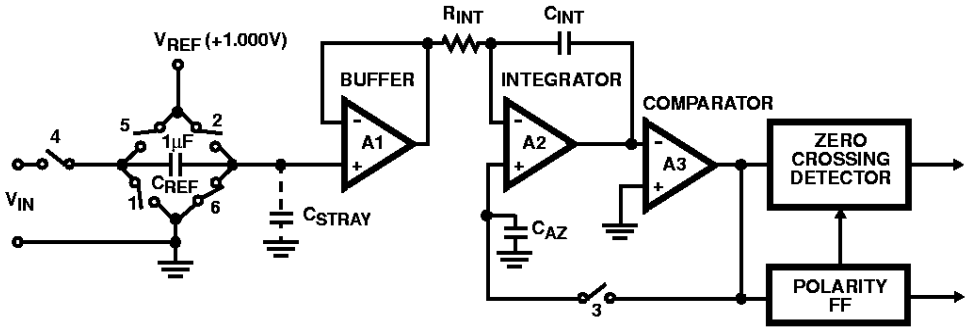


FIGURE 2C. PHASE III + DEINTEGRATE

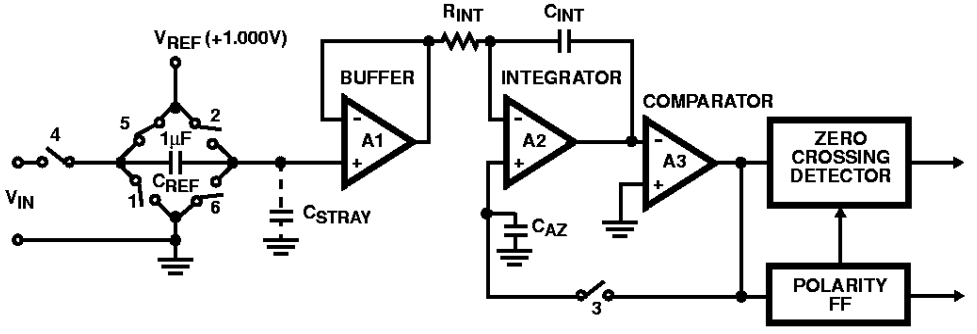


FIGURE 2D. PHASE III - DEINTEGRATE

FIGURE 2. ANALOG SECTION OF EITHER ICL8052 OR ICL8068 WITH ICL71C03

COUNTS			
	PHASE I	PHASE II	PHASE III
$4^1/_2$ DIGIT	10,001	10,000	20,001
$3^1/_2$ DIGIT	1,001	1,000	2,001

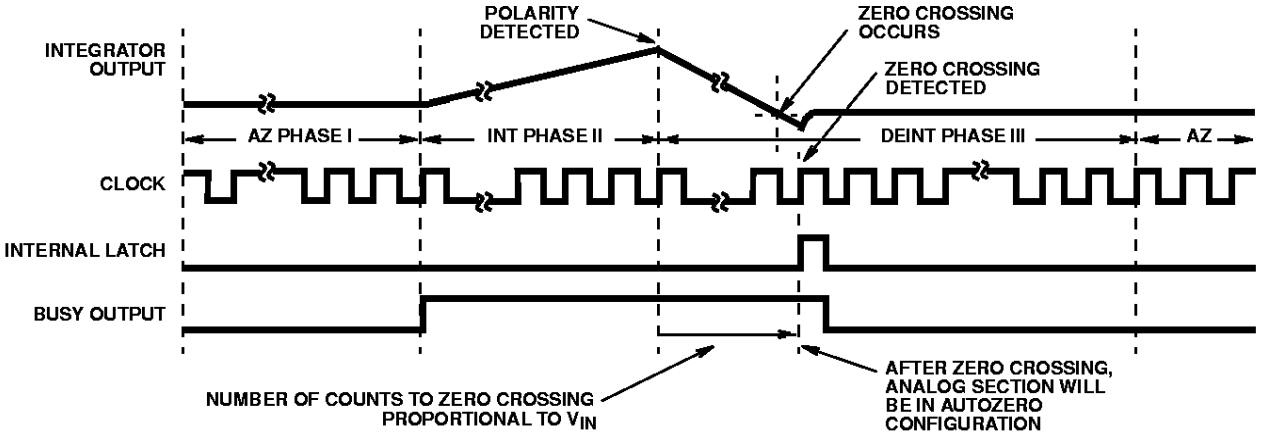


FIGURE 3. CONVERSION TIMING

Zero-Crossing Flip-Flop

Figure 4 shows the problem that the zero-crossing F/F is designated to solve.

The integrator output is approaching the zero-crossing point where the count will be latched and the reading displayed. For a 20,000 count instrument, the ramp is changing approximately 0.50mV per clock pulse (10V Max integrator output divided by 20,000 counts). The clock pulse feedthrough superimposed upon this ramp would have to be less than 100mV peak to avoid causing significant errors.

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one count delay compensates for the delay of the zero crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

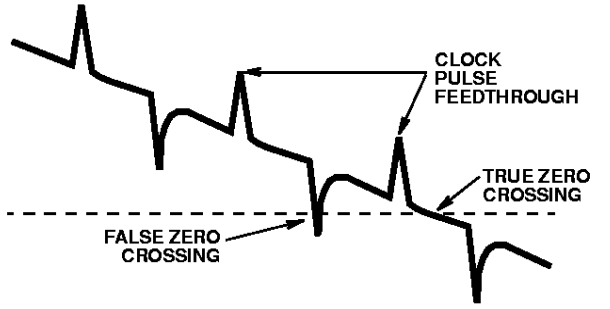


FIGURE 4. INTEGRATOR OUTPUT NEAR ZERO-CROSSING

Detailed Description

DIGITAL SECTION

The 71C03 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

4-1/2 / $\overline{\text{3-1/2}}$ (Pin 2)

When high (or open) the internal counter operates as a full $4^1/_2$ decade counter, with a complete measurement cycle requiring 40,002 counts. When held low, the least significant decade is cleared and the clock is fed directly into the next decade. A measurement cycle now requires only 4,0002 clock pulses. All 5 digit drivers are active in either case, with each digit lasting 200 counts with Pin 2 high ($4^1/_2$ digit) and 20 counts for Pin 2 low ($3^1/_2$ digit).

RUN/$\overline{\text{HOLD}}$ (Pin 4)

When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,0002/4,002 clock pulses. If taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as Pin 4 is held low. A short positive pulse (greater then 300ns) will now initiate a new measurement cycle beginning with up to 10,001/1,001 counts of auto zero. Of course if the pulse occurs before the full measurement cycle (40,002/4,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that full measurement cycle has been completed is that the first $\overline{\text{STROBE}}$ pulse (see below) will occur 101/11 counts after the end of this cycle. Thus, if RUN/$\overline{\text{HOLD}}$ is low and has been low for at least 101/11 counts, converter is holding and ready to start a new measurement when pulsed high.

$\overline{\text{STROBE}}$ (Pin 18)

This is a negative-going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative-going $\overline{\text{STROBE}}$ pulses that occur