

Functional Block Diagram

PIN DESCRIPTION

DATA

- X₁₅₋₀** X Operand Input
- Y₁₅₋₀** Y Operand Input
- TMS₁₅₋₀** MSP of 32-Bit T Output
- TLS₁₅₋₀** LSP of 32-Bit T Output

CONTROL

- XEN** Enable X-Input Latch
- YEN** Enable Y-Input Latch
- WEN** Enable W Latch
- XM** X-Input Data Format
- YM** Y-Input Data Format
- FA** Format Adjust
- LD** Load Concatenated X and Y Operands
- RND** Round MSP
- TME** Enable TMS Output (Active LO)
- TLE** Enable TLS Output (Active LO)
- TSEL** Select MSP or LSP to TMS Port

STATUS

- ZERO** Zero
- OVFL** Overflow
- NEG** Negative

CLOCKS

- CK1** Input Latches Clock
- CK2** Output Latches Clock

POWER

- V_{CC1}** Positive Supply Voltage to Internal Logic
- V_{CC2}** Positive Supply Voltage to Output Circuits
- GND1** Negative Supply Voltage to Internal Logic
- GND2** Negative Supply Voltage to Output Circuits

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

METHOD OF OPERATION

The X-Input Latch holds its most recent contents unless $\overline{\text{CLK1}}$ is LO (logic 0) when enabled (made transparent) by $\overline{\text{XEN}}$ also LO. Similarly, the Y-Input Latch holds its most recent contents unless $\overline{\text{CLK1}}$ is LO when enabled by $\overline{\text{YEN}}$ also LO. The state of the $\overline{\text{CK1}}$ input clock has no effect on each input latch unless the input enable lines $\overline{\text{XEN}}$ and $\overline{\text{YEN}}$ are LO, respectively. When these enable lines are LO, the respective latches will pass data when the $\overline{\text{CK1}}$ input is LO and hold data when the $\overline{\text{CK1}}$ input is HI (logic 1).

The X and Y input data can be either in twos-complement, unsigned-magnitude, or mixed-mode formats (Table I). Twos-complement input data is indicated by HI levels on the XM line for X input data and HI levels on the YM line for Y input data. Unsigned-magnitude X and Y inputs are indicated by LO levels on the XM and YM lines, respectively. Outputs will be in the same format as inputs unless the input formats are mixed, in which case the outputs will be in twos-complement representation. XM and YM are latched into the X-Input and Y-Input Latches with the input operand data.

The Instruction Latch holds its most recent contents unless $\overline{\text{CLK1}}$ is LO when enabled by either $\overline{\text{XEN}}$ or $\overline{\text{YEN}}$ also LO. When $\overline{\text{CK1}}$ is HI, the contents of the Instruction Latch will be held. If both $\overline{\text{XEN}}$ and $\overline{\text{YEN}}$ are HI, the contents of the Instruction Latch will also be held. Round (RND), format adjust (FA), and load (LD) are the three instruction bits that pass through or are held at the Instruction Latch.

The ADSP-7018's W output is fielded into a 16-bit most significant product (MSP) and a 16-bit least significant product (LSP). When the RND is HI, the MSP of the W result will be rounded by adding a binary 1 (with carry) to the most significant bit (MSB) of the LSP, consistently rounding toward positive infinity at mid-scale. Truncating the MSP (RND LO) introduces a large-sample statistical bias of $-(2^{16}-1)/2$ LSBs of the LSP, while rounding (RND HI) reduces the bias to $+1/2$ LSBs of the LSP.

The FA control format adjusts the Z output from the multiplier array. When FA is HI, the full 32-bit Z result is passed unmodified to the W latch (Tables II and III). All possible products can be represented without overflow, including twos-complement fractional $(-1.0) \times (-1.0)$. The binary point in the MSP of a twos-complement fractional product will not align with the binary point in the input operands. Thus, the numeric weighting of data within a system using this format (with FA HI) will not be uniform. Also, the two highest-order bits in a twos-complement product are normally redundant. An additional bit of precision in the MSP could be obtained by eliminating one of these redundant bits.

Format adjust (FA LO) shifts the Z result left by one bit position and right-fills a binary zero (Table III). Thus, format adjust eliminates redundant high-order bits in twos-complement products. The MSPs of fractional twos-complement products also receive proper weighting relative to input data. However, an overflow on format adjust will occur when full-scale negative is multiplied by itself, yielding full-scale negative instead of the correct positive product (which is not representable in format-adjusted twos-complement format). This special condition is monitored by the OVFL flag so that it does not go undetected.

The Load (LD) instruction determines whether the multiplier array is active or put into a pass-through mode. When LD is LO, the multiplier array is active and produces the product of the X and Y input values as Z result. When LD is HI, the multiplier array is put in the pass-through mode and the X and Y input values are concatenated to form a Z result with the X input in the most significant position (Table II). XM determines the sign mode of the complete 32-bit Z result. ZERO, OVFL and NEG are set depending on the value of this Z result. RND and FA can also be used in this mode. Load allows any 32-bit number loaded through the input ports to be rounded, tested for zero and sign, and to have fractional binary points aligned while testing for overflow. It is also valuable for system testing by providing a direct path through the multiplier and greater access to latches within the ADSP-7018.

Output flags ZERO, OVFL, and NEG are generated from the intermediate Z result. When not rounding (RND LO), ZERO is set when the full 32-bit result is zero. When rounding (RND HI), ZERO is set when the format-adjusted MSP in the W result will be zero. That is, when rounding, ZERO is set for Z_{31-16} equals zero when FA HI but ZERO is set for Z_{31-15} equals zero when FA LO. Zero will not be set if an overflow condition exists.

OVFL is set only for twos-complement multiplications of full-scale negative times full-scale negative when format adjusting (FA LO).

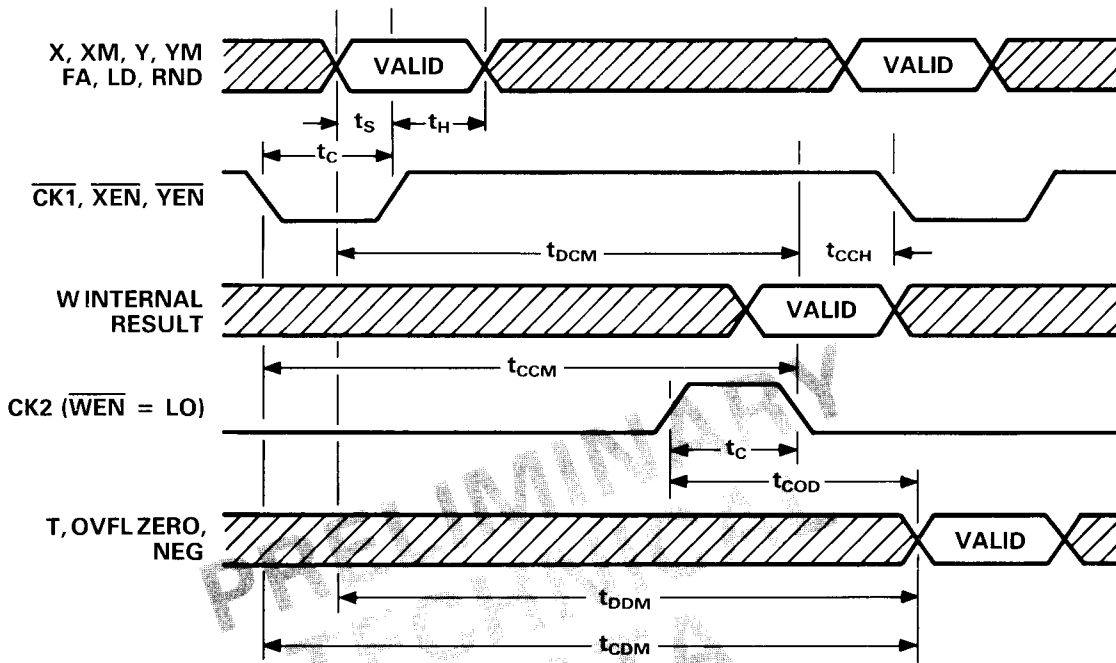
NEG is set only when a twos-complement or mixed-mode Z result is negative. A loaded, previously overflowed result (MSB of 1 followed by all zeros) will set NEG as well as OVFL, if loaded with XM HI.

The output latches for data and flags ZERO, OVFL and NEG hold their most recent contents unless CLK2 is HI when enabled by $\overline{\text{WEN}}$ LO. With $\overline{\text{WEN}}$ LO, the output latches are transparent when CK2 is HI and data is held when CK2 is LO. The ADSP-7018 can be made a totally asynchronous device by holding all enables active ($\overline{\text{XEN}}$, $\overline{\text{YEN}}$, and $\overline{\text{WEN}}$ all LO) and $\overline{\text{CLK1}}$ LO and CLK2 HI. Note that the clock definitions are complementary; if CLK1 and CLK2 are tied together and enable lines asserted, input latches will be transparent when output latches are latched and vice versa. $\overline{\text{CLK1}}$ and CLK2 are fully independent, allowing double-clock operation. For triple-clock operation, the two clock lines can be held active which causes the three latch enable controls to behave like independent clock lines.

The T output is fielded into two 16-bit portions, TMS and TLS, each with its own three-state controls. A HI on the asynchronous $\overline{\text{TME}}$ or $\overline{\text{TLE}}$ lines disables the corresponding TMS or TLS output driver to a high-impedance state. Conversely, a LO on $\overline{\text{TME}}$ or $\overline{\text{TLE}}$ enables the corresponding output driver, driving the output bus.

TSEL controls the multiplexer feeding the TMS field (Table IV). When TSEL is LO, the MSP from the W Latch will be passed to the TMS output. When TSEL is HI, the LSP will be routed to TMS. This multiplexer and its associated TSEL control simplifies operation of the ADSP-7018 in 16-bit bus systems.

**TTL 16 × 16-BIT FIXED-POINT MULTIPLIER
CLOCKED AND UNCLOCKED TIMING**



NOTE: FOR FLOWTHROUGH OPERATION, THE LATCHES MUST BE MADE TRANSPARENT.

OUTPUT ENABLE

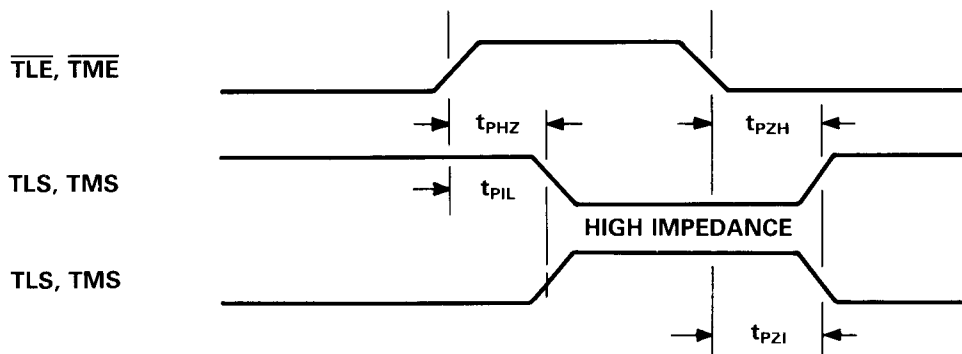


Figure 1. ADSP-7018 Timing Diagram

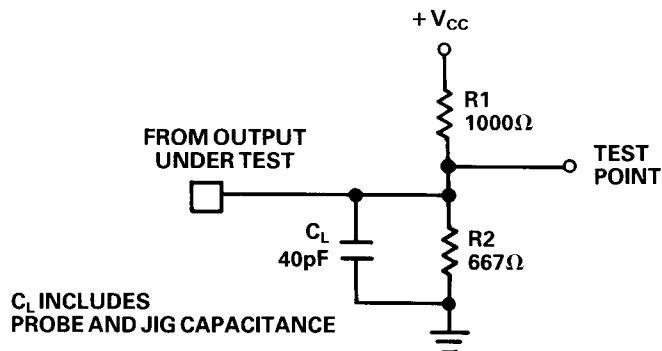


Figure 2. ADSP-7018 Load Test Circuit

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

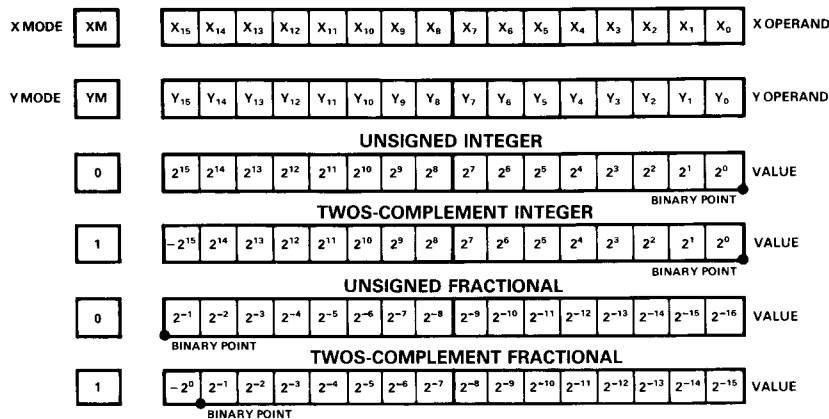


Table I. ADSP-7018 Input Data Formats

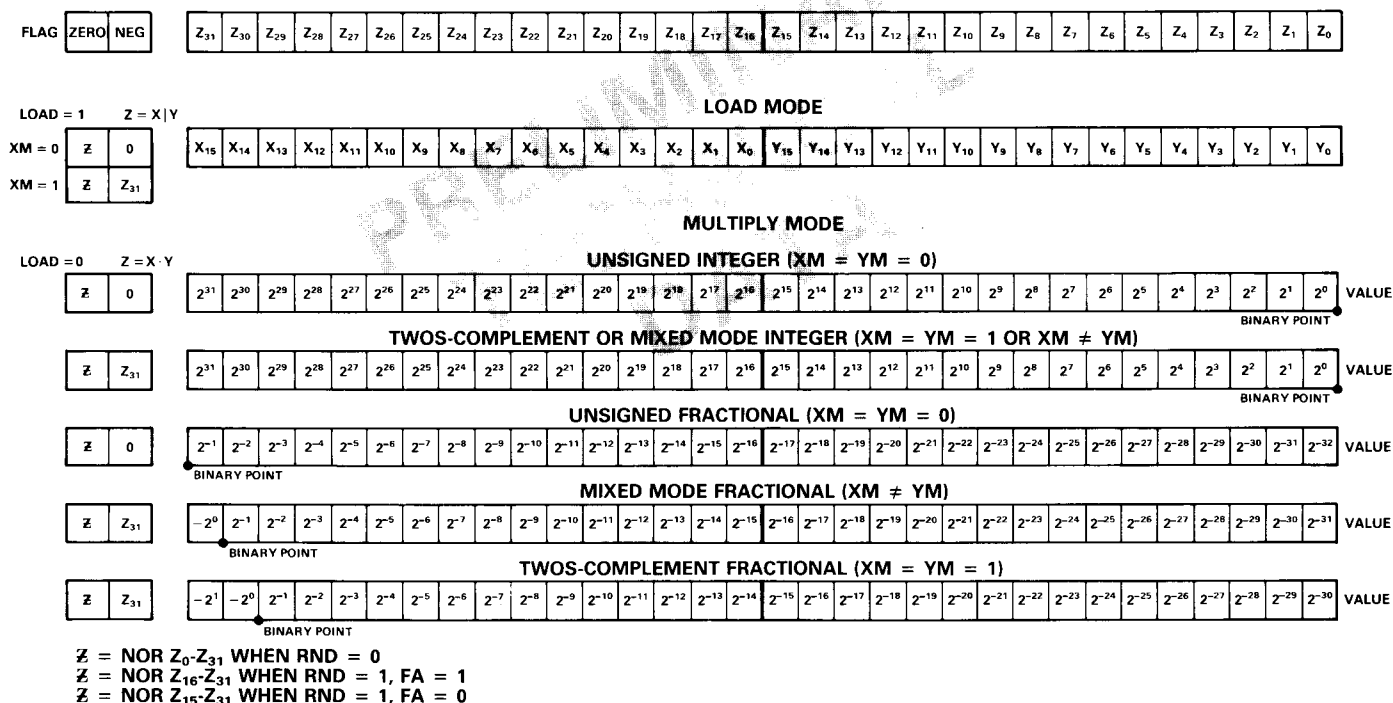
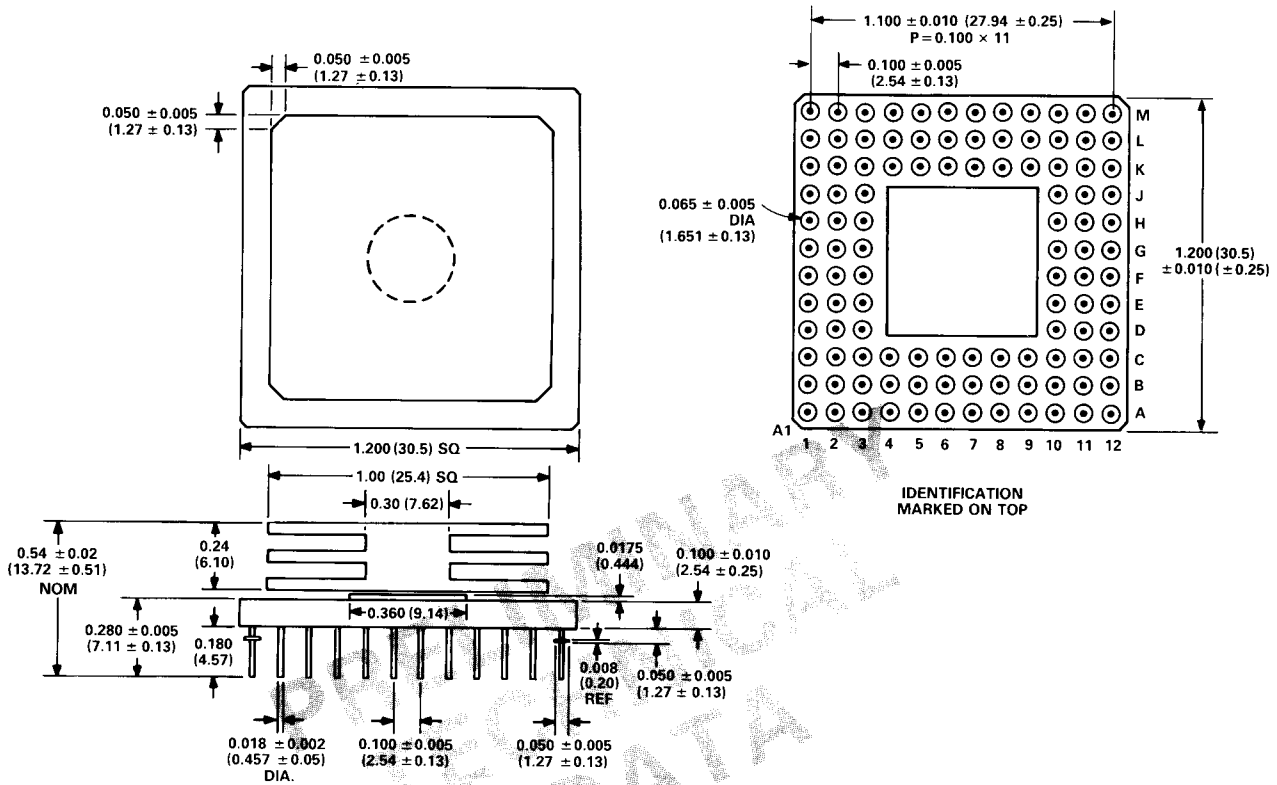


Table II. ADSP-7018 Z Result Formats, ZERO and NEG Flags, and Load Operation

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ADSP-7018 PIN CONFIGURATION

GND2	V _{CC2}	V _{CC1}	V _{CC2}	TMS5	TMS7	GND2	V _{CC1}	V _{CC2}	V _{CC1}	OVFL	V _{CC2}	M
V _{CC1}	TLS14	TMS0	TMS2	TMS3	V _{CC1}	TMS9	TMS10	TMS13	TMS14	NEG	GND2	L
GND1	TLS13	TLS15	TMS1	TMS4	TMS6	TMS8	TMS11	TMS12	TMS15	ZERO	Y15	K
V _{CC1}	TLS11	TLS12	BOTTOM VIEW						YM	Y14	Y13	J
V _{CC2}	TLS9	TLS10							Y12	Y11	Y10	H
GND2	TLS8	V _{CC1}							Y9	GND1	V _{CC1}	G
V _{CC1}	TLS7	TLS6							Y6	Y7	Y8	F
V _{CC2}	TLS5	TLS4	Y3	Y4	Y5	E						
GND1	TLS3	TLS2	Y0	Y1	Y2	D						
V _{CC1}	TLS1	GND2	TSEL	\overline{XEN}	ROUND	X2	X6	X9	X12	GND1	V _{CC1}	C
TLS0	V _{CC1}	\overline{TLE}	CK2	\overline{YEN}	LOAD	X3	X5	X8	X11	X14	XM	B
V _{CC2}	\overline{TME}	\overline{WEN}	$\overline{CK1}$	FA	X0	X1	X4	X7	X10	X13	X15	A
1	2	3	4	5	6	7	8	9	10	11	12	

- NOTES
 1. ALL V_{CC1} PINS MUST BE TIED TO ALL V_{CC2} PINS.
 2. ALL GND1 PINS MUST BE TIED TO ALL GND2 PINS.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

FEATURES

16 × 16-bit Parallel Multiplication
15ns Max Multiplication Time
ECL 10KH Compatible
4.125W Max Power Dissipation
**Independent Input and Output Latches which
Can Be Made Transparent**
**Unclocked, Single-, Double-, and Triple-Clock
Operation**
**Twos Complement, Unsigned Magnitude, and
Mixed Mode**
Format Adjust and Rounding
Parallel Data Load and Passthrough from Input Port
Full 32-Bit Product Output Port
Sign, Overflow, and Zero Status Flags
Pin-Compatible with B3018
1.20" Square 108-Pin Grid Array

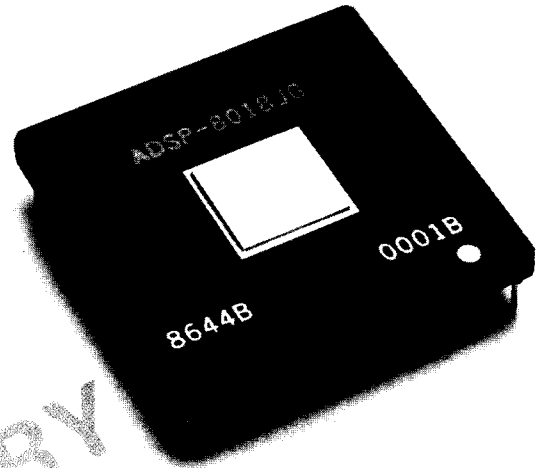
APPLICATIONS

Digital Signal Processing
Array Processors
Super-Minicomputers
General-Purpose Computing

GENERAL DESCRIPTION

The ADSP-8018 is a high-speed 16 × 16-bit parallel ECL multiplier. The ADSP-8018 has two 16-bit input ports and a fielded 32-bit output port. These 32-bit products are available in parallel, as independently enabled 16-bit Least Significant Product (LSP) and 16-bit Most Significant Product (MSP) portions, or LSP and MSP multiplexed to a single 16-bit port. Each 16-bit field of the product latch has its own output enable control.

Inputs can be represented in either twos-complement, unsigned-magnitude, or mixed-mode formats. The input, instruction, status, and output latches are all latches which can be enabled to be transparent. Input operands and output results are stored in individually enabled latches with separate clocks for input and output. For unclocked flow-through operation, the latches can be made transparent by holding clocks and enables active. Tying clocks together as a single clock causes input and output latches to operate in complementary fashion, simplifying synchronous operation. The two clocks are fully independent, allowing double clock operation. With both clock lines held active, the three enable controls can function as three independent clock lines for the two data input ports and the output port, respectively.



The ADSP-8018 produces a 32-bit product that may be format-adjusted for consistent signed fractional output format and for maximum precision in a 16-bit MSP. The MSP of the format-adjusted 32-bit product can be rounded with a control which causes a 1 to be added to the Most Significant Bit (MSB) of the LSP. Three status flags indicate the presence of a zero, negative, or overflowed result. The input operands can be loaded and passed directly through without multiplication, but with format adjustment, rounding, and setting of status flags.

The ADSP-8018 is a pin-for-pin replacement for Bipolar Integrated Technology's B3018 ECL 16 × 16 Multiplier.

The ADSP-8018 is available for commercial temperature ranges in a compact, hermetically-sealed 108-pin grid array.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS¹

ABSOLUTE MAXIMUM RATINGS

Parameter	ADSP-8018		Unit
	Min	Max	
V _{EE} Supply Voltage (V _{CC} = 0)	-8.0	0	V
V _{IN} Input Voltage (V _{CC} = 0)	V _{EE}	0	V
I _O Output Source Current Continuous		30	mA
		100	mA
T _{ST} Storage Temperature (Ambient)	-55	+150	°C
T _J Operating Junction Temperature		+165	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	ADSP-8018			Unit
	Min	Nom	Max	
V _{EE} Supply Voltage (V _{CC} = 0)	-5.46	-5.20	-4.94	V
T _{AMB} Operating Temperature (Ambient) ³	0		+70	°C
R _L Output Termination to -2.0V dc		50		Ω

ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	ADSP-8018						Unit
		0°C		25°C		70°C		
		Min	Max	Min	Max	Min	Max	
V _{IH} High-Level Input Voltage	@V _{EE} = max	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V
V _{IL} Low-Level Input Voltage	@V _{EE} = min	-1.95	-1.55	-1.95	-1.50	-1.95	-1.50	V
V _{OH} High-Level Output Voltage (Terminated)	@V _{EE} = max	-1.02	-0.84	-0.99	-0.81	-0.93	-0.735	V
V _{OL} Low-Level Output Voltage (Terminated)	@V _{EE} = max	-1.95	-1.60	-1.95	-1.56	-1.95	-1.56	V

Parameter	Test Conditions	Min	Nom	Max	Unit
		I _{IH} High-Level Input Current, All Inputs	@ V _{EE} = min & V _{IN} = -800mV		
I _{IL} Low-Level Input Current, All Inputs	@V _{EE} = min & V _{IN} = -1.8V			300	μA
I _{EE} Supply Current	@V _{EE} = min; ECL inputs			825	mA
C _I Input Capacitance			5		pF

SWITCHING CHARACTERISTICS²

Parameter	ADSP-8018J		Unit
	Min	Max	
t _S Input Setup Time	0.8		ns
t _H Input Hold Time	3.0		ns
t _C Clock and Latch Enable Pulse Duration	3.5		ns
t _{DCM} Data to Clock Multiply Time		12	ns
t _{CCH} Clock to Clock Hold Time	-1.5		ns
t _{CCM} Clock to Clock Multiply Time		15	ns
t _{COD} Clocked Output Delay		5.5	ns
t _{DDM} Data to Data Multiply Time		15.5	ns
t _{CDM} Clock to Data Multiply Time		18	ns
t _{DAO} Output Disable Delay		5.5	ns
t _{ENO} Output Enable Delay		5.5	ns

NOTES

¹All min and max specifications are over power-supply and temperature range indicated.

²Input levels are -1.8V and -800mV. Rise times are 2ns typical. Input and output timing reference levels are -1.3V.

³500 linear feet per minute ambient air flow. See also Figure 3.

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.