12 x 2.7 Gbps Parallel Optical Transmitter/Receiver

PL-TCP-02-S53-11 Transmitter

PL-RCP-02-S53-11 Receiver

Key Features

- **Delivers bandwidth to key system bottlenecks**
- **Reduces inventory costs**
- **Enables field replacement**
- **Improves manufacturing yield**
- **Minimizes impact on system power budget**
- **Eases system design**
- **Enables multiple data channel fanout**
- **Multisource availability strengthens supply chain**

Applications

- Optical backplane extension
- System interconnect
  - Cross connect switching
  - Network edge devices
  - Access network equipment
  - Mass storage systems
- Massively parallel OC-48, InfiniBand or Gigabit Ethernet extension
- High end CPU interconnect
- Rack-to-rack/Board-to-board interconnect

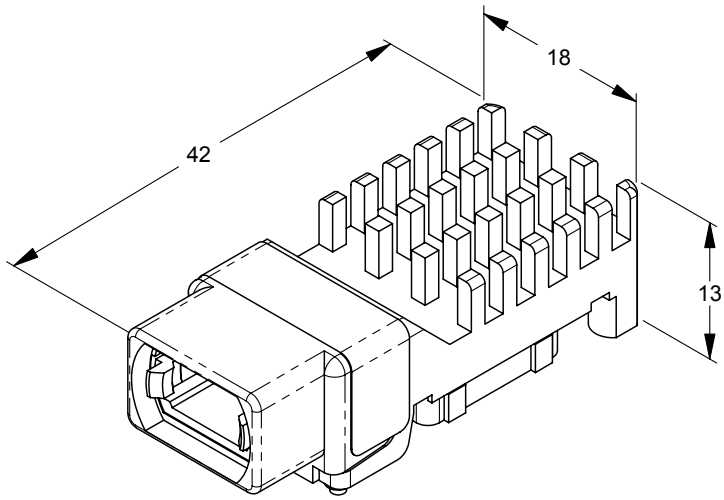
The JDSU parallel optical interconnect is a transmitter/receiver pair operating with 12 channels at 2.7 Gbps for an aggregate bandwidth of 32.4 Gbps. The parallel modules are another in JDSU's family of products for optical backplane applications, where high-speed, high-density components are needed to handle increased bandwidth demand. The parallel optical interconnect is compatible with the SNAP12 multisource agreement, and features JDSU's highly reliable 850 nm, oxide vertical-cavity surface-emitting laser (VCSEL) array with a standard FCI Meg-Array® connector interface. The module's pluggable, connectorized design enables manufacturers to provision bandwidth on demand, upgrading cards in the field with the snap-on optics.

Highlights

- Expands bandwidth across equipment backplanes, meeting ultra-high capacity demand for faster central office switching
- FCI Meg-Array connector attachment enables "snap-on" optics that improve customers' manufacturing yields, reduce inventory costs, and provide capability for system field upgrade to add bandwidth
- Thumb-sized modules typically consume only 2.2 watts of power per pair, lowering system power costs and increasing density
- System backplanes become "distance-independent," seamlessly connecting equipment from 0 to 600 meters over OM3 fiber, 0 to 300 meters over OM2 fiber
- 2.7 Gbps data rates per channel, allowing customers to select the optimum model for their applications
- SNAP12 multisource agreement compatibility ensures reliable supply chain

PL-xCP-02-S53-11 Features

- Utilizes a JDSU high reliability, high speed, 850 nm, oxide VCSEL array
- Data rate to 2.7 Gbps per channel for a total link data rate of 32.4 Gbps
- Mass production compatible FCI Meg-Array connector interface
- Low power consumption (approx. 2 watts per module pair)
- 12 asynchronous independent electrical/optical data channels
- Bit Error Rate < $1x10^{-12}$ without FEC
- Supports 50/125 µm and 62.5/125 µm multimode fiber
- Industry standard MTP optical interface
- IEC 60825-1 Amendment 2 (2001-01) Class 1M laser eye safe
- 0°C to 80°C operating range
- Single +3.3 V power supply
- Supplied with process plug



DIMENSIONS MM - MAXIMUM

The 12-channel PL-xCP-02-S53-11 parallel optical interconnect combines the convenience of low-cost, snap-on connector pluggability with the speed of parallel optics. It sets the standard for ease of design, manufacture, test and field support of ultrahigh-speed optics required across equipment backplane in core switches, routers and multiplexors.

Section 1 Functional Description

The PL-xCP-02-S53-11 850 nm VCSEL Gigabit Transmitter/Receiver is designed to transmit and receive DC balanced data, such as 2.488G OC-48, or 8B/10B encoded data, over 50/125 µm or 62.5/125 µm optical fiber.

Note: All references to SNAP12 MSA specifications refer to version 1.1 of that document.

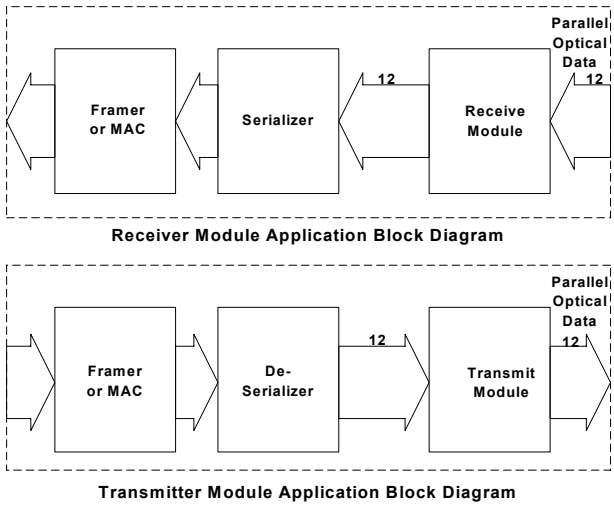


Figure 1 Recommended application for the PL-xCP-02-S53-11 transmitter/receiver

Transmitter

The transmitter converts 12 channels of encoded DC balanced CML electrical data into serial optical data. Transmit data lines (DIN 01: DIN 12) are terminated with 100 Ω differential. See Figure 7 on page 6, and Figures 8 and 9 on page 7 for application schematic information. Unused channels should have inputs tied together.

TXEN/TXDIS

LVCMOS logic level Transmit Enable (TXEN) and Transmit Disable (TXDIS) are provided. A logic "1" or no connection on the TXEN pin and a logic "0" or no connection on the TXDIS pin allow normal operation. Both signals must be connected as described for normal operation. A logic "0" on the TXEN pin or a logic "1" on the TXDIS pin will disable all transmit channels.

-Reset/-Fault

An LVCMOS logic level fault output (-Fault) is provided. A logic "1" on this pin indicates proper operation. A logic "0" on this pin indicates a fault has occurred in the laser circuitry and the faulty laser outputs are disabled.

An LVCMOS logic level reset input (-Reset) is provided. A logic "1" on this pin allows normal operation. A logic "0" on this pin will reset the laser circuitry and disable all laser outputs. During power-up, -Reset must remain logic "0" until the power supply (Vcc) has reached a minimum of 3V.

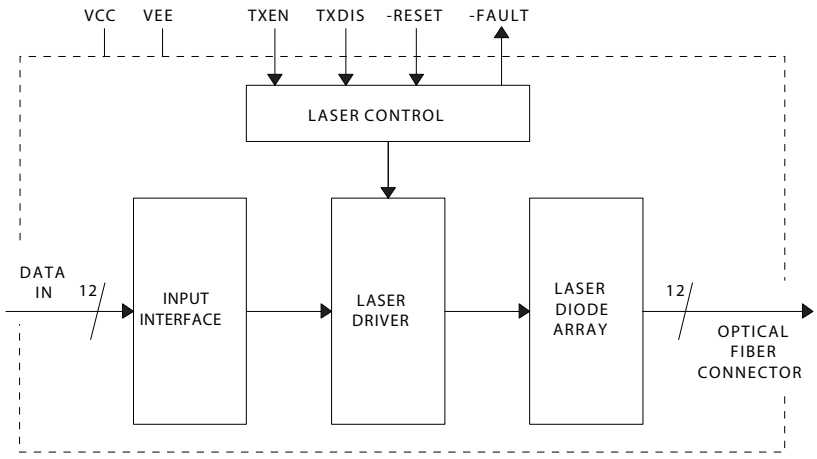


Figure 2 Transmit module block diagram

Receiver

The receiver converts encoded serial optical data into DC balanced parallel CML electrical data. Receive data lines (DOUT1:DOUT12) should be terminated into single-ended 50 Ω loads or equivalent.

SD/SD1/-SD12

LVCMOS Signal Detect Status Outputs (SD, SD1 and -SD12) are provided. SD, SD1 and -SD12 are independent signal detect status indicators for all channels, channel 1, and channel 12 respectively. A logic "1" on SD indicates that sufficient optical signal has been detected on all channels (see Section 3.5 Electrical characteristics; "Signal Detect Assert/Negate Level on page 17). A logic "0" on SD indicates that insufficient optical signal for proper operation has been detected on at least one of the 12 channels. A logic "1" on SD1 and a logic "0" on -SD12 indicate that sufficient optical signal has been detected on channels 1 and 12. A logic "0" on SD1 and/or a logic "1" on -SD12 indicates that insufficient optical signal has been detected at channel 1 and/or 12 for proper operation.

RXEN

An LVCMOS Receive Output Enable Input (RXEN) is provided. A logic "1" on RXEN will enable proper operation of the high speed data outputs. A logic "0" on RXEN powers down the outputs which leaves them fixed at Vpp.

SQEN

An LVCMOS Squelch Enable Input (SQEN) is provided. A logic "1" on SQEN will turn sqelch on. A logic "0" on SQEN turns squelch off.

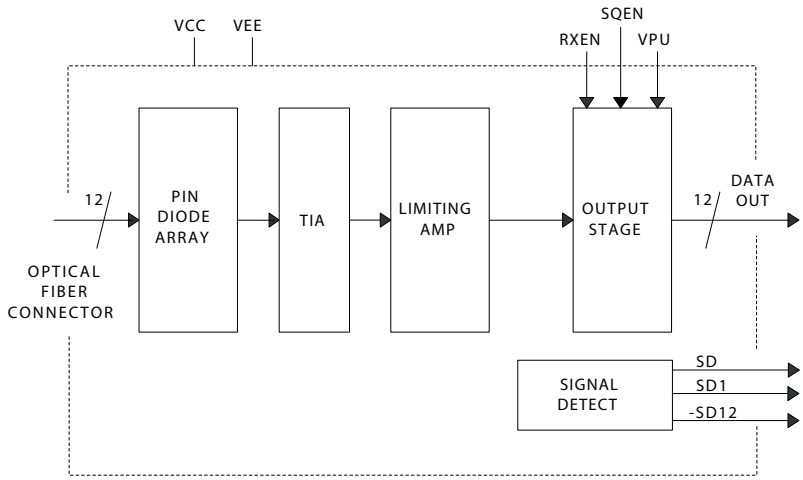


Figure 3 Receive module block diagram

VPU

VPU is defined in the SNAP 12 MSA as the power supply for the receiver output stage. For part number PL-RCP-02-S53-11 this must be connected to a power supply in the range 2.5V to 3.3V. Use of 2.5V will reduce power dissipation. For part number PL-RCP-02-S53-8A the output stage is internally connected to 3.3V and VPU pins can be left open circuit.

Power supply and grounding

Power supply filtering is recommended for both the transmitter and receiver. Filtering should be placed on the host assembly as close to the Vcc pins as possible for optimal performance. Recommended filtering shown in Figure 4.

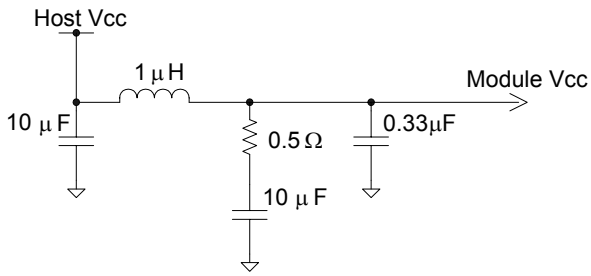


Figure 4 Recommended filtering

Module signal and power grounds are common. The module case is not connected internally to power ground. To ensure that the entire case is grounded, it is necessary to ground both the front and rear screws.

Section 2 Application Schematics

Recommended connections to the PL-xCP-02-S53-11 transmitter/receiver are shown in Figure 5, 6, 7, 8, and 9.

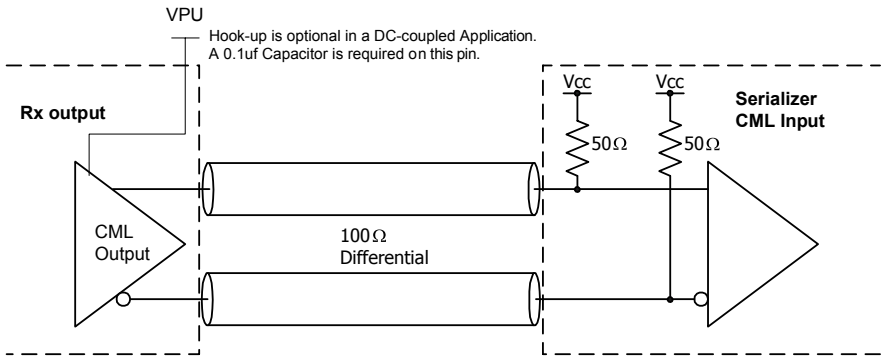


Figure 5 Rx module; high speed output; CML interface

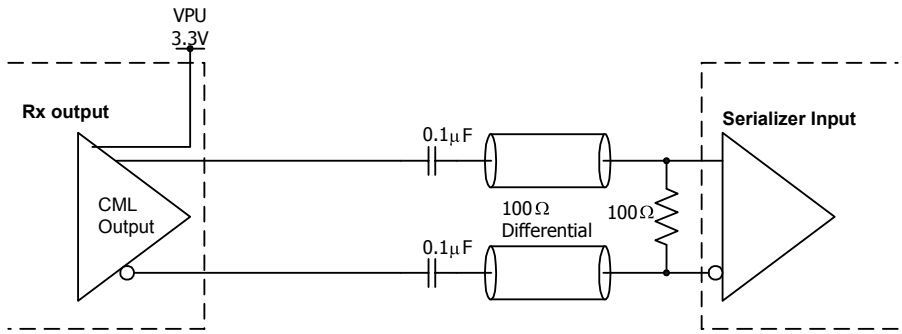


Figure 6 Rx module; high speed output; AC coupled interface

Note: Connect VPU to an external CML pull-up voltage (SNAP12 MSA VPU connect to 3.3 V) using the power supply filtering circuit shown in Figure 4. However, it is optional for part number PL-RCP-020S53-8A.

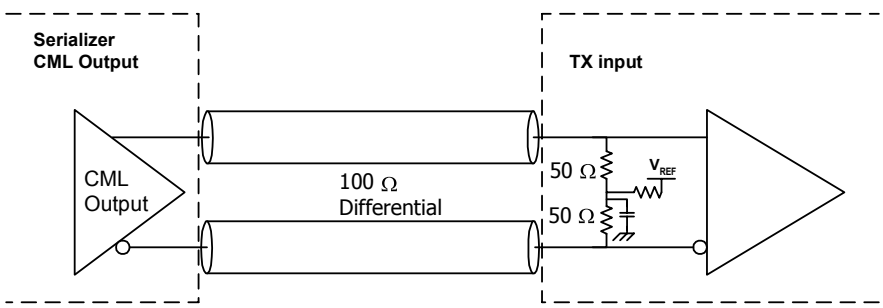


Figure 7 Tx module; high speed input; CML interface

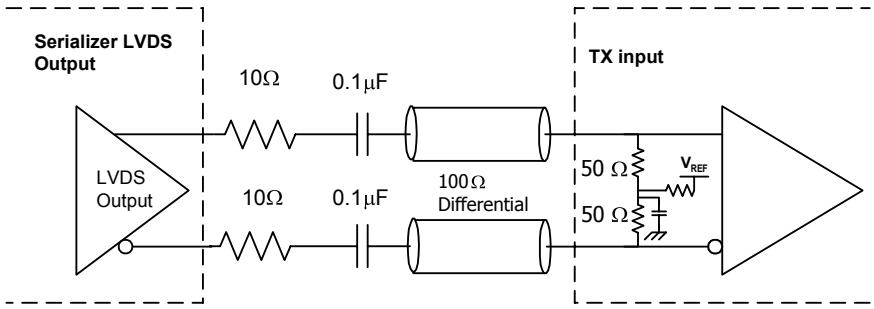


Figure 8 Tx module; high speed input; LVDS or similar interface

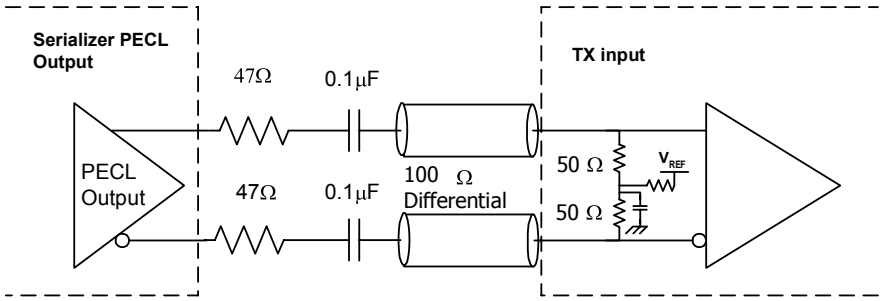


Figure 9 Tx module; high speed input; PECL or similar interface

Notes:
Power supply filtering components should be placed on the opposite side of the PCB directly under the PL-xCP-02-S53-11 transmitter/receiver, as close to the Vcc pins as possible for optimal performance.

PECL, LVDS, or other outputs may require biasing networks, not shown. Consult Application Information for those devices.

Transmission lines should be 100 ohm differential traces. It is recommended that the termination resistor be placed beyond the Rx IC pins.

For unused channels, receiver output pairs should be terminated to Vpp or AC terminated to ground. Unused transmitter inputs should be tied together, or DC biased to the zero state (preferred).

If using dc coupling, users must ensure data remains dc balanced, or maintain a steady zero level at the TX input, otherwise rated optical output power may be exceeded.

Series resistors can be used to improve electrical crosstalk on a system board and to improve impedance match at the source.

Section 3 Technical Data

Technical data related to the 12 x 2.7 Gbps Parallel Optical Transmitter/Receiver includes:

3.1 Receiver pin descriptions

Pin Number	Symbol	Type	Description
A2	GND		Ground
A3	GND		Groung
A5	GND		Ground
A6	GND		Ground
B1	GND		Ground
B2	Dout9n	CML Out	Data Output, inverted
B3	Dout9p	CML Out	Data Output, non-inverted
B4	GND		Ground
B5	Dout10p	CML Out	Data Output, non-inverted
B6	Dout10n	CML Out	Data Output, inverted
B7	GND		Ground
B8	GND		Ground
B9	GND		Ground
C1	GND		Ground
C2	GND		Ground
C3	Dout8n	CML Out	Data Output, inverted
C4	Dout8p	CML Out	Data Output, non-inverted
C5	GND		Ground
C6	Dout11p	CML Out	Data Output, non-inverted
C7	Dout11n	CML Out	Data Output, inverted
C8	GND		Ground
C9	GND		Ground
D1	GND		Ground
D2	GND		Ground
D3	GND		Ground
D4	Dout7n	CML Out	Data Output, inverted
D5	Dout7p	CML Out	Data Output, non-inverted
D6	GND		Ground
D7	Dout12p	CML Out	Data Output, non-inverted
D8	Dout12n	CML Out	Data Output, inverted
D9	GND		Ground
E1	GND		Ground
E2	Dout6n	CML Out	Data Output, inverted

3.1 Receiver pin descriptions

Continued

Pin Number	Symbol	Type	Description
E3	Dout6p	CML Out	Data Output, non-inverted
E4	GND		Ground
E5	Dout3n	CML Out	Data Output, inverted
E6	Dout3p	CML Out	Data Output, non-inverted
E7	GND		Ground
E8	GND		Ground
E9	GND		Ground
F1	GND		Ground
F2	GND		Ground
F3	Dout5n	CML Out	Data Output, inverted
F4	Dout5p	CML Out	Data Output, non-inverted
F5	GND		Ground
F6	Dout2n	CML Out	Data Output, inverted
F7	Dout2p	CML Out	Data Output, non-inverted
F8	GND		Ground
F9	GND		Ground
G1	GND		Ground
G2	GND		Ground
G3	GND		Ground
G4	Dout4n	CML Out	Data Output, inverted
G5	Dout4p	CML Out	Data Output, non-inverted
G6	GND		Ground
G7	Dout1n	CML Out	Data Output, inverted
G8	Dout1p	CML Out	Data Output, non-inverted
G9	GND		Ground
H3	VCC		Power supply voltage
H4	VCC		Power supply voltage
H5	VCC		Power supply voltage
H6	VCC		Power supply voltage
H7	SD	LVCMOS Out	Signal Detect on all fibers High=signal of sufficient AC power is present on all fibers Low=signal on at least one fiber is insufficient
H8	SD1	LVCMOS Out	Signal Detect on fiber #1 High=signal of sufficient AC power is present on fiber #1 Low=signal on fiber #1 is insufficient
J3	VCC		Power supply voltage
J4	VCC		Power supply voltage
J5	VCC		Power supply voltage
J6	VCC		Power supply voltage
J8	-SD12	LVCMOS Out	Signal Detect on fiber #12 Low=signal of sufficient AC power is present on fiber #12 High=signal on fiber #12 is insufficient
J9	RXEN	LVCMOS In	High=normal output operation Low=all data outputs disabled Internal pull-up
K1[1]	VPU (SNAP12 MSA = VPP)		Power supply voltage to CML output pull-up resistors.
K2[1]	VPU (SNAP12 MSA = VPP)		Power supply voltage to CML output pull-up resistors.
K8	VPU (SNAP12 MSA = VPP)		Power supply voltage to CML output pull-up resistors.
K9	VPU (SNAP12 MSA = VPP)		Power supply voltage to CML output pull-up resistors.
K10	SQEN	LVCMOS In	Squelch enable. High= data outputs driven to logic “0” when SD is active (low) on that channel Low=squelch disabled Internal pull-up.

1. NIC for part number PL-RCP-02-S53-8A

3.1.1 RX module signals on user's board

Top view of user's board (this edge towards fiber ribbon)
Larger connector orientation feature/key

	K	J	H	G	F	E	D	C	B	A
1	VPU (SNAP12:VPP)	NIC	NIC	GND	GND	GND	GND	GND	GND	NIC
2	VPU (SNAP12:VPP)	NIC	NIC	GND	GND	DOUT6n	GND	GND	DOUT9n	GND
3	NIC	VCC	VCC	GND	DOUT5n	DOUT6p	GND	DOUT8n	DOUT9p	GND
4	NIC	VCC	VCC	DOUT4n	DOUT5p	GND	DOUT7n	DOUT8p	GND	NIC
5	NIC	VCC	VCC	DOUT4p	GND	DOUT3n	DOUT7p	GND	DOUT10p	GND
6	NIC	VCC	VCC	GND	DOUT2n	DOUT3p	GND	DOUT11p	DOUT10n	GND
7	NIC	NIC	SD	DOUT1n	DOUT2p	GND	DOUT12p	DOUT11n	GND	NIC
8	VPU (SNAP12:VPP)	-SD12	SD1	DOUT1p	GND	GND	DOUT12n	GND	GND	NIC
9	VPU (SNAP12:VPP)	RXEN	NIC (SNAP12 ENSD)	GND	GND	GND	GND	GND	GND	NIC
10	SQEN	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC
				Smaller connector orientation feature/key						

Notes:
DNC is do not connect (module vendor specific pin).
NIC is no internal connection.

3.1.2 Rx MTP connector (front view of module)

FRONT VIEW – MTP KEY IS UP

CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
User PCB below											

3.2 Transmitter pin descriptions

Pin Number	Symbol	Type	Description
A2	GND		Ground
A3	GND		Ground
A5	GND		Ground
A6	GND		Ground
B1	GND		Ground
B2	Din9p	Signal In	Data Input, non-inverted
B3	Din9n	Signal In	Data Input, inverted
B4	GND		Ground

3.2 Transmitter pin descriptions

Continued

Pin Number	Symbol	Type	Description
B5	Din10n	Signal In	Data Input, inverted
B6	Din10p	Signal In	Data Input, non-inverted
B7	GND		Ground
B8	GND		Ground
B9	GND		Ground
C1	GND		Ground
C2	GND		Ground
C3	Din8p	Signal In	Data Input, non-inverted
C4	Din8n	Signal In	Data Input, inverted
C5	GND		Ground
C6	Din11n	Signal In	Data Input, inverted
C7	Din11p	Signal In	Data Input, non-inverted
C8	GND		Ground
C9	GND		Ground
D1	GND		Ground
D2	GND		Ground
D3	GND		Ground
D4	Din7p	Signal In	Data Input, non-inverted
D5	Din7n	Signal In	Data Input, inverted
D6	GND		Ground
D7	Din12n	Signal In	Data Input, inverted
D8	Din12p	Signal In	Data Input, non-inverted
D9	GND		Ground
E1	GND		Ground
E2	Din6p	Signal In	Data Input, non-inverted
E3	Din6n	Signal In	Data Input, inverted
E4	GND		Ground
E5	Din3p	Signal In	Data Input, non-inverted
E6	Din3n	Signal In	Data Input, inverted
E7	GND		Ground
E8	GND		Ground
E9	GND		Ground
F1	GND		Ground
F2	GND		Ground
F3	Din5p	Signal In	Data Input, non-inverted
F4	Din5n	Signal In	Data Input, inverted
F5	GND		Ground
F6	Din2p	Signal In	Data Input, non-inverted
F7	Din2n	Signal In	Data Input, inverted
F8	GND		Ground
F9	GND		Ground
G1	GND		Ground
G2	GND		Ground
G3	GND		Ground
G4	Din4p	Signal In	Data Input, non-inverted
G5	Din4n	Signal In	Data Input, inverted
G6	GND		Ground
G7	Din1p	Signal In	Data Input, non-inverted
G8	Din1n	Signal In	Data Input, inverted
G9	GND		Ground

3.2 Transmitter pin descriptions

Continued

Pin Number	Symbol	Type	Description
H3	VCC		Power supply voltage of laser driver
H4	VCC		Power supply voltage of laser driver
H5	VCC		Power supply voltage of laser driver
H6	VCC		Power supply voltage of laser driver
H8	-FAULT	LVCMOS Out	Transmit laser fault. Low level indicates a fault.
H9	TXDIS		Transmit laser disable. Active high. Internal pull-down.
J3	VCC		Power supply voltage of laser driver
J4	VCC		Power supply voltage of laser driver
J5	VCC		Power supply voltage of laser driver
J6	VCC		Power supply voltage of laser driver
J8	-RESET	LVCMOS In	Reset fault condition. Active Low. Internal pull-up.
J9	TXEN	LVCMOS In	Transmit laser enable. Active high. Internal pull-up.

3.2.1 TX module signals on user's board

Top view of user's board (this edge towards fiber ribbon)
Larger connector orientation feature/key

	K	J	H	G	F	E	D	C	B	A
1	DNC	NIC	NIC	GND	GND	GND	GND	GND	GND	NIC
2	DNC	NIC	NIC	GND	GND	DIN6p	GND	GND	DIN9p	GND
3	NIC	VCC	VCC	GND	DIN5p	DIN6n	GND	DIN8p	DIN9n	GND
4	NIC	VCC	VCC	DIN4p	DIN5n	GND	DIN7p	DIN8n	GND	NIC
5	NIC	VCC	VCC	DIN4n	GND	DIN3p	DIN7n	GND	DIN10n	GND
6	NIC	VCC	VCC	GND	DIN2p	DIN3n	GND	DIN11n	DIN10p	GND
7	NIC	NIC	NIC	DIN1p	DIN2n	GND	DIN12n	DIN11p	GND	NIC
8	DNC	-RESET	-FAULT	DIN1n	GND	GND	DIN12p	GND	GND	NIC
9	DNC	TXEN	TXDIS	GND	GND	GND	GND	GND	GND	NIC
10	NIC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC

Smaller connector orientation feature/key

Notes:
DNC is do not connect (module vendor specific pin).
NIC is no internal connection.

3.2.2 Tx MTP connector (front view of module)

FRONT VIEW – MTP KEY IS UP

CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

User PCB below

3.3 Signaling timing diagrams

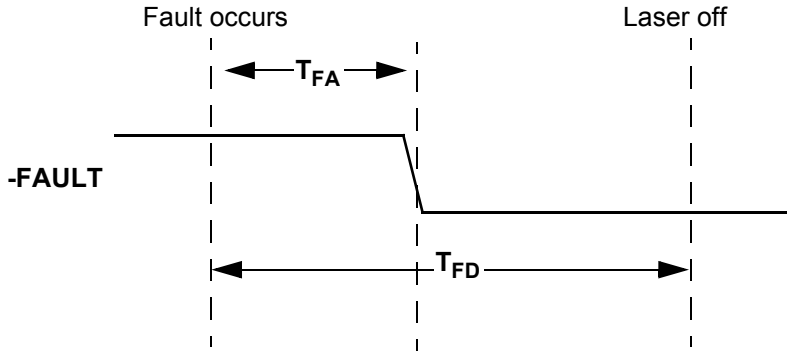


Figure 10 Transmit fault

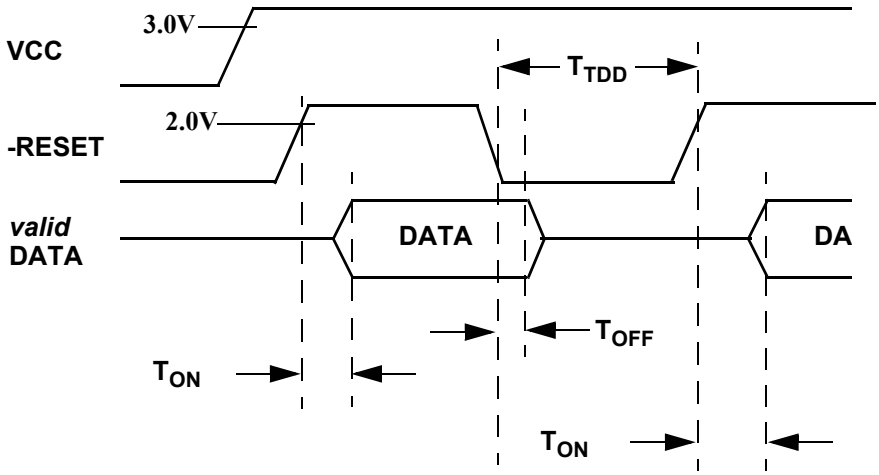


Figure 11 Transmit startup and reset

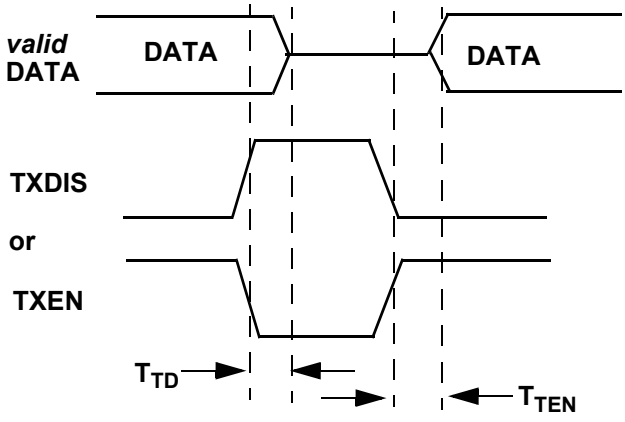


Figure 12 Transmit enable/disable

3.3 Signaling timing diagrams

Continued

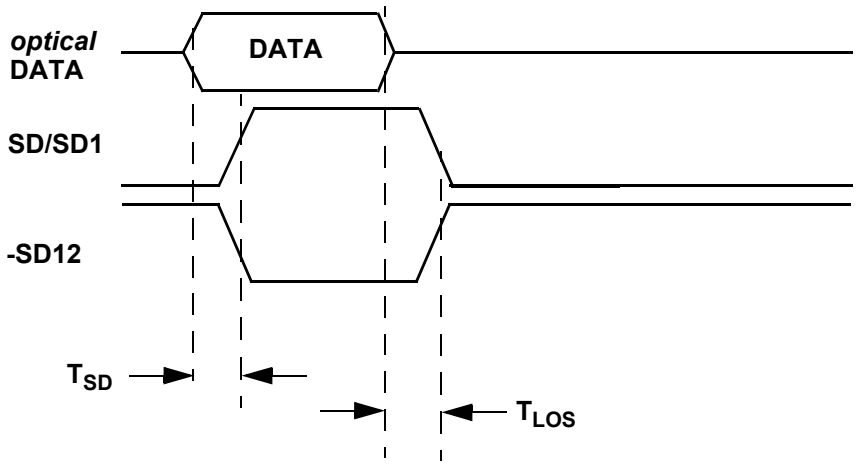


Figure 13 Receive data signal detect

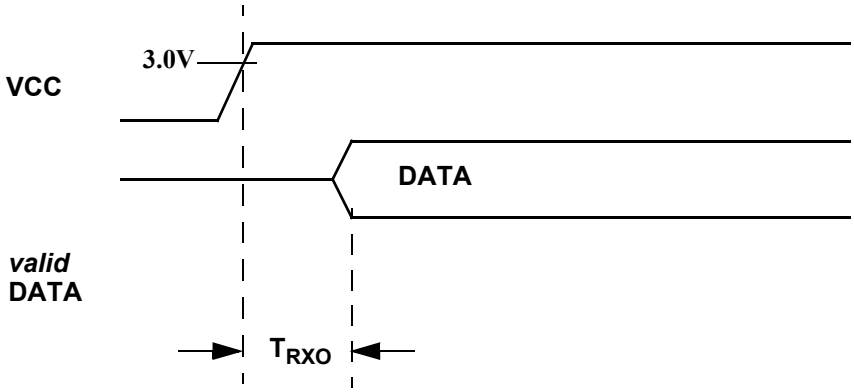


Figure 14 Receive startup timing

3.4 Absolute maximum ratings

(These values represent the damage threshold level of the devices.)

Parameter	Symbol	Ratings	Unit	Note
Storage temperature	T_{st}	-40 to +100	°C	
Transmitter operating case temperature	T_{CTX}	0 to +80	°C	1
Receiver operating case temperature	T_{CRX}	0 to +80	°C	1
Power supply voltage	V_{cc}	-0.3 to +4.5	V	
Transmitter differential input voltage	V_D	1.4	V	
Input voltage range	V_{IR}	-0.3 to Vcc + 0.3	V	
Electrostatic discharge	ESD	±1000	V	
Relative humidity	RH	5% to 95% non-condensing		

Note:
1. Typical ambient temperature with no air flow is 65°C to result in 80°C case temperature.

3.5 Electrical characteristics

(T_{CTX} = 0°C to 80°C, T_{CRX} = 0°C to 80°C, Vcc = 3.15V to 3.45V)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	Vcc	3.15	3.3	3.45	V	
Data rate	D_{TR}	0.5		2.72	Gbps	
Power supply noise$_1$	N_{P1}			10	mV_{p-p}	@ 1KHz to 1MHz
Power supply noise$_2$	N_{P2}			100	mV_{p-p}	@ 1MHz to 2GHz
Transmitter						
Supply current	I_{CCT}		290	500	mA	
Power consumption	P_I		1.2	1.75	W	
Data input voltage swing	V_{TDp-p}	200		900	mV_{p-p}	
Data input range	V_{INR}	1500		Vcc	mV	
Data input rise/fall time	t_{INR}/t_{INF}	100		200	ps	20% - 80%, differential
Data input skew	t_{INS}	0		30	ps	Single Channel, Data/$\overline{\text{Data}}$
Transmit control signal voltage level (LVCMOS)	V_{IH} V_{IL}	2 0		Vcc 0.8	V V	
Transmit disable enable assert time	T_{TEN} T_{TD}			1 100	ms µs	See Figure 12, "Transmit enable/ disable," on page 13
Transmit reset time	T_{TDD} T_{ON}	10			µs ms	See Figure 11, "Transmit startup and reset," on page 13
Transmit fault time	T_{FA} T_{FD}			100 100	µs µs	See Figure 10, "Transmit fault," on page 13 SNAP12 MSA = 100 ms max for T_{FA} and T_{FD}
Receiver						
Supply current	I_{CCR}		300	450	mA	
Power consumption	P_R		1.0	1.5	W	
Instantaneous data output voltage	V_{DOR}	Vpp -1.1		Vpp +0.1	V	
Data output voltage swing	V_{DOS}	470		800	mV_{p-p}	R_{LOAD} = 100 Ω, differential
Data output rise/fall time			100	150	ps	20% - 80%, differential
Data output skew				30	ps	R_{LOAD} = 100 Ω, Intra Channel, differential
Data output impedance	R_{OL}		100		Ohm	Differential
Data output deterministic jitter	Dj			0.14	UI	±K28.5 pattern (note 1)
Data output total jitter	Tj			0.39	UI	2^{23}-1 pattern, BER < $1x10^{-12}$ (note 1)
Signal detect voltage level	V_{OH} V_{OL}	2.4 0		Vcc 0.4	V V	I_O < 1mA (note 2)
Signal detect assert time	T_{SD} T_{SD1}, T_{-SD12}			50 50	µs µs	See Figure 13, "Receive data signal detect," on page 14
Signal detect de-assert time	T_{LOS}			50	µs	
Receive reset time	T_{RXO}			500	ms	See Figure 14, "Receive startup timing," on page 14

Notes:
1. UI (Unit Interval): one UI is equal to one bit time. For example, 2.5 Gbits/s corresponds to a UI of 400 ps.
2. For SD_A and SD_N definitions, see Signal Detect Assert/Negate Level in Section 3.6 Optical characteristics on page 16.

3.6 Optical characteristics

(T_{CTX} = 0°C to 80°C, T_{CRX} = 0°C to 80°C, Vcc = 3.15V to 3.45V)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Wavelength	λ_p	830	850	860	nm	
RMS spectral width	$\Delta\lambda$		0.5	0.65	nm	SNAP12 MSA = 0.85 nm max
Average optical power	P_{AVG}	-8.0		-2.0	dBm	
Average optical power, disabled				-30	dBm	
Optical output rise/fall time	$t_{rise/fall}$			160	ps	20% - 80%, unfiltered
Optical modulation amplitude	OMA	190			µW	Equivalent to 6dB ER at P_{AVG} = -8dBm
Deterministic jitter	Dj			0.14	UI	±K28.5 pattern (note 1)
Total jitter	Tj			0.33	UI	2^{23}-1 pattern, BER<1x10^{-12} (note 1)
Channel to channel skew	T_{C-C}			200	ps	
Relative intensity noise	RIN		-130	-117	dB/Hz	1GHz, 12 dB reflection
Receiver						
Wavelength	λ	830	850	860	nm	
Optical input power	Po			-2.0	dBm	
Sensitivity	S			-16	dBm	note 2
Stressed sensitivity	S_S			-12	dBm	note 3
Signal detect assert/negate level	SD_A			-17	dBm	note 4
	SD_N	-30			dBm	
Low frequency cutoff	F_C	25		160	kHz	-3 dB, P<-16 dBm
Optical return loss		12			dB	

Notes:
1. UI (Unit Interval): one UI is equal to one bit time. For example, 2.5 Gbits/s corresponds to a UI of 400 ps.
2. Sensitivity and saturation parameters using a Pseudo Random Bit Sequence (PRBS) 2^{23} - 1, an extinction ration (ER) greater than 6 dB and a maximum bit error ratio (BER) of 10^{-12}. For sensitivity measurements, the maximum BER shall be maintained in the presence of the maximum crosstalk penalty. The maximum crosstalk possibility is defined as the 'victim' receiver channel operating at its sensitivity limit and remaining eleven the 'aggressor' receiver channels being actively driven at 6 dB higher incident power and 2.7 Gbps data rate. The minimum average optical power and minimum extinction ratio is equivalent to 30 mW Optical Modulation Amplitude (OMA).
3. Measured with stressed eye pattern at 2.7G Data rate with 2dB eye closure per the SNAP-12 MSA.
4. Signal Detect assertion requires all optical inputs to exhibit a minimum 6 dB Extinction Ratio at SD_A = –17 dBm. All channels not under test are operating with PRBS 23 serial encoded patterns, asynchronous with the channel under test, and an average input power up to 6 dB higher than the input power sensitivity specification.

3.7 Link length

(T_{CTX} = 0°C to 80°C, T_{CRX} = 0°C to 80°C, Vcc = 3.15V to 3.45V)

Data Rate / Standard	Fiber Type	Modal Bandwidth @ 850 nm (MHz*km)	Distance Range (m)
2.7 Gbps	62.5/125 µm MMF	200	0 to 150
2.488Gbps / OC-48	50/125 µm MMF	500	0 to 325

3.8 Regulatory compliance

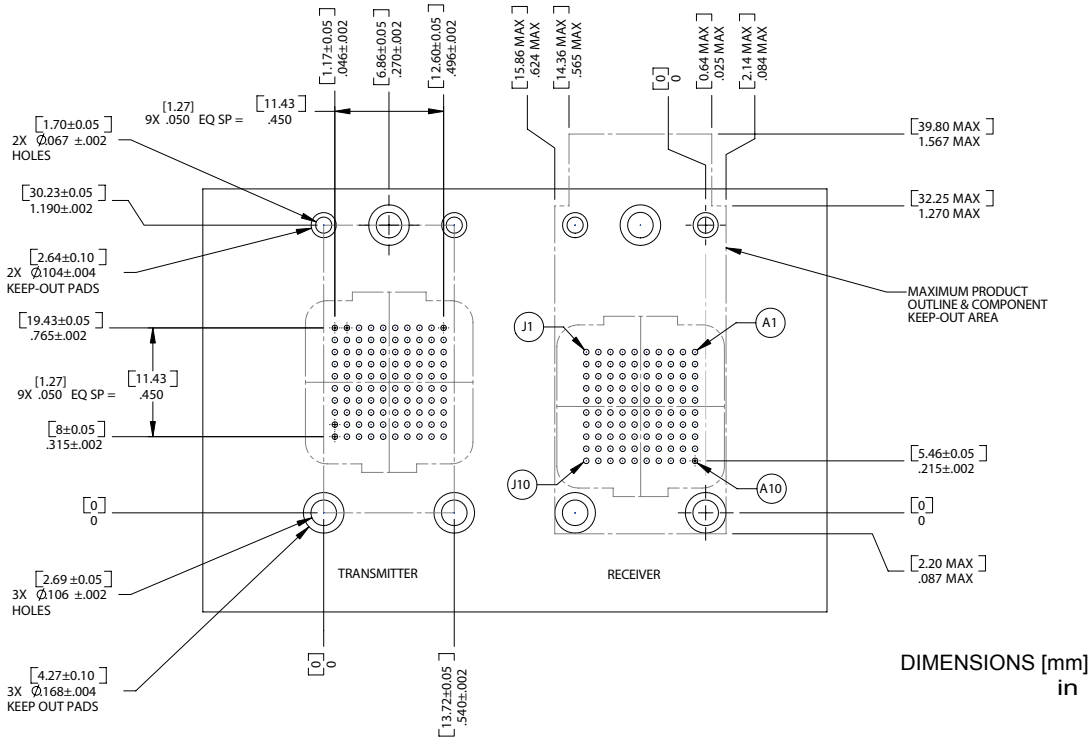
The PL-xCP-02-S53-11 complies with international Electromagnetic Compatibility (EMC) and international safety requirements and standards (see details in Table 1 below). EMC performance is dependent on the overall system design. Information included herein is intended as a figure of merit for designers to use as a basis for design decisions.

The PL-xCP-02-S53-11 has been engineered for product safety and regulatory agency compliance.

Table 1 Regulatory compliance

Feature	Test Method	Performance
RoHS 5/6 Compliant	Directive 2002/95/EC	Compliant per the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment except for lead in tin-lead solder and the manufacturing process.
Component Safety	UL 60950 UL94-V0 EN 60950	UL File E209897 TUV Report/Certificate (CB Scheme)
Laser Eye Safety	EN 60825 U. S. 21CFR 1040.10 and 1040.11	CDRH compliant and Class 1M laser eye safe TUV Certificate
Electromagnetic Compatibility		
CE	EU Declaration of Conformity	Compliant with European EMC and Safety Standards
Electromagnetic Emissions	EMC Directive 89/336/EEC FCC CFR47 Part 15 IEC/CISPR 22 AS/NZS CISPR22 EN 55022 ICES-003, Issue 4 VCCI-03	Noise frequency range: 30 MHz to 16 GHz. Good system EMI design practice required to achieve Class B margins.
Electromagnetic Immunity	EMC Directive 89/336/EEC IEC /CISPR/24 EN 55024	Class 1 (> 1 kV)
ESD Immunity	EN 61000-4-2	Exceeds Requirements. Withstands discharges of; 15kV contact, 25kV air
Radiated Immunity	EN 61000-4-3: 1998	Exceeds Requirements. Field strength of 10V/m RMS, from 10 MHz to 1 GHz. No effect on transmitter/receiver performance is detectable between these limits.

3.9 PCB layout



Note: Recommended PAD size for MEG-array Host Board connector is 0.64 mm (0.025 in)

Figure 15 Top view

3.10 Maximum dimensions

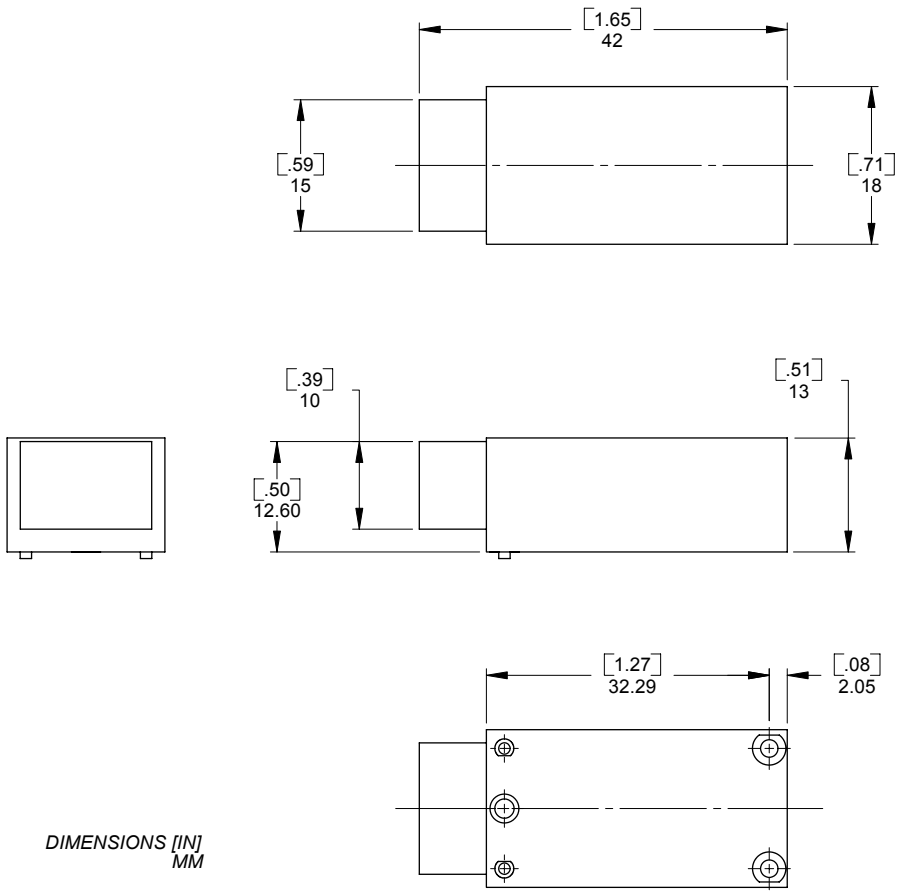


Figure 16 Maximum dimensions

3.11 Module outline

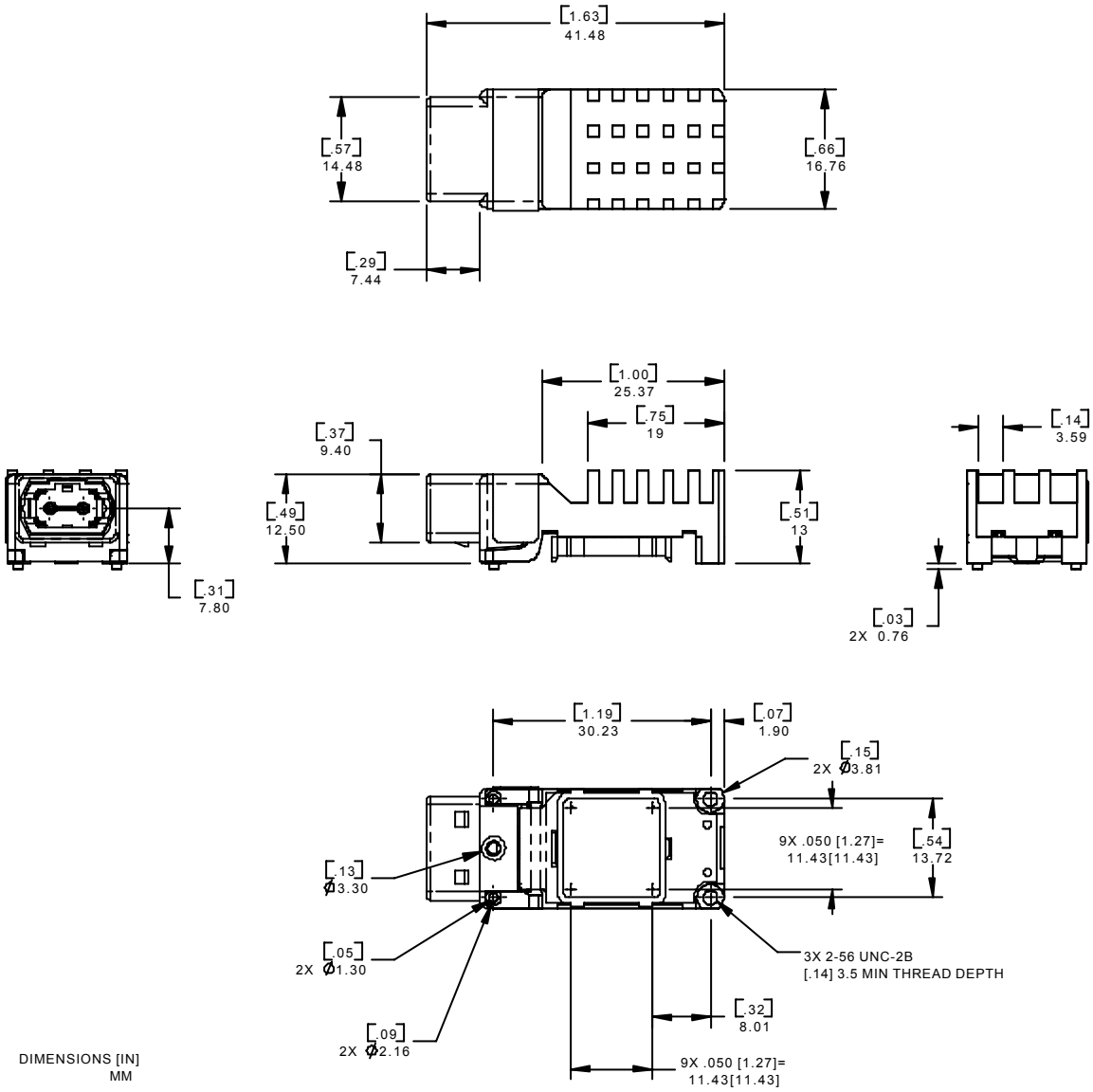


Figure 17 Transmitter Module

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3.11 Module outline

Continued

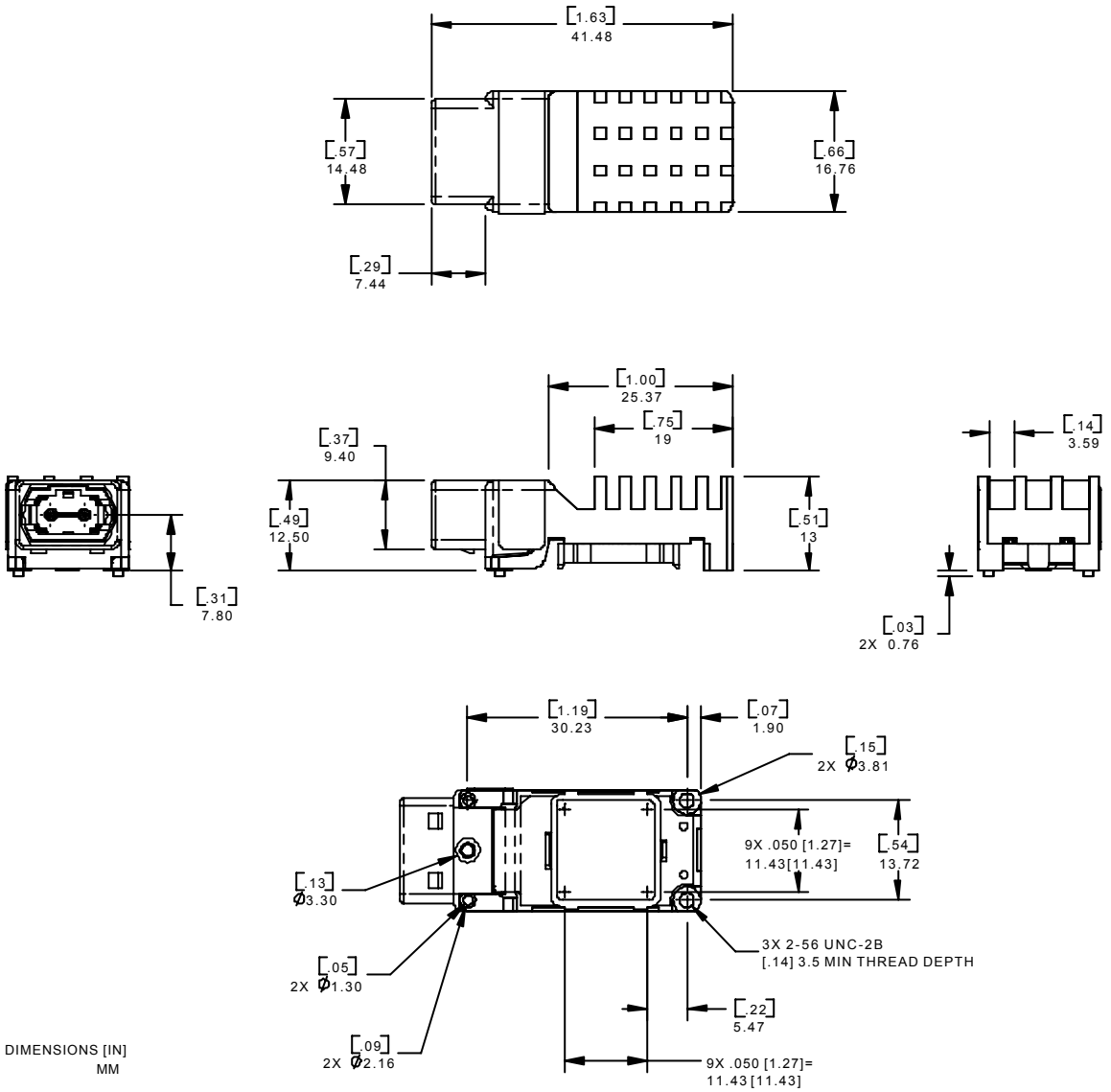


Figure 18 Receiver Module

3.12 Mechanical comparison to SNAP12 MSA

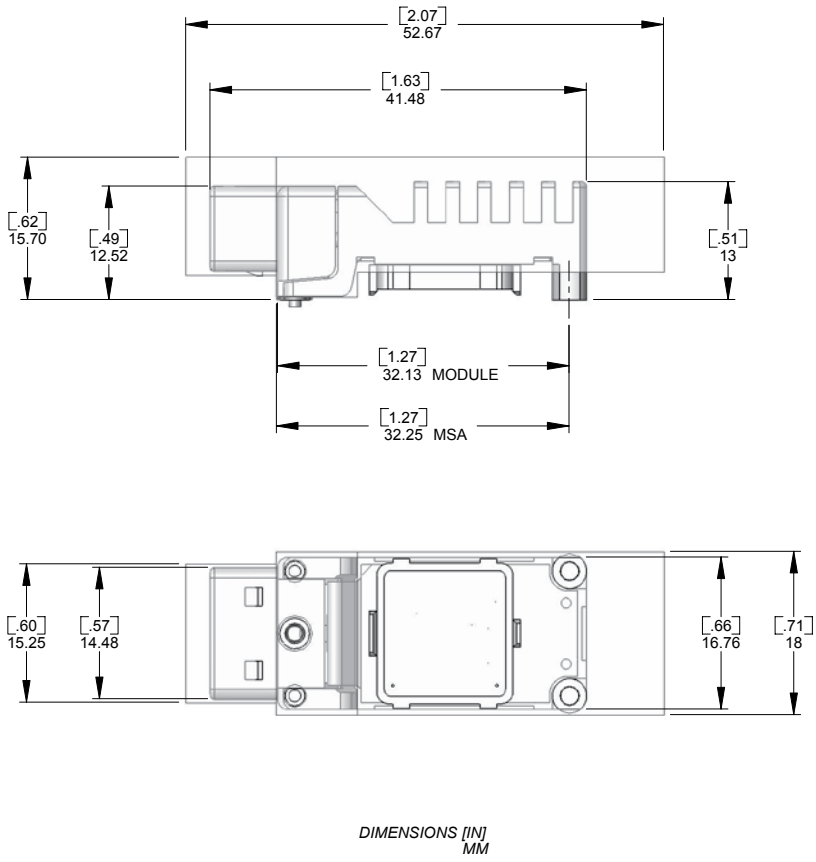


Figure 19

Note: The diagrams above show the mechanical outline of PL-xCP-02-S53-11 modules to the SNAP12 MSA maximum mechanical outline. The JDSU module is indicated in gray.

3.13 Host connector information

Optical	MTP Industry Standard - female
Electrical	MEG-Array #84512-202 manufactured by FCI/Berg meets Telcordia GR-1217-CORE requirements

Note: Recommended PAD size for MEG-array Host Board connector is 0.64 mm (0.025 in)

Section 4 Related Information

Other information related to the 12 x 2.7 Gbps Parallel Optical Transmitter/Receiver includes:

4.1 Package and handling instructions

Process plug
The PL-xCP-02-S53-11 is supplied with a process plug. This plug protects the transmitter/receiver's optics during standard manufacturing processes by preventing contamination from dust or other airborne particles.

Note: It is recommended that the process plug remain in the transmitter/receiver whenever an optical fiber connector is not inserted.

Recommended solder and wash process for host BGA connector
PL-xCP-02-S53-11's mating BGA connector is compatible with standard industry wave solder, hand solder and wash processes. Air knife drying is recommended.

The BGA connector pickup cap must be installed during these process steps.

Recommended cleaning and de-greasing chemicals
JDSU recommends the use of methyl, isopropyl and isobutyl alcohols for cleaning.

Do not use halogenated hydrocarbons (e.g. trichloroethane, ketones such as acetone, chloroform, ethyl acetate, MEK, methylene chloride, methylene dichloride, phenol, N-methylpyrolldone).

Flammability
The PL-xCP-02-S53-11 housing is a metal casting.

4.2 ESD discharge (ESD)

Handling
Normal ESD precautions are required during the handling of this module. This transmitter or receiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Test and operation
In most applications, the optical connector will protrude through the system chassis and be subjected to the same ESD environment as the system. Once properly installed in the system, this transmitter/receiver should meet and exceed common ESD testing practices and fulfill system ESD requirements.

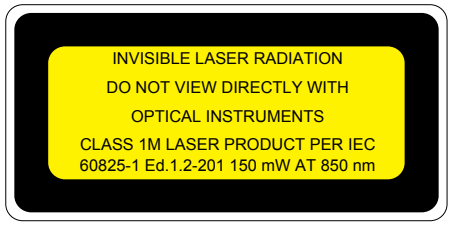
Typical of optical transmitter/receivers, this module's receiver contains a highly sensitive optical detector and amplifier which may become temporarily saturated during an ESD strike. This could result in a short burst of bit errors. Such an event might require that the application re-acquire synchronization at the higher layers (e.g. Serializer/Deserializer chip).

4.3 Eye safety

The PL-TCP-02-S53-11 is a Class 1M Laser Product per IEC/EN 60825-1:2001 and complies with CDRH 21CRF 1040.10 and 1040.11 except for deviations pursuant to Laser Notice no. 50, dated 5/27/2001. The PL-TCP-02-S53-11 is an eye safe device when operated within the limits of this specification. The PL-TCP-02-S53-11 is an eye safe device when no input signals are applied.

Operating this product in a manner inconsistent with intended usage and specification may result in hazardous radiation exposure.

Caution
Tampering with this laser-based product or operating this product outside the limits of this specification may be considered an act of "manufacturing," and will require, under law, recertification of the modified product with the U.S. Food and Drug Administration



Ordering Information

For more information on this or other products and their availability, please contact your local JDSU account manager or JDSU directly at 1-800-498-JDSU (5378) in North America and +800-5378-JDSU worldwide or via e-mail at customer.service@jdsu.com.

Sample: PL-RCP-02-S53-11

Part Number	Description
PL-TCP-02-S53-11	12 x 2.7 Gbps Transmitter with Aluminum body with integrated heat sink and FCI 84513-201 Connector
PL-RCP-02-S53-11	12 x 2.7 Gbps Receiver with Aluminum body with integrated heat sink and FCI 84513-201 Connector
PL-TCP-02-S53-12	12 x 2.7 Gbps Transmitter with Aluminum body with integrated heat sink and FCI 84513-201 Connectorwith EMI collar
PL-RCP-02-S53-12	12 x 2.7 Gbps Receiver with Aluminum body with integrated heat sink and FCI 84513-201 Connector with EMI collar
PL-RCP-02-S53-8A	12 x 2.7 Gbps Receiver with Aluminum body with integrated heat sink and FCI 84513-201 Connector with GSD,VPP Short