CMOS MT90733

DS3 Framer (DS3F)

Preliminary Information

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Features

- Maps broadband payloads in the DS3 format
- DS3 payload access in either bit-serial or nibble-parallel mode
- C-bit parity or M13 operating mode
- Separate interface for C-bits
- Detection and generation of DS3 AIS, and idle signals
- Transmit and receive FEAC channel under software control
- Detection and generation of FEBE, C-bit parity, and P-bit parity errors
- Transmit-to-Receive and Receive-to-Transmit loopbacks

Applications

- Subrate multiplexing
- Wideband data or video transport
- DS3 monitor and test
- Channel extenders
- DS3 test sets

Ordering Information

MT90733AP 68 Pin PLCC

-40° to 85°C

Description

The MT90733 DS3 Framer (DS3F) is designed for mapping broadband payloads, from either a bit-serial or nibble-parallel interface, into the 44.736 Mbit/s DS3 signal. It supports the M13 or C-bit parity format conforming to Bellcore TR-TSY-00009, ANSI T1.107-1988 and supplement T1.107a-1990.

The DS3F uses 21 byte wide registers, accessible under software control for various control and performance monitoring purposes.

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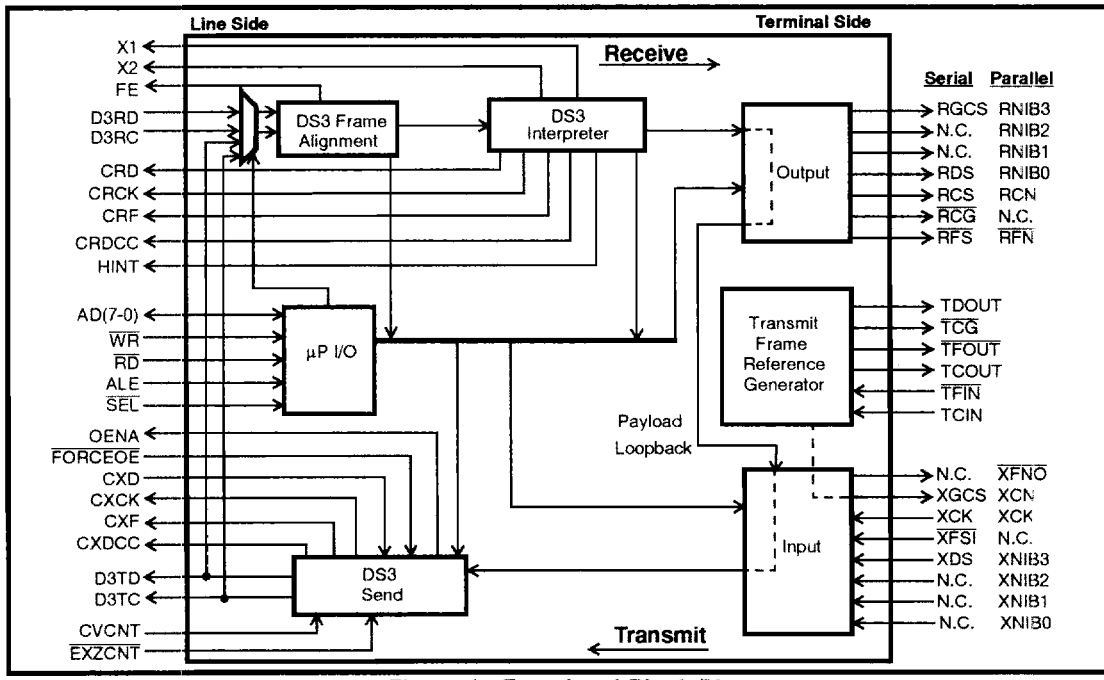

Figure 1 - Functional Block Diagram

U.S. Patent Number 5040170

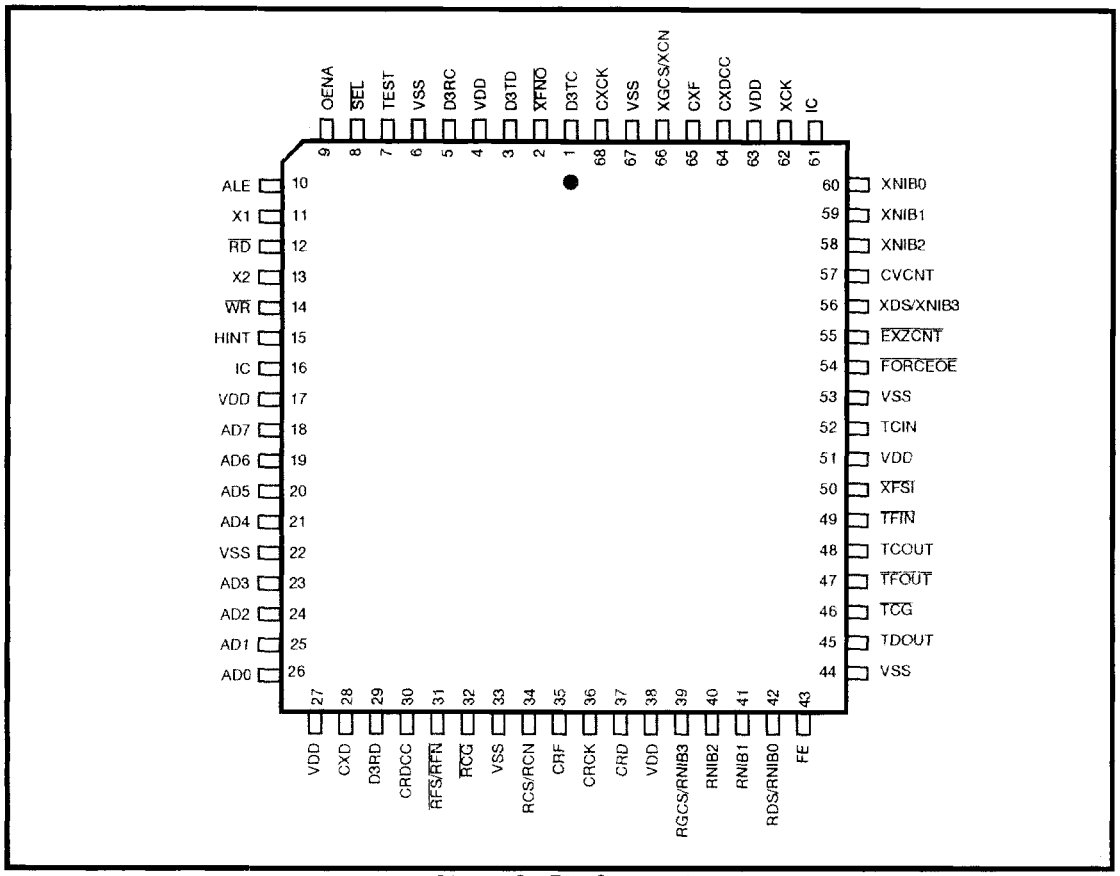

Figure 2 - Pin Connections

Pin Description

Power Supply & Ground

Pin #	Name	I/O/P	Description
4, 17, 27 38, 51, 63	V_{DD}	P	**Power Supply Input.** +5v± 5%.
6, 22, 33 44, 53, 67	V_{SS}	P	**Ground.**

Note: I = Input; O = Output; P = Power

DS3 Receive Line Side Interface

Pin #	Name	I/O/P	Description
5	D3RC	I	**DS3 Receive Clock.** CMOS Type I compatible. A 44.736 MHz clock used for clocking in receive data. It provides a time base for the DS3F receiver.
29	D3RD	I	**DS3 Receive Data.** TTL Type I compatible. DS3 line side serial receive data which is clocked into the DS3F on positive transitions of the receive clock (D3RC).

Note: I = Input; O = Output; P = Power. Refer to DC Characteristics section for CMOS and TTL type definitions.

DS3 Transmit Line Side Interface

Pin #	Name	I/O/P	Description
1	D3TC	O	**DS3 Transmit Clock.** CMOS Type III compatible. A 44.736 MHz clock that is derived from the transmit clock (XCK) signal and is used for clocking out the line side DS3 data signal.
3	D3TD	O	**DS3 Transmit Data.** CMOS Type II compatible. DS3 line side serial transmit data which is clocked out on positive transitions of the transmit clock (D3TC).

Note: I = Input; O = Output; P = Power. Refer to DC Characteristics section for CMOS and TTL type definitions.

Receive Terminal Side Interface

Pin #	Name	I/O/P	Description
31	$\overline{RFS}/\overline{RFN}$	O	**Receive Framing Pulse for Serial/Nibble Interface.** CMOS Type III compatible. The framing pulse is active low for one clock cycle (RCS/RCN), and is synchronous with the first bit in the DS3 frame. For the nibble interface, the framing pulse is synchronous with nibble 1175.
32	$\overline{RCG}$	O	**Receive Clock Gap Signal.** CMOS Type III compatible. An active low gap signal is synchronous with each overhead bit in the serial DS3 frame (first bit in the 85-bit group). In the M13 mode under serial interface, if bit 7 (STFREN) of register 14H is set to one, the stuff bit locations are also identified by $\overline{RCG}$ if 2 out 3 C-bits in that subframe are set to one
34	RCS/RCN	O	**Receive Clock for Serial/Nibble Interface.** CMOS Type III compatible. Clock used for clocking out the terminal side receive serial and nibble data. This clock is derived from the line side clock (D3RC).
39 40 41 42	RGCS/ RNIB3 RNIB2 RNIB1 RDS/RNIB0	O	**Receive Nibble/Serial Interface.** TTL Type III compatible. Nibble Interface: Nibble data (RNIB3-RNIB0) is clocked out on positive transitions of the nibble clock (RCN). There are 1176 nibbles provided in each frame. The data and clock (RCN) are stretched to accommodate the 56 individual overhead bits (first bit in the 85-bit group), which are not provided at the interface. The first bit received in a nibble is present on RNIB3. Serial Interface: Serial data (RDS) is clocked out on negative transitions of the receive clock (RCS). RDS consists of all the bits in the frame (including the overhead bits) of either the M13 or C-bit parity format. A gapped clock for the serial interface (RGCS) is generated by the receive circuitry when bit 2 (SER) of register 01H and bit 5 (RGCEN) of register 0EH are both set to 1. RGCS is gapped (held low) over one clock cycle for each DS3 overhead bit position (first bit in the 85-bit group).

Note: I = Input; O = Output; P = Power. Refer to DC Characteristics section for CMOS and TTL type definitions.

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Transmit Terminal Side Interface

Pin #	Name	I/O/P	Description
2	$\overline{\text{XFNO}}$	O	**Transmit Nibble Interface Framing Pulse.** TTL Type III compatible. An active low, one nibble clock (XCN) cycle wide pulse that occurs during the second nibble time.
50	$\overline{\text{XFSI}}$	I	**Serial Data Transmit Framing Pulse.** TTL Type II compatible. A framing pulse whose leading edge must be synchronous with the first bit in the transmit serial data DS3 frame, and it occurs once per even number of frames. The DS3F rewrites the 56 overhead bits based on the location of the transmit framing pulse. $\overline{\text{XFSI}}$ can be derived from $\overline{\text{TFOUT}}$ (pin 47) by a simply circuit shown in Figure 4. $\overline{\text{XFSI}}$ should not be applied while control bit RTPLOOP (bit 6 of register 0C) is set to 1. $\overline{\text{XFSI}}$ may also be used for resetting registers in the memory map. If $\overline{\text{XFSI}}$ is held low for a duration greater than 1 frame, then reset to zero of all register bit positions at registers 02H-04H, 05H bit 7 and 08H-14H will occur until this pin is taken high.
56 58 59 60	XDS/XNIB3 XNIB2 XNIB1 XNIB0	I	**Transmit Nibble/Serial Interface.** TTL Type I compatible. Nibble Interface: Nibble data (XNIB3-XNIB0) is clocked in on positive transitions of the nibble clock (XCN). There are 1176 nibbles in each frame. XCN is stretched to accommodate the 56 overhead bits which are not required at the interface. The DS3F inserts the X, F, C, P, and M overhead bits into the transmitted frame based on the framing pulse $\overline{\text{XFNO}}$. The first bit transmitted in a nibble is present on XNIB3. Serial Interface: The serial data (XDS) is clocked into the DS3F on positive transitions of the transmit clock (XCK). XDS should consist of all the bits in the frame (4760 bits). The DS3F rewrites the 56 overhead bits in the frame based on the location of the framing pulse $\overline{\text{XFSI}}$, when operating in the C-bit parity mode. In the M13 operating mode, the 21 C-bits are treated as user data, while the other overhead bits (X, F, P, and M bits) are written into the DS3 frame by the DS3F.
62	XCK	I	**Transmit Clock.** CMOS Type I compatible. A 44.736 Mbit/s ±20 ppm clock with a duty cycle 50 ±10%. XCK provides the time base for the transmitter in the DS3F. If XCK fails, the DS3F uses the receive clock (D3RC) instead.
66	XGCS/XCN	O	**Transmit Clock for Nibble/Serial Interface.** TTL Type III compatible. XGCS is a gapped clock signal generated by the Timing Generator circuit for the serial interface. To use TGCS, both bit 2 (SER) of register 01H and bit 4 (TGCEN) of register 0EH must be set to 1. TGCS is gapped (held high) over one clock cycle for each DS3 overhead bit position (first bit in the 85-bit group). XCN is the clock signal for transmit nibble data. XCN is stretched in order to accommodate the 56 overhead bit positions which are not required by the external terminal circuitry for the nibble interface (XNIBn).

Note: I = Input; O = Output; P = Power. Refer to DC Characteristics section for CMOS and TTL type definitions.

Transmit Reference Generator Interface

Pin #	Name	I/O/P	Description
45	TDOUT	O	**Transmit Reference Generator Data Output.** TTL Type III compatible. A DS3 signal contains either frames of all zeros (including overhead bits) or frames of all ones in the overhead bit positions and zeros elsewhere. The pattern is as follows: The number of frames with ones in the overhead bit positions is 7 of every 18 frames. They are one frame of every three for the first 15 frames and two of the last 3 of the 18-frame group; the rest of frames in the 18-frame group contain all zeros everywhere. this completes the 7 of 18 pattern.
46	$\overline{TCG}$	O	**Transmit Reference Generator Clock Gap Signal.** TTL Type III compatible. An active low, one clock cycle wide (TCOUT) pulse that is synchronous with the first bit (the overhead bit) in each 85-bit group of the DS3 frame.
47	$\overline{TFOUT}$	O	**Transmit Reference Generator Framing Pulse.** TTL Type III compatible. An active low, one clock cycle wide (TCOUT) pulse that is synchronous with the first bit in the DS3 frame. May be used as the serial data transmit framing pulse ($\overline{XFSI}$) if properly delayed by the payload multiplexer circuitry.
48	TCOUT	O	**Transmit Reference Generator Clock Out.** CMOS Type III compatible. A clock signal, derived from the transmit reference generator clock input (TCIN), provides a time base for multiplexing an external payload into the serial signal TDOUT provided by the reference generator. TCOUT may also be used as the transmit input clock (XCK) in the serial mode. Transmit reference generator signals are clocked out on positive transitions of TCOUT.
52	TCIN	I	**Transmit Reference Generator Clock In.** TTL Type I compatible. A 44.736 Mbit/s ±20 ppm clock with a duty cycle of 50 ±10%. TCIN provides a time base for generating the various signals in the DS3F transmit reference generator.

Note: I = Input; O = Output; P = Power. Refer to DC Characteristics section for CMOS and TTL type definitions.

Receive C-Bit Interface

Pin #	Name	I/O/P	Description
30	CRDCC	O	**C-Bit Receive Data Link Clock.** TTL Type III compatible. When bit 4 of register 0CH, M13DLM =0: CRDCC provides a gapped clock for clocking the three data link bits (C13, C14, and C15) into external circuitry from the serial data (CRD). In addition, the timing of CRDCC pulses can be advanced by one-half CRCK cycle if the control bit CRDCINV (bit 0 of register 0EH) is set to 1. When bit 4 of register 0CH, M13DLM =1: CRDCC becomes a single envelope pulse (three CRCK cycle wide) to indicate the position of data link bits (C13, C14, and C15).
35	CRF	O	**C-Bit Receive Framing Pulse.** TTL Type III compatible. Provides a time base reference for clocking in the C-bits in a DS3 frame.
36	CRCK	O	**C-Bit Receive Clock.** TTL Type III compatible. A gapped clock which clocks C-bit data out of the DS3F.
37	CRD	O	**C-Bit Receive Data.** TTL Type III compatible. Serial interface for receiving the following C-bits in the C-bit parity mode: C2, C3, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. CRD is clocked out by the clock signals CRDCC and CRCK. The falling edge of CRCK indicates when valid data is available.

Note: I = Input; O = Output; P = Power. Refer to DC Characteristics section for CMOS and TTL type definitions.

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Transmit C-Bit Interface

Pin #	Name	I/O/P	Description
28	CXD	I	**C-Bit Transmit Data.** TTL Type I compatible. Serial interface for transmitting the following C-bits in the C-bit parity mode: C2, C4, C5, C6, C13, C14, C15, C16, C17, C18, C19, C20, and C21. C-bit data is clocked into the DS3F on positive transitions of the C-bit gapped clock (CXCK). A C-bit must be transmitted as a one if not used.
64	CXDCC	O	**C-Bit Transmit Data Link Clock.** TTL Type III compatible. When bit 4 of register 0CH, M13DLM =0: CXDCC provides a gapped clock for clocking the three data link bits (C13, C14, and C15) into the DS3F from the serial data (CXD). When bit 4 of register 0CH, M13DLM =1: CXDCC becomes a single envelope pulse (three CXCK cycle wide) to indicate the position of data link bits (C13, C14, and C15).
65	CXF	O	**C-Bit Transmit Framing Pulse.** TTL Type III compatible. Identifies the location of the first C-bit (C1) in the DS3 frame.
68	CXCK	O	**C-Bit Transmit Clock.** TTL Type III compatible. A gapped clock which clocks the external C-bit serial data (CXD) into the DS3F.

Note: I = Input; O = Output; P = Power. Refer to DC Characteristics section for CMOS and TTL type definitions.

Other Signals

Pin #	Name	I/O/P	Description
7	TEST	I	**Test Pin.** Leave open.
9	OENA	O	**Overhead Enable.** TTL Type III compatible. An active high signal that enables an overhead error to be introduced into the overhead bit in the next 85th group by placing a low on the FORCEOE lead.
11	X1	O	**DS3 Received X-Bit 1.** TTL Type III compatible. An output of the state of the first X-bit (X1) received in the DS3 frame (bit 1). The state of this pin is held until the next X1 bit is detected.
13	X2	O	**DS3 Received X-Bit 2.** TTL Type III compatible. An output of the state of the second X-bit (X2) received in the DS3 frame (bit 680). The state of this pin is held until the next X2 bit is detected.
15	HINT	O	**Hardware Interrupt.** TTL Type III compatible. If bit 2 (HINTEN) of register 0EH is set to one, an active high signal is presented on this pin to inform the microprocessor that a severe alarm condition has occurred. When at least one of the eight interrupt enable mask bits (Address 11H, bits 7-0) is 1, occurrence of a corresponding alarm condition causes HINT pin to go high. HINT may be used as input to the interrupt pin of the microprocessor, and it can be changed to active low by setting bit 3 (HINTINV) of register 0EH to one.
16	IC	-	**Internal Connection.** Leave open.
43	FE	O	**Framing Error Indication.** TTL Type III compatible. The FE pin will go high for a period of 85 DS3 clock cycles (1.9µs) when a F-bit framing error is detected. When no F-bit error occurs or during an Out of Frame condition the FE pin is held low.

Other Signals

Pin #	Name	I/O/P	Description
49	$\overline{\text{TFIN}}$	I	**Transmit Framing Input.** TTL Type II compatible. An optional active low input signal which resets the counters of the Transmit Frame Reference Generator block to zero and holds the output signals of the block to their corresponding states.
54	$\overline{\text{FORCEOE}}$	I	**Force DS3 Overhead Bit Error.** TTL Type II compatible. An active low signal used in conjunction with the overhead enable signal (OENA) for introducing an overhead bit error in the next transmitted 85-bit group.
55	$\overline{\text{EXZCNT}}$	I	**Excessive Zeros Count Input.** TTL Type II compatible. This pin is intended to be driven by the Excessive Zeros output pin ($\overline{\text{EXZ}}$) of a DS3 line interface. An internal 16-bit counter, CVEXZ at Addresses 12H and 13H, is incremented when the pin is low during the falling edge of the DS3 receive clock (D3RC). To activate the counter, a one must be written into bit 1 (EXZEN) of register 14H.
57	CVCNT	I	**Coding Violation Count Input.** TTL Type II compatible. This pin is intended to be driven by the Coding Violation (CV) output pin of a DS3 line interface. An internal 16-bit counter, CVEXZ at Addresses 12H and 13H, is incremented when the pin is high during the falling edge of the DS3 receive clock (D3RC). To activate the counter, a one must be written into bit 0 (CVEN) of register 14.
61	IC	-	**Internal Connection.** Set to high for normal operation.

Note: I = Input; O = Output; P = Power. Refer to DC Characteristics section for CMOS and TTL type definitions.

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Microprocessor Interface

Pin #	Name	I/O/P	Description
8	$\overline{\text{SEL}}$	I	**Microprocessor Select.** TTL Type I compatible. A low enables the microprocessor to access the DS3F memory map for control, status and alarm information.
10	ALE	I	**Address Latch Enable.** TTL Type I compatible. An active high signal generated by the microprocessor. Used by the microprocessor to hold an address stable during a read/write bus cycle on the falling edge.
12	$\overline{\text{RD}}$	I	**Read.** TTL Type I compatible. An active low signal generated by the microprocessor for reading the registers which reside in the DS3F memory map. The DS3F memory I/O is selected by placing a low on the select lead.
14	$\overline{\text{WR}}$	I	**Write.** TTL Type I compatible. An active low signal generated by the microprocessor for writing to the registers which reside in the memory map. The DS3F memory I/O is selected by placing a low on the select lead.
18-21 23-26	AD(7-4) AD(3-0))	I/O	**Address/Data Bus.** TTL Type IV compatible. These leads constitute the time multiplexed address and data bus for accessing the registers which reside in the DS3F memory map.

Note: I = Input; O = Output; P = Power. Refer to DC Characteristics section for CMOS and TTL type definitions.

Functional Description

The MT90737 (DS3F) is designed for DS3 framer applications in which broadband payloads, through either a bit serial or nibble-parallel interface, are mapped into the DS3 frame in either M13 or C-bit parity format. A separate interface for selected C-bits is provided in the C-bit parity operation mode. Under software control, the DS3F can transmit and receive the Far End Alarm & Control (FEAC) channel, generate and detect DS3 AIS, DS3 idle, P-bit parity and C-bit parity. In addition, the DS3F also provides various performance counters (for FEBE, C-bit parity error, P-bit parity error, etc.), hardware interrupt signal (maskable for eight alarm conditions), as well as loopback functions (transmit-to-receive and receive-to-transmit).

Operating at 44.736 Mbit/s, the DS3 signal has a framed structure, which is shown in Figure 3. The DS3 signal is partitioned into M-frames of 4760 bits each. An M-frame consists of seven M-subframes of 680 bits. Each M-subframe is further divided into 8 blocks of 85 bits with 84 of the 85 bits available for payloads and one used for frame overhead.

The DS3F supports two different DS3 signal formats - the M13 format and the C-bit parity format. The operating mode is chosen by writing a control bit, MODE (bit 3 of register 01H). A one in MODE enables the DS3F to operate in the M13 mode as specified in Bellcore TR-TSY-000009 and the ANSI T1.107-1988. A zero in MODE enables the DS3F to operate in the C-bit parity mode as specified in the ANSI T1.107-1988 and supplement ANSI T1.107a-1990. In the M13 mode the C-bits are used for stuffing control, while in the C-bit parity mode, they are redefined for providing end-to-end path performance monitoring and in-band data links. Table 1 shows the DS3 C-bit assignments in the C-bit parity format.

DS3 Receive

The DS3F receives a DS3 data signal (D3RD), clocked in on positive transitions of the DS3 receive clock (D3RC), from a line interface device. The DS3 Frame Alignment Block performs DS3 frame alignment, monitors the input signal and clock for Loss of Signal (LOS), Out Of Frame (OOF), and Loss Of Clock (LOC). These alarms are reported by their corresponding status bits in the memory map. A framing error (FE) output is provided to indicate when any of the 28 framing bits in the DS3 signal are in error. A one will present on FE pin for a period of 85 clock cycles (1.9µs) if a F-bit error is detected. Furthermore, the DS3F also provides an F-bit error counter (register 0AH) and an M-bit error counter (register 0BH) that can be accessed via software.

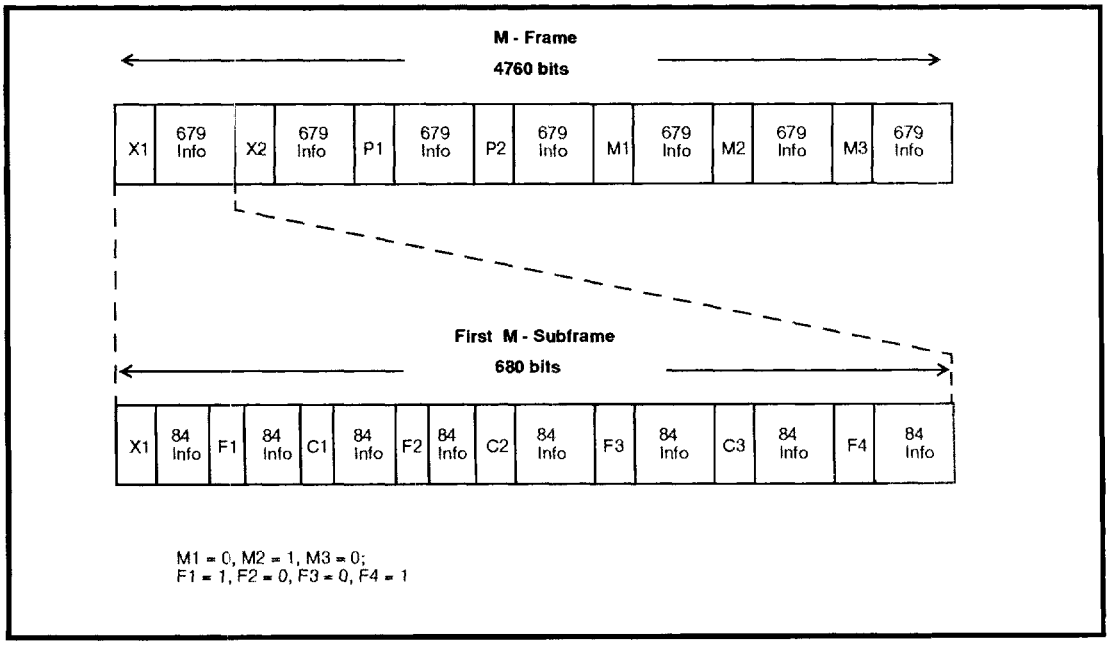

Figure 3 - The DS3 Frame Stucture

The DS3 Interpreter Block performs P-bit and C-bit parity detection and error counting, receive AIS and idle signal detection, far end block error (FEBE) detection and error counting, far end alarm and control (FEAC) code word detection, C-bit reception and X-bit reception.

P-Bit Parity Detection

The P-bits, two in each DS3 frame, carry the parity information of the preceding frame for performance monitoring. In any DS3 frame, the two P-bits shall be identical. The DS3 sources compute parity over all 4704 DS3 payload bits in a DS3 frame and insert the resulting parity information in the P-bits of the following frame. The two P-bits are set to one if the previous DS3 frame contains an odd number of ones in payload. Conversely, the two P-bits are set to zero if an even number of ones is found in the previous DS3 frame payload.

The DS3F detects P-bit parity error by comparing the received P-bits with the desired values calculated based on the payload in the preceding DS3 frame. An 8-bit saturating counter (register 04H) is used for counting the P-bit parity errors.

C-Bit Parity Detection

In the C-bit parity mode, the three C-bits (C7, C8, and C9) in the third subframe, designated as CP-bits, are used to carry parity information from source terminal to sink terminal. The three CP-bits are set to the same value of the P-bits in the DS3 source terminal. While values of the P-bits may be modified by some equipment in a DS3 path, the CP-bits are not altered by any intermediate equipment. Therefore, an end-to-end parity checking capability is offered in the C-bit parity mode.

The DS3F detects the C-bit parity errors and counts the errors in an 8-bit saturating counter (register 03H).

Alarm Indication Signal (AIS) Detection

The Alarm Indication Signal (AIS) is a maintenance signal that is inserted into the DS3 stream when a failure is detected. The DS3F detects the AIS signal as defined in ANSI T1.107a-1990, which is described as follows:

- Valid M-bits, F-bits, and P-bits;
- All C-bits are zeros;
- X-bits are set to 1;
- 1010... repeating sequence for the information bit.

The DS3F will set bit 5 (RXAIS) of register 00H to 1 if a AIS pattern is found in the receive DS3 stream.

IDLE Signal Detection

The IDLE signal is used to indicate that the DS3 channel is functionally sound, but has not yet been assigned to any traffic. The DS3F detects the idle signal as defined in ANSI T1.107a-1990, which is described as follows:

- Valid M-bits, F-bits, and P-bits;
- The three C-bits in subframe 3 (CP bits) are zeros;
- X-bits are set to 1;
- 1100... repeating sequence for the information bit.

The DS3F will set bit 4 (RXIDL) of register 00H to 1 if an idle pattern is found in the receive DS3 stream.

Subframe	C-bits			Function
1	C1	C2	C3	C1 = Application Identification C2 = Reserved C3 = Far End Alarm & Control (FEAC)
2	C4	C5	C6	Not defined
3	C7	C8	C9	C-Parity bits (CP-bits)
4	C10	C11	C12	Far End Block Error (FEBE)
5	C13	C14	C15	Maintenance data link (28 Kbit/s)
6	C16	C17	C18	Not defined
7	C19	C20	C21	Not defined

Table 1 - C-Bit Assignments in the C-bit Parity Format

Receive FEAC

The third C-bit (C3) in the first subframe is used as Far End Alarm and Control (FEAC) channel between the far end DS3 terminal and the near end DS3 terminal. The FEAC channel carries:

- Alarm and status information,
- Loopback commands to initiate and deactivate DS3 and DS1 loopbacks at the distant terminal.

FEAC signals are encoded into repeating 16-bit codewords of the form 0xxxxxx011111111 (where x can be either 1 or 0), with the right-most bit transmitted first. The 6 bits labeled x can represent 64 distinct messages, of which 43 have been defined in the standard. When the FEAC channel is used as far end alarm signals, the FEAC codeword shall be transmitted continuously for the duration of the alarm condition, or 10 repetitions of the codeword, whichever is longer. When the FEAC is used to control DS3 and DS1 loopbacks, ten repetitions of either the activate or deactivate codeword is transmitted first, immediately followed by ten repetitions of the codeword identifying the DS3 or DS1 line (or all). The DS3F detects FEAC messages and stores them in an internal four-word deep stack. The top word of the stack can be accessed from the memory map (bits 5-0 of register 0FH).

Receive FEBE

The three C-bits (C10, C11, and C12) in subframe 4 are designated as Far End Block Error (FEBE) channel. If a CP-bit parity error or a framing error is detected on the incoming signal, the FEBE bits shall be set to any pattern other than 111 to indicate an error. The FEBE bits are set to 111 only if both of the following conditions are true:

- No M-bit or F-bit framing error has occurred, and
- No CP-bit parity error has occurred.

Therefore, in the C-bit parity application, with the FEBE function and FEAC signals, the overall performance of the full-duplex DS3 path can be determined at either end of the path. The DS3F uses an 8-bit counter (register 02H) to count the number of FEBE indications received. A FEBE indication is defined as any one or more of the C10, C11, or C12 bits in a DS3 frame being zero.

Receive C-Bit Interface

In the C-bit parity mode, a separate interface is provided for receive 14 of the 21 C-bits. The receive C-bit interface consists of a serial data signal (CRD), a clock signal (CRCK), a framing pulse (CRF), and a data link clock signal (CRDCC). The receive C-bit clock signal (CRCK) is gapped and is available for clocking out C-bits C2 through C6, and C13 through C21. The data link clock signal (CRDCC) is present for the data link C-bits (C13, C14 and C15). A control bit, M13DLM (bit 4 of register 0CH) is available to let CRDCC be either a gapped clock (M13DLM = 0) or an envelope pulse (M13DLM = 1). Refer to Figure 16 for the receive C-bit interface timing.

X-Bits Reception

X-bits are used for sending yellow alarm. When a DS3 receiver cannot identify valid framing, or detects an AIS, it should send a yellow alarm by setting the transmit X-bits to zero in the returning DS3 path. The X-bits are set to one under non-alarm condition.

The received X-bits can be accessed from either two output pins, X1 and X2 (pin 11 and 13) or two bits, XRX1 and XRX2 (bits 0-1 of register 00H) in the memory map.

Hardware Interrupt (HINT)

The Hardware Interrupt output (HINT, pin 15) is used to inform the microprocessor that a severe alarm condition has occurred if the HINT enable bit, HINTEN (bit 2 of register 0EH) is set to one. The polarity of the Hardware Interrupt output is selectable by a control bit, HINTINV (bit 3 of register 0EH), to meet the requirements of the microprocessor's interrupt input pin. The occurrence of a hardware interrupt may be caused by one or more of up to eight different latched alarm conditions (in register 10H) if corresponding enable bits (in register 11H) are set.

Terminal Side Interface for Data Output

The Output Block provides a bit-serial or a nibble-parallel interface for both C-bit parity and M13 modes of operation. The interface type is selected by writing to a control bit, SER (bit 2 of register 01H), and is common to the DS3F receive and transmit circuitry. The signals provided for the bit-serial interface consist of a data signal (RDS), a gapped clock signal (RGCS), a receive clock signal (RCS), a receive clock gap signal ($\overline{\text{RCG}}$) and framing pulse ($\overline{\text{RFS}}$). The nibble-parallel interface consists of the

nibble data signal (RNIB3 through RNIB0), a clock out signal (RCN), and a framing pulse output ($\overline{RFN}$). The RNIB3 bit corresponds to the first bit received in a four-bit serial bit stream segment.

DS3 Transmit

In the transmit direction, the DS3F maps the terminal side input payloads (serial or nibble data) into the DS3 frame in either the M13 format or C-bit parity format. The transmit DS3 data (D3TD) is clocked out of the DS3F on positive transitions of the transmit clock (D3TC).

Terminal Side Interface for Data Input

The Input Block provides either a bit-serial or nibble-parallel interface for the terminal side input data. The bit-serial interface consists of a data signal (XDS), a gapped clock signal (XGCS), a transmit clock signal (XCK), and a framing pulse ($\overline{XFSI}$). The framing pulse, synchronous with the first bit of a DS3 frame, must occur once per even number of frames. Figure 4 shows a circuit that can be used to derive an $\overline{XFSI}$ pulse every two frames from the $\overline{TFOUT}$ (pin 47) signal, which occurs at bit 1 of every frame.

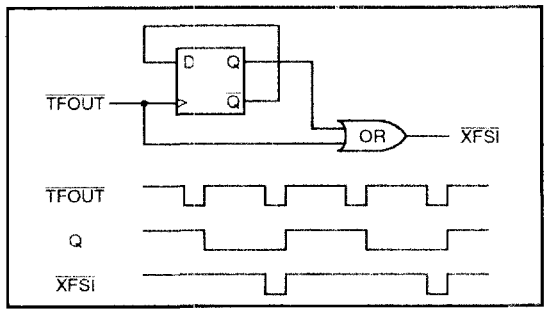

Figure 4 - $\overline{XFSI}$ Pulse Derived From $\overline{TFOUT}$

The nibble-parallel interface consists of a nibble data (XNIB3 through XNIB0), a transmit clock signal (XCK), a framing pulse ($\overline{XFNO}$), and a nibble clock signal (XCN). The XNIB3 bit corresponds to the first bit transmitted.

The DS3 Send Block performs P-bit and C-bit parity generation, AIS and idle pattern generation, Far End Alarm and Control (single or double FEAC codeword) transmission, X-bit insertion, and C-bit insertion. The C-bits may be generated internally (such as C-bit parity), written by the microprocessor (such as the FEAC channel), or provided from the external C-bit interface. The capability to generate and transmit single overhead bit errors is also provided.

P-Bit and C-Bit Parity Generation

The DS3F calculates the parity over all 4704 information bits in a DS3 frame and inserts the result into the P-bits of the following DS3 frame. In the C-bit parity mode, the CP-bits (C7, C8, and C9) are also set to the same value as the P-bits in the DS3 frame.

AIS and Idle Signal Generation

The DS3F may generate and transmit DS3 AIS and idle signals under software control. A one written in bit 6 (TXAIS) of register 01H enables the DS3F to transmit an AIS signal. If bit 5 (ENAIS) of register 01H is set to one, the DS3F will automatically transmit DS3 AIS whenever a receive DS3 Out of Frame (RXOOF) condition is detected. To transmit a DS3 idle signal, a one must be written into bit 4 (TXIDL) of register 01H. Note that in order to ensure a successful transmission of DS3 AIS or idle signal, a one must be written (if not yet) into bit 0 (XTX) of register 01H to set the transmit X-bits to one.

FEAC Transmission

Under software control, the transmission of FEAC messages is either continuous, or single codeword (10 repetitions of the 16-bit FEAC codeword), or double codeword (10 repetitions of a FEAC codeword followed by 10 repetitions of another FEAC codeword).

- *Continuous FEAC Transmission*: A one written into bit 6 (START) of register 05H enable the DS3F to start sending repetitively a FEAC codeword with the x labeled bits taken from bits 5-0 of register 05H, provided that the bit 7 (FEAC10) of register 0EH contains a zero.

- *Single FEAC Transmission*: If the bit 7 (FEAC10) of register 0EH is set to 1, a one in the START bit enables the DS3F to send exactly 10 times a FEAC codeword with x labeled bits taken from bits 5-0 of register 05H.

- *Double FEAC Transmission*: When bit 6 (DFEXEC) of register 0DH is set to 1, the DS3F transmits 10 repetitions of a FEAC codeword with x labeled bits taken from bits 5-0 of register 0DH, followed by 10 repetitions of a FEAC codeword with x labeled bits taken from bits 5-0 of register 05H.

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X-Bit Insertion

The value of inserted X-bits is selectable by setting bit 0 (XTX) of register 01H. A one written in XTX causes the DS3F to transmit a one for both X1 and X2 bits. Each of the transmit X1 and X2 bits may also be individually inverted by writing a one into bit 2 (ITX1) and bit 3 (ITX2) of register 08H.

Transmit C-bit Interface

A separate interface is provided for transmit 13 of the 21 C-bits. These 13 C-bits are C2, C4-6, and C13-21. The transmit C-bit interface consists of a data input signal (CXD), a clock signal (CXCK), a framing pulse (CXF) and a data link clock signal (CXDCC). A control bit, M13DLM (bit 4 of register 0CH) is available to let CXDCC be either a gapped clock (M13DLM = 0) or an envelope pulse (M13DLM = 1). Note that this C-bit interface may be completely or partially turned off by setting control bits DLCB1 (bit 3 of register 0CH), C2OFF (bit 2 of register 0CH) and MCB1 (bit 1 of register 0CH).

Error Insertion

A one written into FORCECP (bit 3 of register 14H), FORCEPP (bit 4 of register 14H), and FORCEFEBE (bit 5 of register 14H) causes the DS3F to send C-bit parity error, P-bit parity error, and FEBE error respectively. In addition, if bit 0 (CPARINV) of register 0CH is set to one, the CP-bits and FEBE will be set to the inverse of their corresponding states. The overhead bit error may also be inserted from the pins. The $\overline{\text{FORCEOE}}$ pin (pin 54) is used in conjunction with the enable signal (OENA, pin 9) for introducing an overhead bit error in the next 85-bit segment of the DS3 frame.

Miscellaneous

Initialization

During the initialization, a one must be written into the INI bit (bit 7 of register 05H), and all unused read/write bits in the memory map are to be set to zero by the software.

Loopbacks

The DS3F transmit-to-receive (TR) loopback is activated by setting bit 1 (3LOOP) of register 01H to one. The entire device is used when TR loopback is in effect, but the line side input data and clock are blocked (by the gate preceding the DS3 Frame Alignment Block shown in Figure 1). A receive-to-transmit payload (RTP) loopback is also available by setting control bits RTPLOOP (bit 6 of register 0CH) and RTPLLEN (bit 7 of register 0CH).

Receive Loop Timing

A one written in LPTIME (bit 0 of register 08H) disables the transmit clock (XCK) and causes the DS3 receive clock (D3RC) to become the DS3 transmit clock. If D3RC fails during the receive loop timing, the DS3F will automatically switch over to the original transmit clock (XCK).

Transmit Frame Reference Generator

The Transmit Frame Reference Generator Block provides reference timing for bit-serial operation. This block accepts an external 44.736MHz clock signal (TCIN) and derives a clock signal (TCOUT), a framing pulse ($\overline{\text{TFOUT}}$), a clock gap signal ($\overline{\text{TCG}}$), a transmit gapped clock signal (XGCS) and a data signal (TDOUT). TDOUT contains frames of either all zeros, or all ones in the overhead bit positions and zeros elsewhere. The purpose of the TDOUT signal is to provide external circuitry with a time reference for stuff control in the M13 type multiplexing. An optional input framing pulse ($\overline{\text{TFIN}}$) is also provided to reset the reference generator, but is not required for normal operation.

Unframed All Ones Signal

The DS3F can transmit and detect unframed all ones signal. A one written into bit 5 (TALL1) of register 08H enables the DS3F to transmit unframed all ones.When an unframed all one signal is received, bit 5 (RALL1) of register 09H will be set to one.

Severely Errored Frame (SEF) Detection

A Severely Errored Frame (SEF) is defined as three out of sixteen F-bits in error. The DS3F uses a sliding window of sixteen F-bits to monitor the SEF condition and report it in bit 7 (SEF) of register 09H.

Coding Violation/Excessive Zero Counter

A 16-bits saturating counter (register 12H and 13H) is provided to count events on input pin CVCNT (pin 57). Events on input pin $\overline{\text{EXZCNT}}$ (pin 55) are also counted if bit 1 (EXZEN) of register 14H is set to one. Indications of these events (Coding Violation and/or Excessive Zeros) are provided to the DS3F by line interface devices such as TranSwitch's ART/ARTE (TXC-02020/02021). The DS3F has an internal 16-bit shadow counter incorporated into its counter

design to prevent event counts being lost during a read cycle. Note that to utilize the coding violation/ excessive zero counter, bit 0 (CVEN) of register 14 must be set to one.

Microprocessor Interface

The DS3F microprocessor interface consists of an 8-bit multiplexed data and address bus (AD0-AD7), along with other microprocessor control leads. The microprocessor bus is used to write control information and to read status information and alarms from the DS3F memory map that contains twenty-one byte registers (00H-14H).

Tri-State Output Pins

A one written into bit 4 (OUTDIS) of register 08H will tri-state all output pins except the microprocessor address/data bus.

Throughput Delays

The DS3F throughput delays for the serial terminal interface are given below in terms of DS3 bit times (1 bit = 22.35 nsec nominal):

1. The throughput delay from the transmit terminal side input to the transmit line side output is 3 bit times.

2. The throughput delay from the receive line side input to the receive terminal side output is 2 bit times.

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Memory Map

Address (Hex)	Mode*	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	R	RXLOS	RXOOF	RXAIS	RXIDL	RXLOC	TXLOC	XRX2	XRX1
01	R/W	NOFEBE	TXAIS	ENAIS	TXIDL	MODE	SER	3LOOP	XTX
02	R	FEBE / Framing Bit Error Performance Counter (saturating counter, clears when read)							
03	R	C-Bit Parity Error Performance/Number of Frames Counter (saturating counter, clears when read)							
04	R	P-Bit Parity Error Performance Counter (saturating counter, clears when read)							
05	R/W	INI	START	FEAC Transmit Data					
06	R	FIDL	NEW	FEAC Receive Data					
07	R(L)	RXLOS	RXOOF	RXAIS	RXIDL	CERR	LOC	X2ERR	X1ERR
08	R/W	FBEC	MBEC	TALL1	OUTDIS	ITX2	ITX1	RESET	LPTIME
09	R(L)	SEF	Unused**	RALL1	Unused**	Unused**	Unused**	Unused**	STKOVFL
0A	R	F-Bit Error Counter (saturating counter, clears when read)							
0B	R	M-Bit Error Counter (saturating counter, clears when read)							
0C	R/W	RTPLLEN	RTPLOOP	TESTLOCK	M13DLM	DLCB1	C2OFF	MCB1	CPARINV
0D	R/W	Unused**	DFEXEC	Double FEAC Transmit Data					
0E	R/W	FEAC10	Unused**	RGCEN	TGCEN	HINTINV	HINTEN	MOOFW	CRDCINV
0F	R	MOREFEAC	FEACVLID	RFEAC6	RFEAC5	RFEAC4	RFEAC3	RFEAC2	RFEAC1
10	R(L)	RXLOS	RXOOF	RXAIS	RXIDL	NEWFEAC	RTLOC	SEF	XERR
11	R/W	RXLOSEN	RXOOFEN	RXAISEN	RXIDLEN	NFEACIEN	RTLOCEN	SEFEN	XERREN
12	R	Coding Violation / Excessive Zeros Counter, low order byte (saturating counter, clears when read)							
13	R	Coding Violation / Excessive Zeros Counter, high order byte (saturating counter, clears when read)							
14	R/W	STFREN	STFTGEN	FORCEFEBE	FORCEPP	FORCECP	TSTCNTR	EXZEN	CVEN

* Note: R = Read-only; R(L) = Read-only, latched (clears on read); R/W = Read/Write.

** Note: All unused read-only bits will contain 0. All unused read/write bits are to be set to 0 by the application software.

Memory Map Description

Address	Bit	Symbol	Description
00	7	RXLOS	**Receive DS3 Loss of Signal.** A receive LOS alarm occurs (RXLOS is set to 1) when the incoming DS3 data (D3RD) is stuck low for at least 2048 clock cycles (D3RC). Recovery occurs when two or more ones are detected in the incoming data bit stream.
	6	RXOOF	**Receive DS3 Out of Frame.** A receive OOF occurs (RXOOF is set to 1) when three out of 16 F-bits in a sliding window of 16 bits are in error, or when there are M-bit errors in two frames out of a window of three (if register 0EH, bit 1, MOOFW=1) or four (MOOFW=0) consecutive frames. Recovery occurs when 16 consecutive error-free F-bits (in a repeating 1001 pattern) are detected, followed by the M-bit pattern of 010 being detected for two consecutive frames. Recovery takes approximately 0.95 milliseconds in the worst case. An OOF also inhibits the performance counters at Addresses 02H, 03H, 04H, 0AH and 0BH. The terminal side data output during an RXOOF condition is the received data.
	5	RXAIS	**Receive DS3 Alarm Indication Signal (AIS).** When receive DS3 AIS condition is declared, RXAIS is set to 1. A DS3 AIS condition is declared if all of the following events have occurred during a frame: • Address 00H, bit 6, RXOOF is 0, • The three C-bits in each subframe have been 0 for five consecutive frames, • At least 95% of the payload of each subframe has contained a repeating 1010 bit sequence which begins after each overhead bit for two consecutive frames, • The latest X-bit received is the sixteenth or higher that has arrived with a value of one in the most recent nineteen X-bits received. Recovery occurs (RXAIS is reset to 0) during the first subsequent subframe when one of the above events does not occur. The AIS detection conforms to the bit error rate requirement stated in Bellcore's TR-TSY-000191 (Issue 1, May 1986), "Alarm Indication Signal Requirements and Objectives."
	4	RXIDL	**Receive DS3 Idle.** When receive DS3 Idle condition is declared, RXIDL is set to 1. A receive DS3 idle condition is declared when all of the following events have occurred during a frame: • Address 00H, bit6, RXOOF = 0 , • The three C-bits (C7, C8 and C9) in subframe 3 are 0, • At least 95 per cent of the payload of each subframe contains a repeating 1100 bit sequence which begins after each overhead bit for a period of one frame, • The latest X-bit received is the sixteenth or higher that has arrived with a 1 value in the most recent nineteen X-bits received Recovery occurs (RXIDL =0) at the end of the first subsequent frame during which not all of the above events occur.
	3	RXLOC	**Receive DS3 Loss of Clock.** A receive DS3 LOC occurs (RXLOC is set to 1) when there are no transitions in the receive clock (D3RC) for seven or more XCK clock cycles. XCK clock must be present to count D3RC cycles. Recovery occurs (RXLOC is reset to 0) on the first transition of D3RC.

Memory Map Description (Continued)

Address	Bit	Symbol	Description
00	2	TXLOC	**Transmit DS3 Loss of Clock.** A transmit DS3 LOS occurs (TXLOC is set to 1) when there are no transitions in the transmit clock (XCK) for seven or more D3RC clock cycles. D3RC clock must be present to count XCK cycles. A failure causes the receive clock (D3RC) to become the transmit clock, and it permits the microprocessor interface and transmitter to continue to function. Recovery occurs (TXLOC is reset to 0) on the first transition of XCK.
	1	XRX2	**Receive X-Bit Number 2.** XRX2 indicates the receive state of X2, and is updated each frame.
	0	XRX1	**Receive X-Bit Number 1.** XRX1 indicates the receive state of X1, and is updated each frame.
01	7	NOFEBE	**FEBE Transmission Disabled.** A one written into this bit disables the transmission of a FEBE when a frame alignment error or C-bit parity error occurs.
	6	TXAIS*	**Transmit DS3 Alarm Indication Signal.** A one written into this bit causes the DS3F to transmit a DS3 AIS. A one must also be written (if not already written) into bit 0 (XTX) in register 01H in order to satisfy the definition of DS3 AIS signal.
	5	ENAIS	**Enable Transmit DS3 Alarm Indication Signal Automatically.** A one written into this bit causes the DS3F to transmit DS3 AIS whenever register 00H, bit 6, RXOOF = 1.
	4	TXIDL*	**Transmit DS3 Idle Signal.** A one written into this bit causes the DS3F to transmit a DS3 idle signal. A one must also be written (if not already written) into bit 0 (XTX) in register 01H in order to satisfy the definition of DS3 idle signal.
	3	MODE	**Operating Mode.** A one enables the DS3F to operate in the M13 mode as specified in Bellcore TR-TSY-000009 and ANSI T1.107-1988. A zero enables the DS3F to operate in the C-bit parity mode that is specified in the ANSI T1.107-1988 and supplement T1.107a-1990. In the M13 operating mode, the transmit C-bit interface is disabled and terminal side C-bits are transmitted as user data.
	2	SER	**Serial Interface Terminal Side.** A one configures the DS3F terminal side to be a serial interface for both receive and transmit. A zero configures the terminal side to be a nibble interface.
	1	3LOOP	**DS3 Transmit-to-Receive Loopback.** A one written into this bit disables the DS3 receive input and causes the transmit DS3 output to be looped back as input. Transmit data is provided at the output (D3TD).
	0	XTX	**Transmit X-Bits.** A one written into this bit causes the DS3F to transmit a one for both X1 and X2. The X-bits may be used to transmit a yellow alarm or as a low-speed signalling channel.

* Note: If both TxAIS and TxIDL are set, TxAIS takes precedence.

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Memory Map Description (Continued)

Address	Bit	Symbol	Description
02	7-0	FBn	**FEBE / Framing Bit Error Performance Counter.** In the C-bit parity mode, this register is used as a FEBE counter. While in the M13 mode, it is used as a framing bit error counter. This is a read-only 8-bit saturating counter that stops at a count of 255 and is automatically cleared to zero when it is read by the microprocessor. If one or more errors are received during the microprocessor read cycle or when the DS3F is updating the counter, one single indication is held and the counter is incremented once after completion of the read or update cycle (i.e., any multiple indications received are recorded as a single increment). When the DS3F is operating in the C-bit parity mode, this counter counts the FEBE indications received. A FEBE indication occurs for a received DS3 frame if any one or more of the three C-bits in the forth subframe (C10, C11, and C12) is zero. When the DS3F is operating in the M13 mode, this counter counts framing bit error indications. An error indication occurs for each F-bit in a received DS3 frame that has a value different from the expected framing pattern. For each such indication, the DS3F also provides a FEBE indication in the transmit line output, unless control bit NOFEBE (register 01H, bit7) is 1. The counter is frozen during a DS3 loss of signal or an out of frame condition.
03	7-0	CPn	**C-Bit Parity Error Performance / Number of Frames Counter.** This register is used as C-bit parity error counter in the C-bit parity mode. While in M13 mode, it counts the number of frames. This is a read-only 8-bit saturating counter that stops at a count of 255 and is automatically cleared to zero when it is read by the microprocessor. If one or more incoming count indications are received during the microprocessor read cycle or when the DS3F is updating the counter, only one single indication is held and the counter is incremented once after completion of the read or update cycle (i.e., any multiple indications received are recorded as a single increment). When the DS3F is operating in the C-bit parity mode, this counter counts C-bit parity error indications. An error indication occurs for each received DS3 frame in which the majority (i.e., two or more) of the CP-bits (C7, C8 and C9) differ from the parity bit which was calculated by the DS3F over all 4704 received payload data bits of the preceding frame. For each such indication, the DS3F also provides a FEBE indication in the transmit line output, unless control bit NOFEBE (register 01H, bit7) is 1. When the DS3F is operating in the M13 mode, this counter counts DS3 frames. It takes approximately 27 milliseconds to count 255 frames. The application's software may use this DS3 frame count in conjunction with the count contained in the framing bit error counter (register 02H) to determine an approximate bit error rate (BER). The counter is frozen during a DS3 loss of signal or an out of frame condition.

Memory Map Description (Continued)

Address	Bit	Symbol	Description
04	7-0	PPn	**P-Bit Parity Error Performance Counter.** This register is used as a P-bit parity error counter. This is a read-only 8-bit saturating counter that stops at a count of 255 and is automatically cleared to zero when it is read by the microprocessor. If one or more errors are received during the microprocessor read cycle or when the DS3F is updating the counter, only one indication is held and the counter is incremented once after completion of the read or update cycle (i.e., any multiple indications received are recorded as a single increment). This counter functions in either C-bit parity or M13 operating mode. An error indication occurs for each received DS3 frame during which one or both of the P1 and P2 bits differ from the parity bit calculated by the DS3F over all 4704 of the received payload data bits of the preceding DS3 frame. The DS3F does not provide a FEBE indication in the transmit line output for each such indication. The counter is frozen during a DS3 loss of signal or an out of frame condition.
05	7	INI	**Initialization Bit.** This bit must be set to one in the initialization stage and should be held as one at any time to ensure normal operation of the DS3F.
	6	START	**Start FEAC Transmission.** When START is set to 1, the DS3F starts to send repetitively the 16-bit FEAC code word, including the X labeled bits from bit 5-0, using the third C-bit (C3). If START is 0, then the third C-bit is always zero and the FEAC channel is disabled. (See also FEAC10 at register 0EH, bit 7.)
	5-0	FEAC Transmit Data	**FEAC Transmit Data.** The third C-bit (C3) is used as a far end alarm and control (FEAC) channel. The FEAC channel uses a 16-bit code word that has the form 0XXXXXX0 11111111 to convey information, where the X labeled bits are the FEAC message taken from bit 5 to bit 0 in this register. Bit 0 corresponds to the right-most bit in the FEAC message.
06	7	FIDL	**FEAC Idle Channel Indication.** This bit is cleared whenever a zero C3 bit is received framing the six-bit variable FEAC word.
	6	NEW	**New Received FEAC Message Indication.** The DS3F sets NEW to 1 when it receives a FEAC message (following a series of 1's) for five consecutive FEAC message intervals (5 x 16 = 80 frames). NEW is reset to 0 when register 06H is read.
	5-0	FEAC Receive Data	**Receive FEAC Message.** The received FEAC code word (via the C3 bit) must be repeated at least five times before it is inserted in bits 5-0. The right-most bit position is located in bit 0.
07	7-0	RXLOS RXOOF RXAIS RXIDL CERR LOC X2ERR X1ERR	**Latched-Bit Register.** Bits 7-4 in this register are the latched values of the corresponding bits in register 00H. All of the bits in this register latch and are cleared on a read cycle, but RXAIS maintains its value when the DS3F is in Transmit-to-Receive loopback or no transmit terminal input is present. Bit 3 (CERR) latches when the DS3F receives a C1 bit equal to zero. Bit 2 (LOC) latches when either an RXLOC (bit 3 - 00H) or an TXLOC (bit 2 - 00H) occurs. The X2ERR and X1ERR bits (bits 1 and 0) are latched at the inverse of the XRX2 and XRX1 values (normally 1), so they are normally 0, thus, a value of 1 here indicates an error in the corresponding received X-bit.

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Memory Map Description (Continued)

Address	Bit	Symbol	Description
08	7	FBEC	**F-Bit Error Counter Control.** When this bit is set to 1, the error counter in register 0AH will count only F-bit errors. When this bit is set to 0, the error counter will count both F-bit and M-bit errors.
	6	MBEC	**M-bit Error Counter Control.** When this bit is set to 0, the error counter in register 0BH will count only M-bit errors. When this bit is set to 1, the error counter will count both M-bit and F-bit errors.
	5	TALL1	**Transmit All Ones.** When this bit is set to 1, the DS3F will transmit unframed all 1's.
	4	OUTDIS	**Output Disable.** When set to 1, this control bit disables all DS3F output pins except the microprocessor interface address/data bus.
	3	ITX2	**Invert Transmit X2.** When set to 1, the X2 bit is inverted from the state specified by the XTX bit (register 01H, bit 0).
	2	ITX1	**Invert Transmit X1.** When set to 1, the X1 bit is inverted from the state specified by the XTX bit (register 01H, bit 0).
	1	RESET	**Reset.** When set to 1, the transmit frame counter is reset. If left set to 1 for longer than one frame, then a register reset occurs, i.e., registers 02H - 04H and 08H - 11H, and bit 6 of register 05H will all be cleared. If this bit is set from 1 back to 0 before a frame has elapsed then no register reset will occur. If this bit is set to 1 when pin $\overline{XFSI}$ is low then a register reset occurs immediately.
	0	LPTIME	**Receive Loop Timing.** When set to 1, this control bit disables the transmit clock input (XCK) and causes the DS3 receive clock (D3RC) to become the DS3 transmit clock. If the DS3 receive clock fails in this mode, the DS3F switches over to the transmit clock (XCK).
09	7	SEF	**Severely Errored Frame Indication.** A one indicates that a Severely Errored Frame condition (SEF) has been detected. An SEF is defined as 3 out of 16 F-bits in error, utilizing a sliding window of 16 bits. This is a latched bit, and it clears on a microprocessor read cycle. This bit will then relatch if the condition that causes this bit to latch is still present.
	6	Unused	Internally set to 0.
	5	RALL1	**Receive ALL One Signal.** When this bit is set to 1, the DS3F has detected unframed all 1's. This is a latched bit, and it clears on a microprocessor read cycle. This bit will then relatch if the condition that causes this bit to latch is still present.
	4-1	Unused	Internally set to 0.
	0	STKOVFL	**Stack Overflow indicator for internal receive FEAC FIFO.** This bit is set to 1 when the receive FEAC circuit has detected and stored in its stack more than four FEAC words since the last read of register OFH. This is a latched bit, and it clears on a microprocessor read cycle.
0A	7-0		**Counter for errored DS3 F-bits (and M-bits).** An 8-bit saturating counter that counts the number of F-bits that are in error since the last read cycle, if control bit FBEC at register 08H, bit 7 is set to 1. If FBEC is set to 0, this counter will count both F-bit and M-bit errors. The counter is cleared on a microprocessor read cycle.

Memory Map Description (Continued)

Address	Bit	Symbol	Description
0B	7-0		**Counter for errored DS3 M-bits (and F-bits).** An 8-bit saturating counter that counts the number of M-bits that are in error since the last read cycle, if control bit MBEC at register 08H, bit 6 is set to 0. If MBEC is set to 1, this counter will count both M-bit and F-bit errors. The counter is cleared on a microprocessor read cycle.
0C	7	RTPLLEN	**Receive-to-Transmit Payload Loopback Lock Enable.** Setting this bit to 1 will reset the transmit frame counter so that the data will be synchronized to the overhead bits when using Receive-to-Transmit Payload Loopback. To activate a RT payload loopback, RTPLLEN must first be set to 1 for at least one frame after RTPLOOP (bit 6) has been set to 1, and then be set to 0. The loopback commences on the transition of RTPLLEN reset to 0 and terminates when RTPLOOP is cleared to 0.
	6	RTPLOOP	**Receive-to-Transmit Payload Loopback.** When set to 1, this control bit activates receive-to-transmit payload loopback. This causes the receive output data (payload only) to be internally connected to the transmit side data input. The loopback condition is terminated by clearing this bit to 0. The $\overline{\text{XFSI}}$ (pin 50) input must be either held high or tri-stated while RTPLOOP is set to 1.
	5	TESTLOCK	**Test Lock.** Test bit to reset the transmit frame counter at a different time with respect to the receive. For test purposes only. Normally set to 0.
	4	M13DLM	**M13 Data Link Mode.** When this control bit is set to 0, the C-Bit Transmit Data Link Clocks (CXDCC and CRDCC) are gapped clocks provided for clocking in the three data link bits (C13, C14, and C15). When set to 1, then the outputs CXDCC and CRDCC become pulses (3 clock cycle wide) that identify the location of the three data link C-bits (the same as in the MT90737 (M13) device). See Figures 15 and 16.
	3	DLCB1	**Data Link C-bits Off.** When set to 1, the C-bits used for the data link (C14, C15 and C16) will be set to 1. When set to 0, the data for these data link C-bits is taken from the input pin CXD.
	2	C2OFF	**C2 Bit Off.** When set to 1, the second C-bit (C2) in the first subframe will be 1. When set to 0, the data for the C2 bit is taken from the input pin CXD.
	1	MCB1	**Most C-bits Off.** When set to 1, the C-bits C4 - C6, and C16 - C21 will all be set to 1. When set to 0, the data for these bits is taken from the input pin CXD.
	0	CPARINV	**Parity and FEBE C-bits Off.** When this control bit is set to 1, the C-bits used for parity (C7, C8, and C9) and the C-bits used for FEBE (C10, C11 and C12) will all be set to the inverse of the state that is calculated for the parity and FEBE. When set to 0, the data for these bits is taken from the calculations for parity and FEBE.

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Memory Map Description (Continued)

Address	Bit	Symbol	Description
0D	7	Unused	This bit is to be set to 0 by the application software.
	6	DFEXEC	**Execute Double FEAC Transmission.** When set to 1, this control bit causes the DS3F to transmit 10 repetitions of the 16-bit FEAC codeword using data from the Double FEAC Transmit Data field in bits 5-0, followed by 10 repetitions of the 16-bit FEAC codeword using data from the FEAC Transmit Data field in register 05H, bits 5-0. This bit is cleared upon completion of the transmission.
	5-0	Double FEAC Transmit Data	**Double FEAC Transmit Data.** The third C-bit (C3) is used as a far end alarm and control (FEAC) channel. The FEAC channel uses a 16-bit code word that has the form 0XXXXXX0 11111111 to convey information, where the X labeled bits are the FEAC message. Bit 0 corresponds to the right-most bit in the FEAC message. When the FEAC channel is used for control purposes, one control (activate or deactivate) codeword is transmitted 10 times first, followed by ten repetitions of the second codeword that identifies the DS3 or DS1 line (or all). This field is used for the X labeled bits of the first codeword of a double word message.
0E	7	FEAC10	**Transmit FEAC Word 10 Times.** When set to 1, the duration of the single FEAC transmission (started by setting to 1 the control bit START in bit 6 of Address 05H) is exactly 10 times. When set to 0, the FEAC transmission initiated at register 05H is continuous.
	6	Unused	This bit is to be set to 0 by the application software.
	5	RGCEN	**Receive Gapped Clock Output Enable.** When set to 1 while the SER (Serial) bit is set to 1, a gapped clock signal (RGCS) is generated by the receive circuitry and sent as output on pin 39.
	4	TGCEN	**Timing Generator Gapped Clock Output Enable.** When set to 1 while the SER (Serial) bit is set to 1, a gapped clock signal (XGCS) is generated by the Timing Generator circuit and sent as output on pin 66.
	3	HINTINV	**Hardware Interrupt Invert.** When set to 1, this control bit inverts the HINT output so that it becomes active low.
	2	HINTEN	**Hardware Interrupt Enable.** When set to 1, this control bit enables the HINT output (pin 15) to generate a hardware interrupt to the microprocessor based on the existence of alarm conditions and the state of the interrupt mask register bits at register 11H.
	1	MOOFW	**M-bit Out Of Frame Window.** When set to 1, this control bit changes from 4 frames to 3 frames the duration of the window for M-bit errors that will cause the Out Of Frame condition to be reported.
	0	CRDCINV	**CRDCC Inversion.** When set to 1 while M13DLM (bit 4 of register 0cH) is set to zero, this control bit advances the timing of CRDCC pulses by one-half of a CRCK cycle (see Figure 16).

Memory Map Description (Continued)

Address	Bit	Symbol	Description
0F	7	MOREFEAC	**MORE Valid FEAC words remain in the stack.** A 1 indicates that there is at least one more valid FEAC word in the receive FEAC stack (bits 5-0).
	6	FEACVLID	**FEAC Word Valid.** A 1 indicates that the FEAC word in the receive FEAC stack (bits 5-0) is valid.
	5-0	RFEAC6 RFEAC1	**Receive FEAC Stack Top.** This field provides access to the top word of a four-word deep push-down FEAC stack (maintained internally) that holds the most recent received FEAC words. If more than four FEAC words have been received since the last read of this register then the STKOVFL bit (register 09H, bit 0) will be set to 1.

5

Memory Map Description (Continued)

Address	Bit	Symbol	Description
10	7	RXLOS	**Receive DS3 Loss Of Signal Interrupt.** RXLOS is used to send a hardware interrupt on the HINT pin (pin 15) if the HINTEN bit is set to 1 and the corresponding mask bit is set to 1 in register 11H. This latched bit is set to 1 when RXLOS is detected. RXLOS is cleared when register 10H is read, but will then relatch if the condition that causes it to latch is still present.
	6	RXOOF	**Receive DS3 Out Of Frame Interrupt.** RXOOF is used to send a hardware interrupt on the HINT pin (pin 15) if the HINTEN bit is set to 1 and the corresponding mask bit is set to 1 in register 11H. This latched bit is set to 1 when RXOOF is detected. RXOOF is cleared when register 10H is read, but will then relatch if the condition that causes it to latch is still present.
	5	RXAIS	**Receive DS3 Alarm Interrupt.** This latched bit is set to 1 when RXAIS is detected. This bit is cleared when Address 10H is read, but will then relatch if the condition that causes it to latch is still present.
	4	RXIDL	**Receive DS3 Idle Interrupt.** RXIDL is used to send a hardware interrupt on the HINT pin (pin 15) if the HINTEN bit is set to 1 and the corresponding mask bit is set to 1 in register 11H. This latched bit is set to 1 when RXIDL is detected. RXIDL is cleared when register 10H is read, but will then relatch if the condition that causes it to latch is still present.
	3	NEWFEAC	**New FEAC Receive Interrupt.** NEWFEAC is used to send a hardware interrupt on the HINT pin (pin 15) if the HINTEN bit is set to 1 and the corresponding mask bit is set to 1 in register 11H. This latched bit is set to 1 when a new FEAC word has been received 5 times consecutively. NEWFEAC is cleared when Address 10H is read, but will then relatch if the condition that causes it to latch is still present.
	2	RTLOC	**Receive or Transmit DS3 Clock Failure Interrupt.** RTLOC is used to send a hardware interrupt on the HINT pin (pin 15) if the HINTEN bit is set to 1 and the corresponding mask bit is set to 1 in register 11H. This latched bit is set to 1 when either RXLOC or TXLOC occurs. RTLOC is cleared when register 10H is read, but will then relatch if the condition that causes it to latch is still present.
	1	SEF	**Severely Errored Frame Indication Interrupt.** SEF is used to send a hardware interrupt on the HINT pin (pin 15) if the HINTEN bit is set to 1 and the corresponding mask bit is set to 1 in register 11H. This latched bit is set to 1 when SEF occurs. SEF is cleared when register 10H is read, but will then relatch if the condition that causes it to latch is still present.
	0	XERR	**Receive X-Bit Error Interrupt.** XERR is used to send a hardware interrupt on the HINT pin (pin 15) if the HINTEN bit is set to 1 and the corresponding mask bit is set to 1 in register 11H. This latched bit is set to 1 when X1 or X2 is 0. XERR is cleared when register 10H is read, but will then relatch if the condition that causes it to latch is still present.

Memory Map Description (Continued)

Address	Bit	Symbol	Description
11	7	RXLOSEN	Alarm Interrupt Enable Mask Bits. If any of the eight bits in this register is set to 1, a hardware interrupt will be generated at the HINT pin (pin 15) when the corresponding latched alarm bit is set to 1 in register 10H, provided that the HINTEN bit at register 0EH, bit 2 is set to 1.
	6	RXOOFEN	
	5	RXAISEN	
	4	RXIDLEN	
	3	NFEACIEN	
	2	RTLOCEN	
	1	SEFEN	
	0	XERREN	
12	7-0	CVEXZ7-CVEXZ0	**Coding Violation/Excessive Zeros Counter, low order byte.** A 16-bit saturating counter (the high order byte is in register 13H) that counts the D3RC cycles for which input on the pin CVCNT (pin 57) is high. It also counts the DS3RC cycles for which input on the pin $\overline{\text{EXZCNT}}$ (pin 55) is low, if the control bit EXZEN (bit 1 of register 14H) is set to 1. To ensure that a correct count is obtained, this low order byte should be read first.
13	7-0	CVEXZ15-CVEXZ8	**Coding Violation/Excessive Zeros Counter, high order byte.** This high order byte should be read after the low order byte (register 12H) is read first to ensure that a correct count is obtained.
14	7	STFREN	**Stuff Receive Enable.** When set to 1, the $\overline{\text{RCG}}$ output of the receive data circuitry will include the stuff bit locations if 2 out of 3 C-bits in that subframe are set to 1, when operating in M13 mode and Serial mode.
	6	STFTGEN	**Stuff Timing Generator Enable.** When set to 1, the $\overline{\text{TCG}}$ output of the timing generator will include the stuff bit locations when operating in M13 mode and Serial mode.
	5	FORCEFEBE	**Force FEBE Error.** When the CVEN bit is set to 1, setting this bit to 1 will generate and transmit a far end block error (FEBE) by setting C10, C11, C12 to 0 in the next available DS3 frame when operating in the C-bit parity mode. To send an additional error, the microprocessor must first set this bit to 0 before again setting it to 1.
	4	FORCEPP	**Force P-Bit Parity Error.** When the CVEN bit is set to 1, setting this bit to 1 will generate and transmit a P-bit error by inverting both P-bits in the next available DS3 frame. To send an additional error, the microprocessor must first set this bit to 0 before again setting it to 1.
	3	FORCECP	**Force C-Bit Parity Error.** When the CVEN bit is set to 1, setting this bit to 1 will generate and transmit a C-bit parity error (C7, C8 and C9 inverted) in the next available DS3 frame when operating in the C-bit parity mode. To send an additional error, the microprocessor must first set this bit to 0 before again setting it to 1.
	2	TSTCNTR	**Test Counter.** This bit should be set to 0.
	1	EXZEN	**Excessive Zeros Enable.** When set to 1, the events on the $\overline{\text{EXZCNT}}$ pin (pin 55) are counted in the CVEXZ counter in register 12H-13H.
	0	CVEN	**Coding Violation Counter Enable.** This bit should be set to 1 to enable the CV counter and force single error functions in this register.

5

Applications

The MT90733 (DS3F) has a number of applications for high speed data transmission at the DS3 rate (44.736Mbit/s) while providing performance monitoring capability and in-band data links. It can be used in the T3 DSU/CSU, routers, DS3 testers as well as other proprietary implementations. In particular, the backbone of today's information superhighway also known as the Internet widely utilizes the DS3 circuits. This undoubtedly opens the door for exploring new applications of the DS3F device.

An example of high speed data transmission using the DS3F is illustrated in Figure 5. On the line side, the DS3F is connected to a Line Interface Unit (LIU) which performs the receive and transmit line interface functions required for transmission of the DS3 signal over coaxial cable. On the terminal side, the DS3F interfaces with a high speed HDLC (High-Level Data Link Control) controller. The HDLC controller provides all the functions, such as flag generation/detection, zero insertion/deletion and FCS (Frame Check Sequnce) calculation, for the packeted data transmission. A FIFO (First In First Out) buffer is used to handle the speed discrepancy between the data transmission and microprocessor read/write cycles. The C-bit I/O circuitry performs the C-bit insertion and reception functions. In the C-bit parity mode, the in-band data link channels are accessed through the C-bit I/O circuitry.

The recommended Line Interface Units (LIU) for the MT90733 are Transwitch's TXC-02021 (ARTE) or TXC-02020 (ART), AT&T's T7295-6 (DS3 Receiver) and T9796 (DS3 Transmitter), and EXAR's XR-T7295 (DS3 Receiver) and XR-T7296 (DS3 Transmitter). Figure 6 shows a simplified diagram of the MT90733 interfacing Transwitch's LIU.

Transporting Asynchronous Transfer Mode (ATM) cells over the PDH (Plesiochronous Digital Hierarchy) networks has been recognized as a cost-effective means to integrate the existing carrier systems into the Broadband-ISDN known as B-ISDN. Mapping of ATM cells into the DS3 payload is defined in ANSI T1.646-1995 and ITU-T Recommendation G.804. Figure 7 depicts an example of ATM over DS3 using MT90733 with Transwitch's Cell Delineation Block (CDB). The CDB maps ATM cells in direct mapping mode into the DS3 payload under the Header Error Control (HEC)-based mapping. The DS3F is connected to the CDB through the nibble-parallel interface.

The power and ground connection of the MT90733 should be carefully planned to ensure the device operates properly at high frequency. Figure 8 shows the recommended power and ground connection method for the DS3F device. Separate planes should be employed for V_{DD} and V_{SS}. Bypass networks consist of a 10 µF capacitor in parallel with 0.1 µF capacitors for each V_{DD} pin, as shown. These 0.1 µF capacitors should be RF-quality and closely connected to each of the device's V_{DD} pins to decouple them to ground.

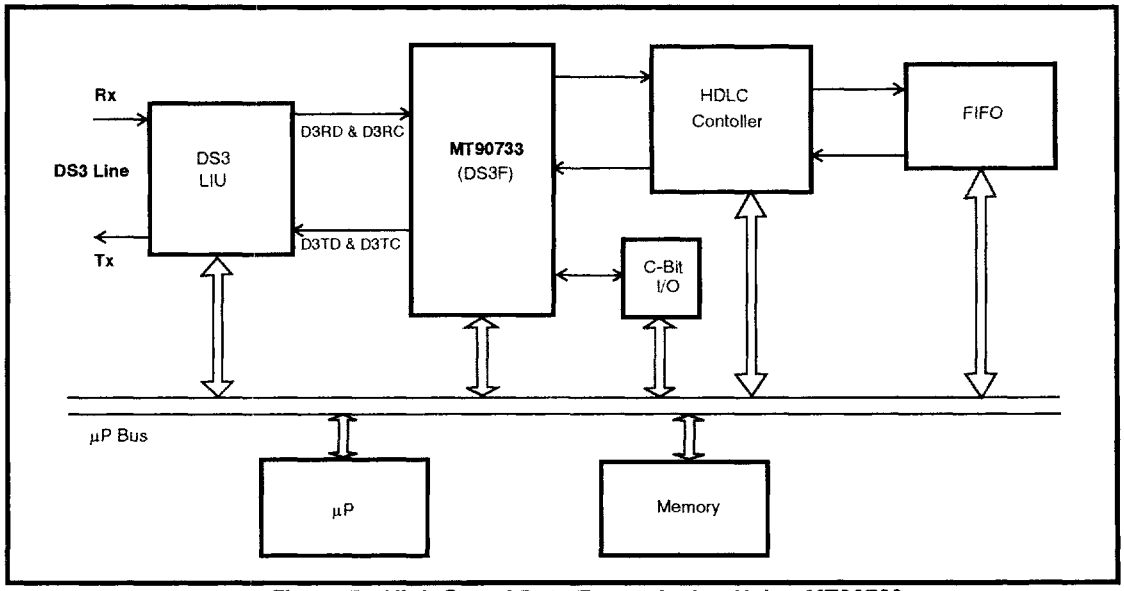

Figure 5 - High Speed Data Transmission Using MT90733

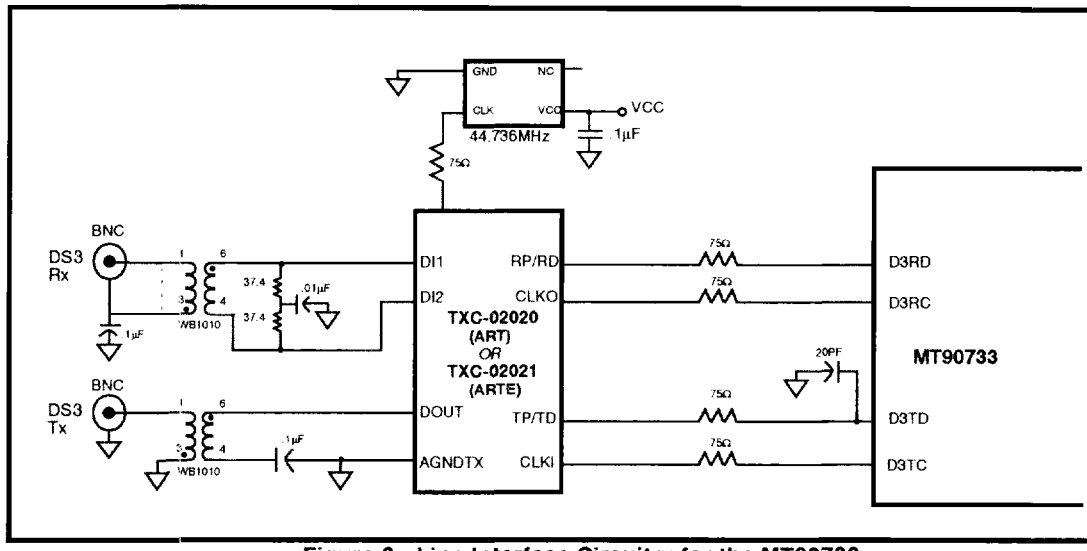

Figure 6 - Line Interface Circuitry for the MT90733

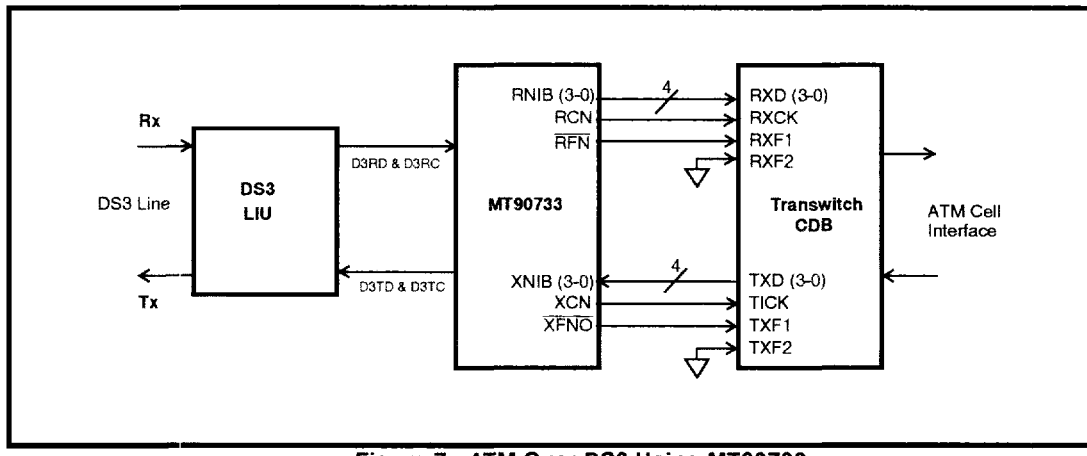

Figure 7 - ATM Over DS3 Using MT90733

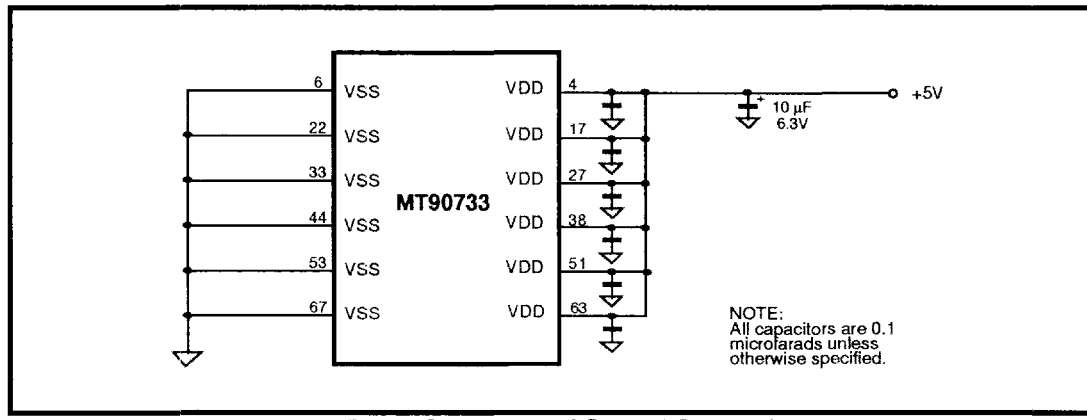

Figure 8 - Power and Ground Connections

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any Input pin	V_{IN}	-0.5	V_{DD} + 0.5	V
3	Continuous power dissipation	P_C		1.0	W
4	Storage Temperature	T_S	-55	150	°C

* Exceeding those values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Supply Current	I_{DD}			150	mA	
3	Operating Temperature	T_{OP}	-40		+85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

DC Electrical Characteristics

Input Parameters for CMOS Type I - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input High Voltage	V_{IH}	3.15			V	$4.75V \leq V_{DD} \leq 5.25V$
2	Input Low Voltage	V_{IL}			1.65	V	$4.75V \leq V_{DD} \leq 5.25V$
3	Input Leakage Current	I_{IL}			10	µA	$V_{DD} = 5.25V$
4	Input Capacitance	C_{IN}		5.5		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

Output Parameters for CMOS Type II - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Output High Voltage	V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75V$; $I_{OH} = -2.0mA$
2	Output Low Voltage	V_{OL}			0.4	V	$V_{DD} = 4.75V$; $I_{OL} = 2.0mA$
3	Output Low Current	I_{OL}			2.0	mA	
4	Output High Current	I_{OH}			-2.0	mA	
5	Rise Time	t_{RISE}		3.1		ns	$C_{LOAD} = 15$ pF
6	Fall Time	t_{FALL}		3.2		ns	$C_{LOAD} = 15$ pF

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

Output Parameters for CMOS Type III - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Output High Voltage	V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75V; I_{OH} = -4.0mA
2	Output Low Voltage	V_{OL}			0.4	V	V_{DD} = 4.75V; I_{OL} = 4.0mA
3	Output Low Current	I_{OL}			4.0	mA	
4	Output High Current	I_{OH}			-4.0	mA	
5	Rise Time	t_{RISE}		1.9		ns	C_{LOAD} = 15 pF
6	Fall Time	t_{FALL}		2.0		ns	C_{LOAD} = 15 pF

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

Input Parameters for TTL Type I - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input High Voltage	V_{IH}	2.0			V	4.75V ≤V_{DD}≤ 5.25V
2	Input Low Voltage	V_{IL}			0.8	V	4.75V ≤V_{DD}≤ 5.25V
3	Input Leakage Current	I_{IL}			10	mA	V_{DD} = 5.25V
4	Input Capacitance	C_{IN}		5.5		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

Input Parameters for TTL Type II - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input High Voltage	V_{IH}	2.0			V	4.75V ≤V_{DD}≤ 5.25V
2	Input Low Voltage	V_{IL}			0.8	V	4.75V ≤V_{DD}≤ 5.25V
3	Input Leakage Current	I_{IL}		0.5	1.4	mA	V_{DD} = 5.25V; Inputs =0V
4	Input Capacitance	C_{IN}		5.5		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
* Note: Input has a 9K (nominal) internal pull-up resistor.

Output Parameters for TTL Type III - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Output High Voltage	V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75V; I_{OH} = -2.0mA
2	Output Low Voltage	V_{OL}			0.4	V	V_{DD} = 4.75V; I_{OL} = 4.0mA
3	Output Low Current	I_{OL}			4.0	mA	
4	Output High Current	I_{OH}			-2.0	mA	
5	Rise Time	t_{RISE}		1.4		ns	C_{LOAD} = 15 pF
6	Fall Time	t_{FALL}		2.7		ns	C_{LOAD} = 15 pF

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
*

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Output Parameters for TTL Type IV - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input High Voltage	V_{IH}	2.0			V	$4.75V \leq V_{DD} \leq 5.25V$
2	Input Low Voltage	V_{IL}			0.8	V	$4.75V \leq V_{DD} \leq 5.25V$
3	Input leakage current	I_{IL}			10	µA	$V_{DD} = 5.25V$
4	Input capacitance	C_{IN}		5.5		pF	
5	Output High Voltage	V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75V$; $I_{OH} = -4.0mA$
6	Output Low Voltage	V_{OL}			0.4	V	$V_{DD} = 4.75V$; $I_{OL} = 8.0mA$
7	Output Low Current	I_{OL}			8.0	mA	
8	Output High Current	I_{OH}			-4.0	mA	
9	Rise Time	t_{RISE}		1.3		ns	$C_{LOAD} = 25$ pF
10	Fall Time	t_{FALL}		2.5		ns	$C_{LOAD} = 25$ pF

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

AC Electrical Characteristics

Detailed timing diagrams for the MT90733 are illustrated in Figures 9 through 20, with values of the timing intervals preceding each figure. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at $(V_{OH} + V_{OL})/2$ or $(V_{IH} + V_{IL})/2$ as applicable.

AC Electrical Characteristics - Line Side DS3 Receive Input Timing (Figure 9)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	D3RC clock period	t_{CYC}	20	22.35		ns	
2	D3RC high time	t_{PWH}	8			ns	
3	D3RC low time	t_{PWL}	8			ns	
4	D3RC duty cycle (t_{PWH}/t_{CYC})	--	40	50	60	%	
5	D3RD set-up time for D3RC↑	t_{SU}	4			ns	
6	D3RD hold time after D3RC↑	t_H	6			ns	

‡ Typical figures are al 25°C and are for design aid only: not guaranteed and not subjected to production testing.

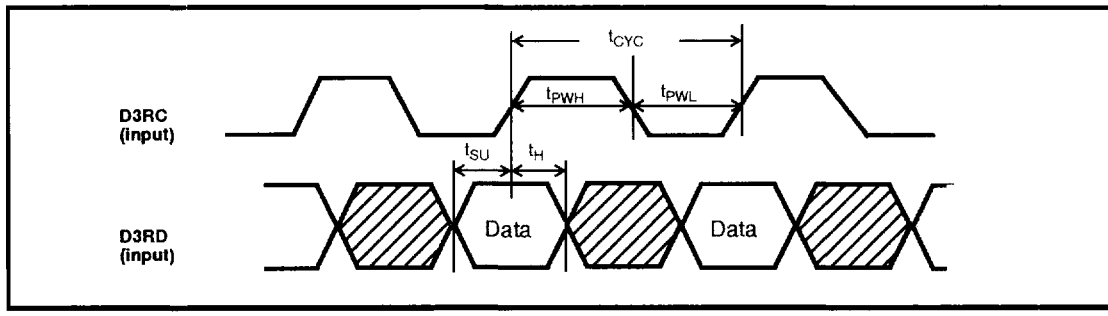

Figure 9 - Line Side DS3 Receive Input Timing

AC Electrical Characteristics - DS3 Transmit Timing (Figure 10)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	D3TC clock period	t_{CYC}	20	22.35		ns	
2	D3TC high time	t_{PWH}	8			ns	
3	D3TC low time	t_{PWH}	8			ns	
3	D3TD output delay after D3TC↑	t_{OD}	2		8	ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

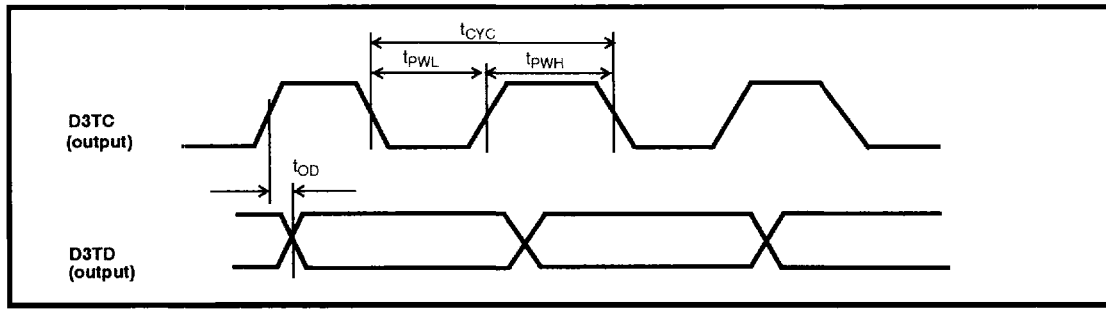

Figure 10 - Line Side DS3 Transmit Output Timing

AC Electrical Characteristics - Terminal Side Receive Nibble Output Timing (Figure 11)

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	RCN clock period	t_{CYC}	89	90.5	111	ns	
2	RCN high time	t_{PWH}	40			ns	
3	RCN low time	t_{PWL}	40			ns	
4	RNIBn delay after RCN↑	$t_{OD(1)}$	20	23	26	ns	
5	$\overline{RFN}$ delay after RCN↑	$t_{OD(2)}$	20	23	26	ns	
6	$\overline{RFN}$ pulse width	t_{PW}	89	1 t_{CYC}	93	ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

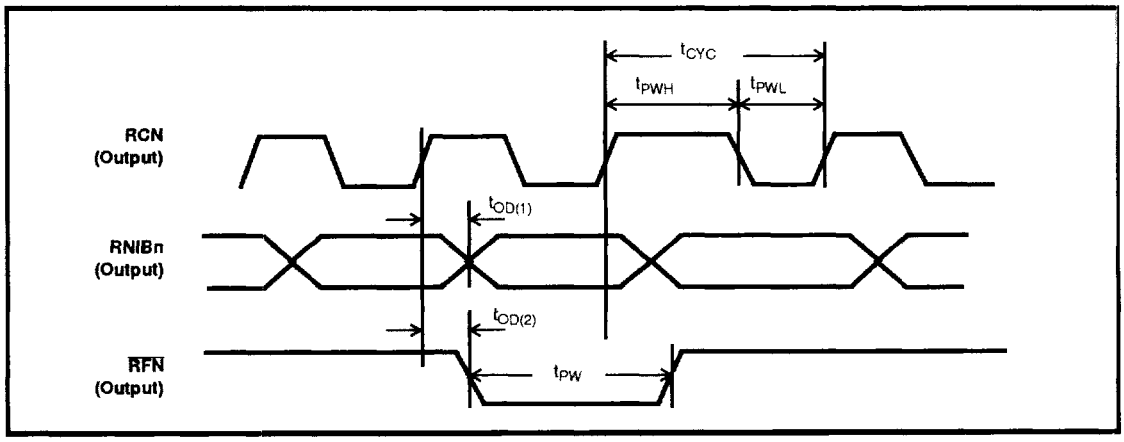

Figure 11 - Terminal Side Receive Nibble Output Timing

AC Electrical Characteristics - Terminal Side Transmit Nibble Input Timing* (Figure 12)

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	XCN clock period	t_{CYC}	89.0	90.5	111	ns	
2	XCN high time	t_{PWH}	40		63	ns	
3	XCN low time	t_{PWL}	40		50	ns	
4	XNIBn set-up time to XCN↑	$t_{SU(1)}$	26			ns	
5	XNIBn hold time after XCN↑	$t_{H(1)}$	-14			ns	
6	$\overline{\text{XNFO}}$ output delay after XCN↑	t_{OD}	8	10	12	ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
* XNIB data input is latched at the midpoint of XCN low.

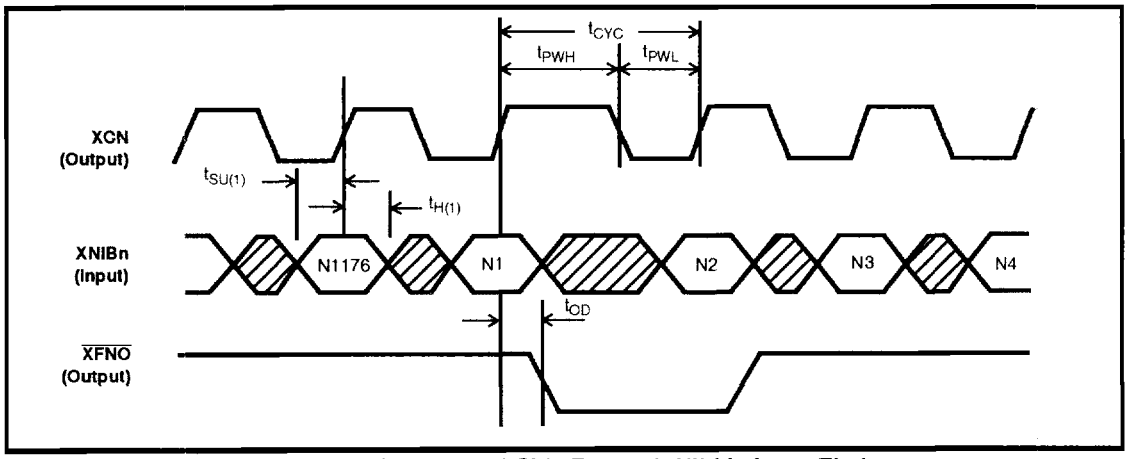

Figure 12 - Terminal Side Transmit Nibble Input Timing

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AC Electrical Characteristics - Terminal Side Receive Serial Output Timing (Figure 13)

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	RCS clock period	t_{CYC}	20	22.35		ns	
2	RCS high time	t_{PWH}	8			ns	
3	RCS low time	t_{PWL}	8			ns	
4	RDS, $\overline{RCG}$, $\overline{RFS}$ output delay after RCS↓	t_{OD}	0	2.5	5	ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

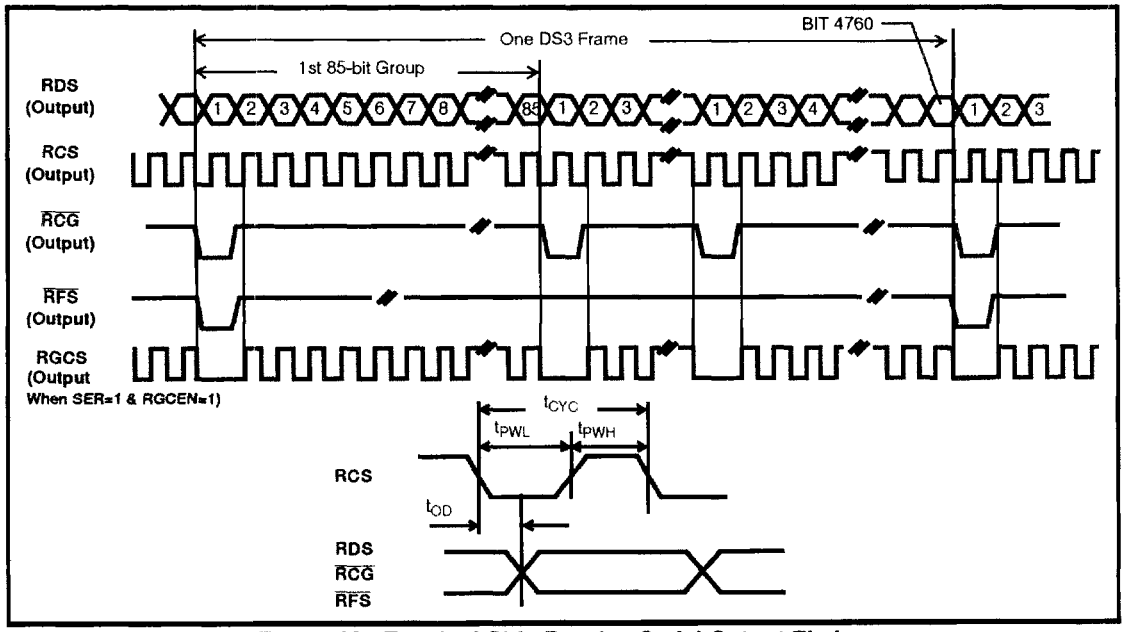

Figure 13 - Terminal Side Receive Serial Output Timing

AC Electrical Characteristics - Terminal Side Transmit Serial Input Timing* (Figure 14)

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	XCK clock period	t_{CYC}	20	22.35		ns	
2	XCK high time	t_{PWH}	8			ns	
3	XCK low time	t_{PWL}	8			ns	
4	XDS, $\overline{XFSI}$ set-up time to XCK↑	t_{SU}	6			ns	
5	XDS, $\overline{XFSI}$ hold time after XCK↑	t_H	4			ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

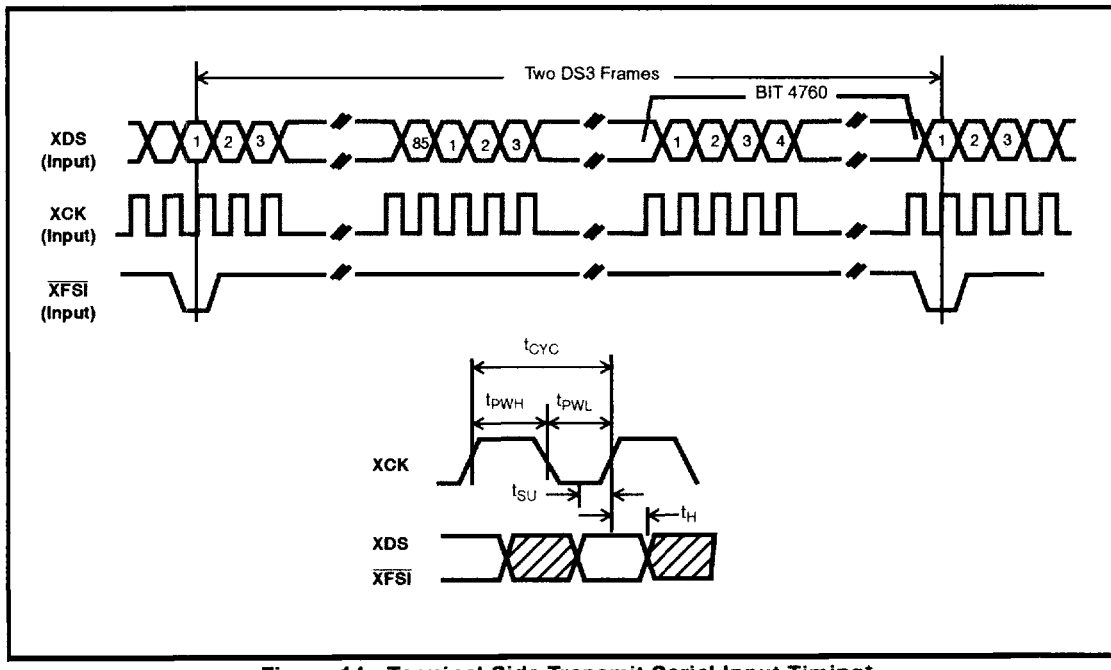

Figure 14 - Terminal Side Transmit Serial Input Timing*

* Note: An additional XGCS is provided by the transmit reference generator (shown in Figure 17) on pin 66 if SER=1 and TGCEN=1.

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AC Electrical Characteristics - C-Bit Transmit Input Timing (Figure 15)

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	CXCK high time	t_{PWH}		85 t_{CYC}		ns	
2	CXD set-up time to CXCK↑	t_{SU}	20			ns	
3	CXD hold time after CXCK↑	t_H	40			ns	
4	CXCK output delay after CXF↑	t_{OD}		170 t_{CYC}		ns	
5	CXF pulse width	t_{PW}		85 t_{CYC}		ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
Note: t_{CYC} is the D3TC clock period (see Figure 10).

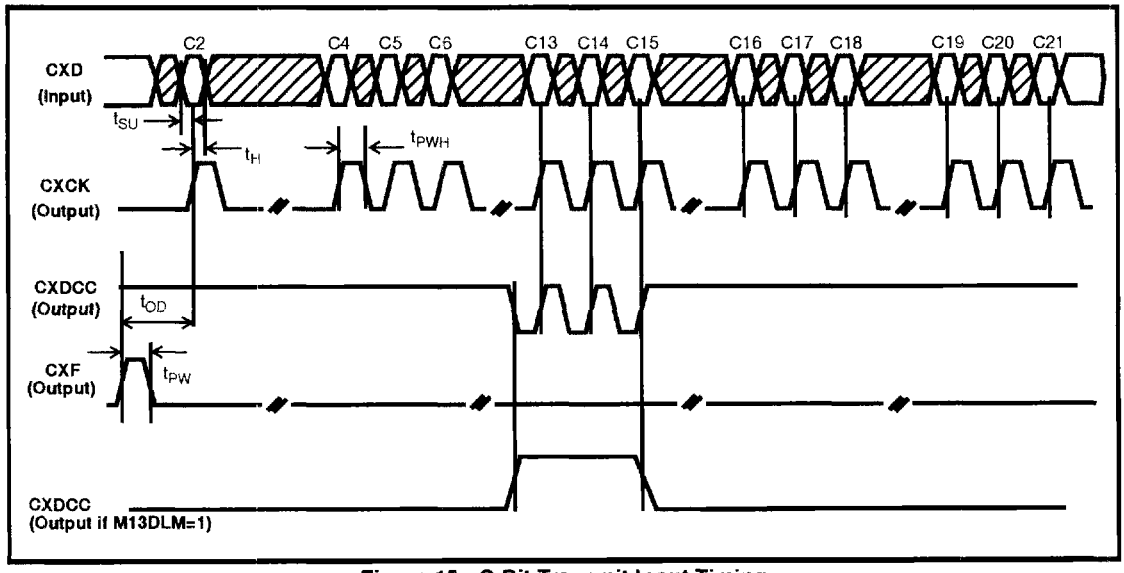

Figure 15 - C-Bit Transmit Input Timing

AC Electrical Characteristics - C-Bit Receive Output Timing (Figure 16)

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	CRCK low time	t_{PWL}		85 t_{CYC}		ns	
2	CRD hold time after CRCK↓	$t_{H(1)}$		85 t_{CYC}		ns	
3	CRCK output delay after CRF↑	$t_{OD(1)}$		170 t_{CYC}		ns	
4	CRF pulse width (high)	t_{PW}		85 t_{CYC}		ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
Note: t_{CYC} is the RCS clock period (see Figure 13).

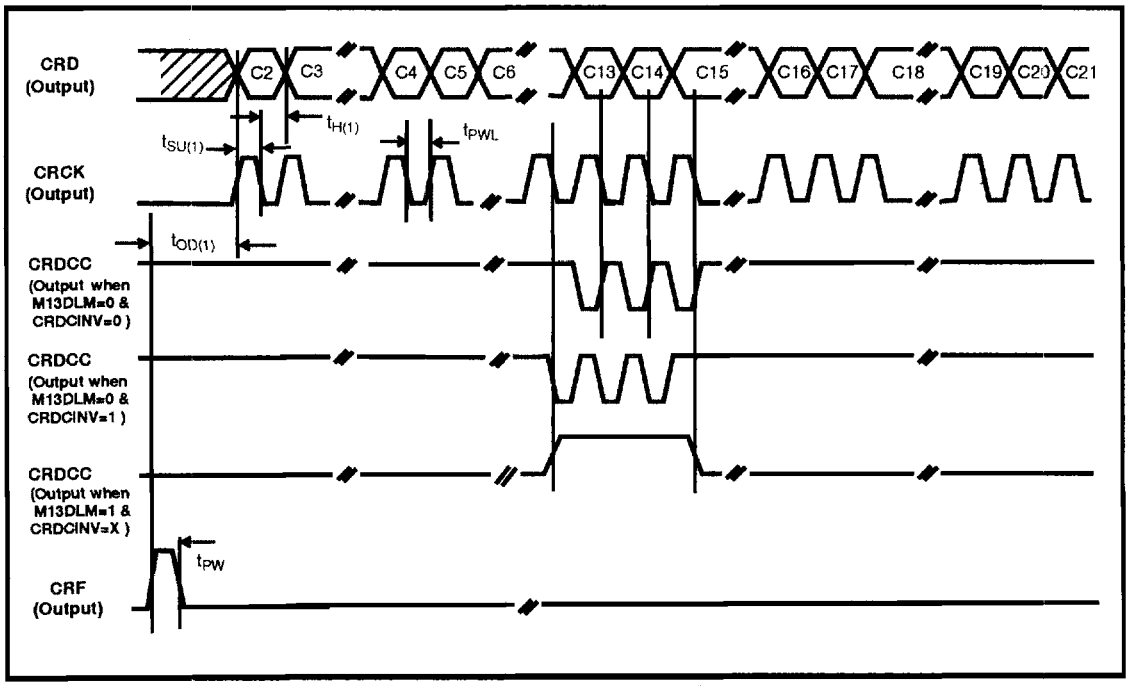

Figure 16 - C-Bit Receive Output Timing

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AC Electrical Characteristics - Transmit Reference Generator Timing (Figure 17)

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	TCIN clock period	$t_{CYC(1)}$	20	22.3		ns	
2	TCIN high time	$t_{PWH(1)}$	10	11.2		ns	
3	TCIN low time	$t_{PWL(1)}$	10	11.2		ns	
4	TCIN duty cycle ($t_{PWH(1)}/t_{CYC(1)}$)	--	40	50	60	%	
5	TCOUT clock period	$t_{CYC(2)}$	$t_{CYC(1)}$	22.3		ns	
6	TCOUT high time	$t_{PWH(2)}$	$t_{PWH(1)}$	11.2		ns	
7	TCOUT output delay after TCIN↓	$t_{OD(1)}$	2	4		ns	
8	TDOUT output delay after TCOUT↑	$t_{OD(2)}$	2	4	7	ns	
9	$\overline{TFOUT}$ output delay after TCOUT↑	$t_{OD(3)}$	2	4	7	ns	
10	$\overline{TCG}$ output delay after TCOUT↑	$t_{OD(4)}$	2	4	7	ns	
11	XGCS output delay after TCIN↓	$t_{OD(5)}$	2	4		ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.

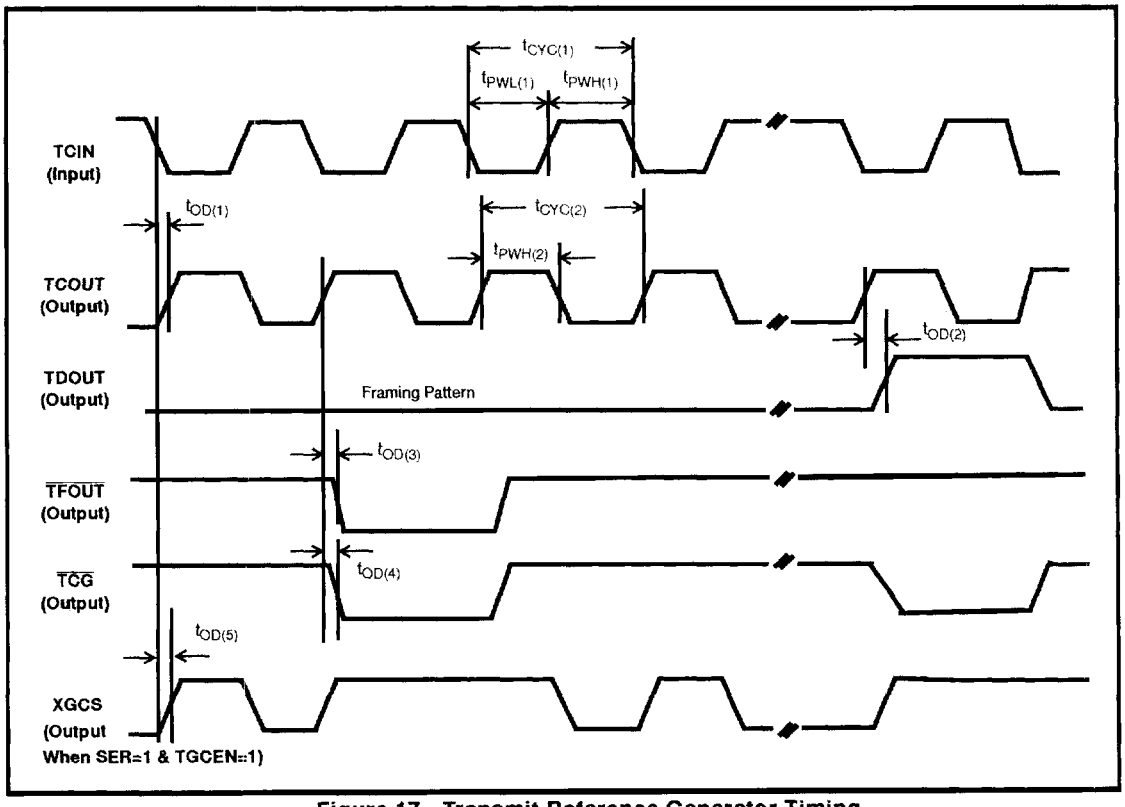

Figure 17 - Transmit Reference Generator Timing

AC Electrical Characteristics - Force Overhead Bit Error Timing (FORCEOE) (Figure 18)

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	D3TC clock period	t_{CYC}	20	22.35		ns	
2	OENA output delay after D3TC↑	t_{OD}	10			ns	
3	OENA pulse width (high)	$t_{PW(1)}$	9 t_{CYC}		80 t_{CYC}	ns	
4	$\overline{\text{FORCEOE}}$ pulse width (low)	$t_{PW(2)}$	9 t_{CYC}		45 t_{CYC}	ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
Note: $\overline{\text{FORCEOE}}$↑ resets OENA.

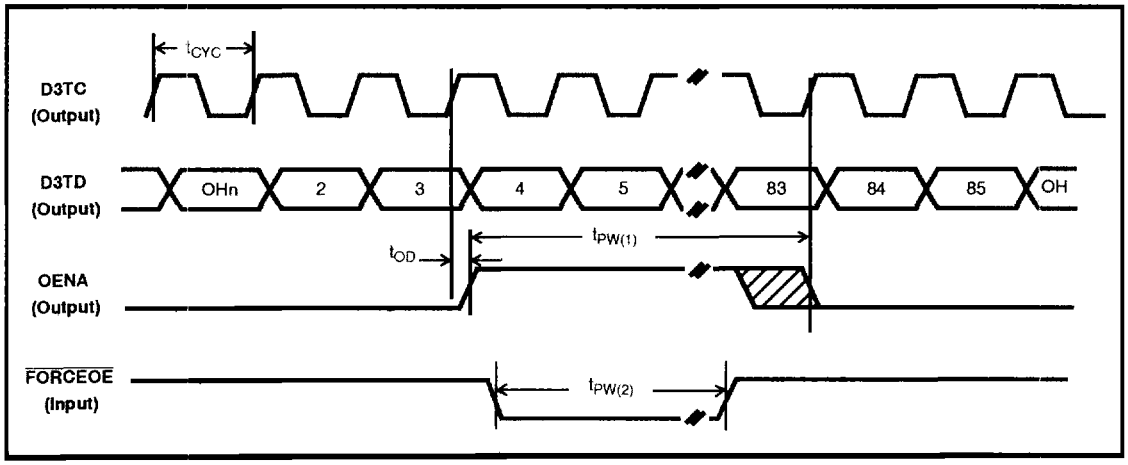

Figure 18 - Force Overhead Bit Error Timing (FORCEOE)

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AC Electrical Characteristics - Microprocessor Read Cycle Timing (Figure 19)

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ALE pulse width	$t_{PW(1)}$	30			ns	
2	ALE wait after $\overline{RD}$ ↑	$t_{W(1)}$	0			ns	
3	Address set-up time to ALE ↓	$t_{SU(1)}$	20			ns	
4	Address hold time after ALE ↓	$t_{H(1)}$	10			ns	
5	Address hold time after $\overline{RD}$ ↓	$t_{H(2)}$			50	ns	
6	Data output delay (to tristate) after $\overline{RD}$ ↑	$t_{OD(1)}$	10		20	ns	
7	Data output delay after $\overline{RD}$ ↓	$t_{OD(2)}$			80	ns	
8	$\overline{SEL}$ wait after ALE↓	$t_{W(2)}$			40	ns	
9	$\overline{SEL}$ wait after $\overline{RD}$ ↑	$t_{W(3)}$	40			ns	
10	$\overline{RD}$ pulse width	$t_{PW(2)}$	100			ns	
11	$\overline{RD}$ wait after ALE ↓	$t_{W(4)}$	50			ns	

‡ *Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.*

Notes:

1. The transmit clock (XCK) or receive clock (D3RC) must be present for the microprocessor bus interface to operate.
2. A minimum of 10 clock cycles must occur after power-up, before the read cycles are valid.

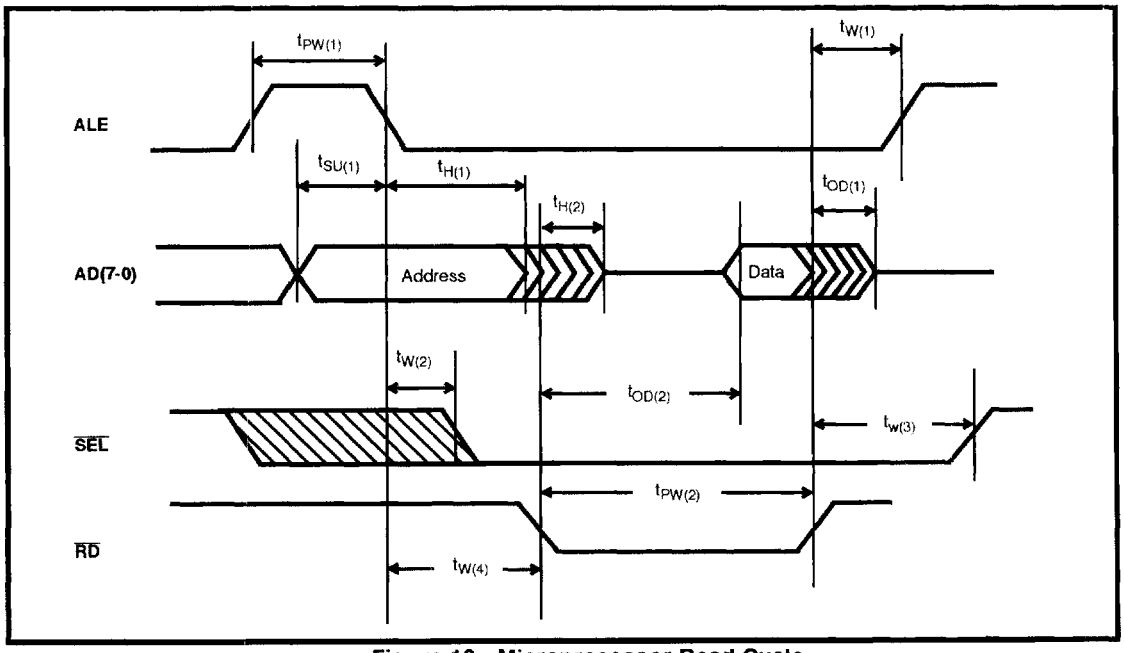

Figure 19 - Microprocessor Read Cycle

AC Electrical Characteristics - Microprocessor Write Cycle Timing (Figure 20)

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ALE pulse width	$t_{PW(1)}$	50			ns	
2	ALE wait after $\overline{WR}$ ↑	$t_{W(1)}$	0			ns	
3	Address set-up time to ALE ↓	$t_{SU(1)}$	30			ns	
4	Address hold time after ALE ↓	$t_{H(1)}$	10			ns	
5	Data hold time after $\overline{WR}$ ↑	$t_{H(2)}$	20			ns	
6	$\overline{SEL}$ wait after ALE↓	$t_{W(2)}$			40	ns	
7	$\overline{SEL}$ wait after $\overline{WR}$↑	$t_{W(3)}$	40			ns	
8	$\overline{WR}$ pulse width	$t_{PW(2)}$	50			ns	
9	$\overline{WR}$ wait after ALE ↓	$t_{W(4)}$	50			ns	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subjected to production testing.
Notes:
1. The transmit clock (XCK) or receive clock (D3RC) must be present for the microprocessor bus interface to operate.
2. A minimum of 10 clock cycles must occur after power-up, before the write cycles are valid.

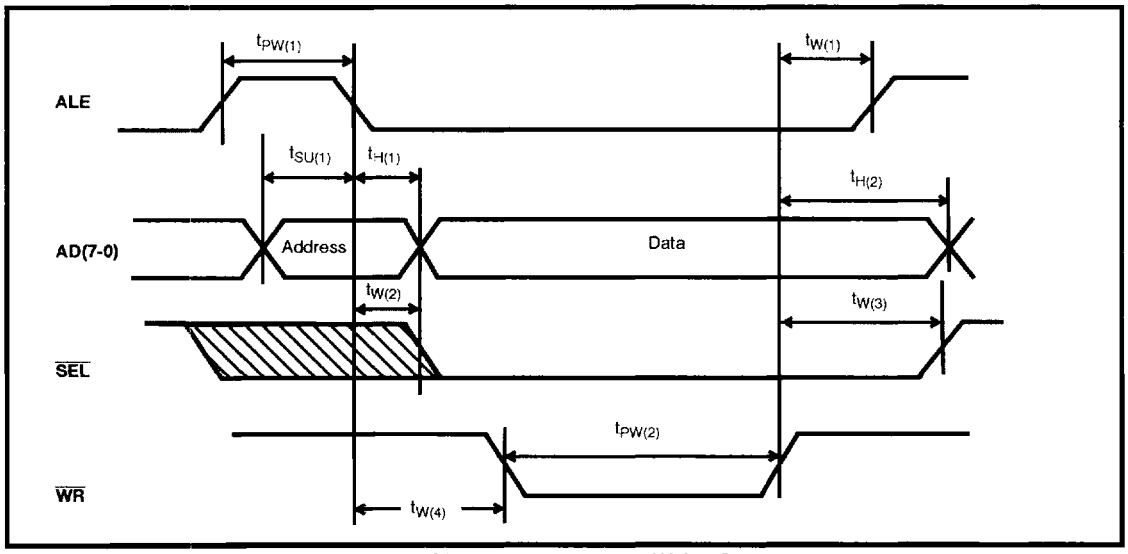

Figure 20 - Microprocessor Write Cycle

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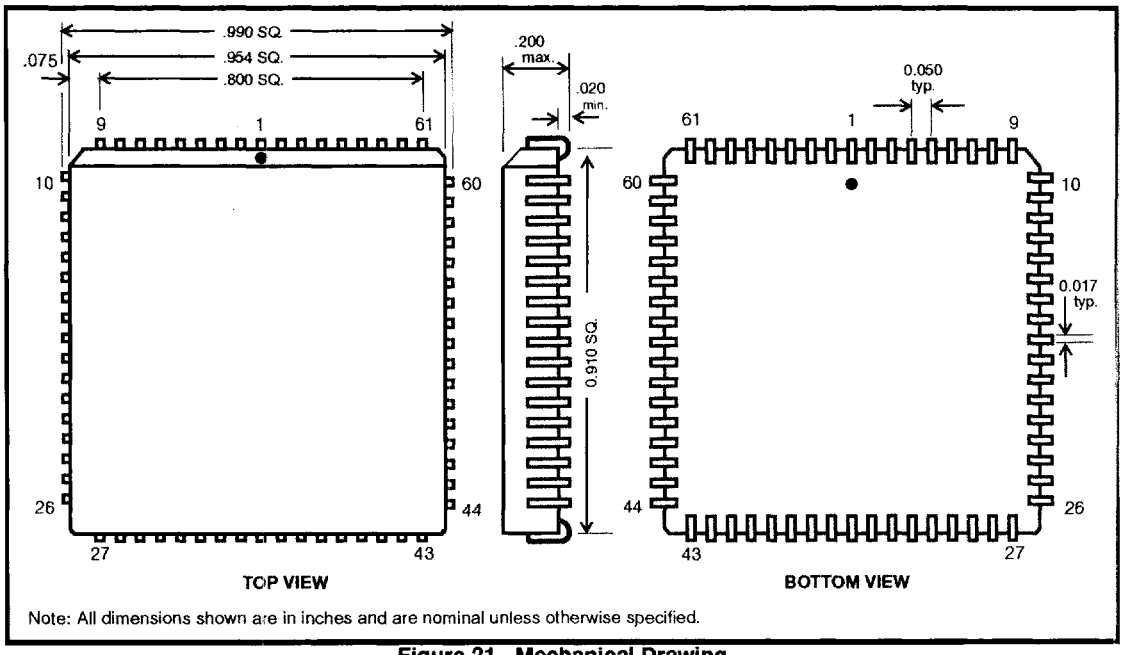

Note: All dimensions shown are in inches and are nominal unless otherwise specified.

Figure 21 - Mechanical Drawing