010058

Am8284/8285

Binary Hexadecimal/BCD Decade Synchronous Up-Down Counters

Description: The Am8284 Binary Hexadecimal and the Am8285 BCD Decade Synchronous Up/Down Counters are functionally, electrically, and pin-for-pin an equivalent to the Signetics 8284 and 8285. They are available in the hermetic dual-in-line package.

Distinctive Characteristics: 100% reliability assurance testing including high temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL STD 883.

Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am8284 and Am8285 Up/Down Counters consist of four "T" (trigger) flip flops driven synchronously by a buffered clock pulse (CP) input. The flip flop outputs Q_1, Q_2, Q_3, Q_4 and $\overline{Q}_4$ are available.

The outputs change states synchronously on the falling edge of the CP input. Count direction is controlled by a single Up/Down (U/D) input. Count Enable (CE) input, when LOW, inhibits the count mode. Carry In (CI) input, when LOW, inhibits the count mode and forces the Carry Out (CO) output to a LOW state.

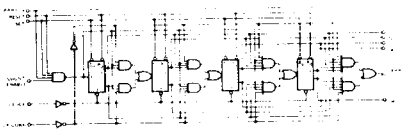
The Am8284 output is in the 8-4-2-1 weighted binary code of 0 through 15. The Am8285 output is in the 8-4-2-1 BCD code of 0 through 9. A HIGH terminal count output, Carry Out (CO), is available when the following conditions are satisfied:

$$CO_{8284} = (CI) \cdot (Q_1Q_2Q_3Q_4UP + \overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{Q}_4\overline{UP})$$
$$CO_{8285} = (CI) \cdot (Q_1\overline{Q}_2\overline{Q}_3Q_4UP + \overline{Q}_1Q_2Q_3\overline{Q}_4\overline{UP})$$

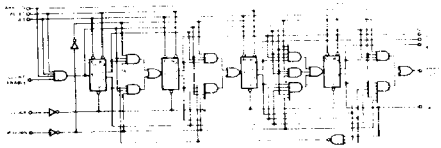
The Set Input LOW sets the Am8284 and Am8285 asynchronously to their respective maximum counts of fifteen (15) and nine (9). Reset Input LOW sets both counters asynchronously to minimum count zero (0). Truth Table I describes the asynchronous and synchronous operating modes for both counters.

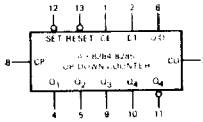
LOGIC DIAGRAMS/SYMBOL

Am8284



Am8285





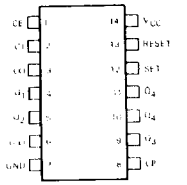
V_{CC} = PIN 8
GND = PIN 7

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
N8284	Hermetic DIP	0°C to +76°C	N8284A
S8284	Hermetic DIP	−55°C to +125°C	S8284A
8284	Dice	Note 10	X8284D
N8285	Hermetic DIP	0°C to +75°C	N8285A
S8285	Hermetic DIP	−55°C to +125°C	S8285A
8285	Dice	Note 10	X8285D

Note 10: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATIN (bove which the useful life may be impaired)

Storage and Junction T ature	−65°C to +175°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} m
DC Input Voltage	−0.5 V to +6.0
Output Current, Into Outputs	100 n
DC Input Current (Note 1)	±30 n

ELECTRICAL CHARACTERISTICS

N8284/N8285 T_A = 0°C to +75°C
S8284/S8285 T_A = −55°C to +125°C

DC Characteristics (Notes 2, 3, 4)

Parameters	Part No.	Test Conditions	LIMITS −55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Units
V_{OH}("1") Output HIGH Voltage	All	V_{CC} = 5.0 V, I_{OH} = 20xI_R = −0.5 mA					2.8							
	S8284 S8285	V_{CCL} = 4.75 V, I_{OH} = 20xI_R = −0.5 mA (Refer to Notes 6 and 9)	2.6					3.0				2.6		Volts
	N8284 N8285				2.6			3.0		2.6				
V_{OL}("0") Output LOW Voltage	All	V_{CC} = 5.0 V, I_{OL} = 6xI_F = 9.6 mA							0.4					
	S8284 S8285	V_{CCL} = 4.75 V, I_{OL} = 6xI_F = 9.6 mA (Refer to Note 6)	0.4					0.2				0.4		Volts
	N8284 N8285					0.4		0.2			0.4			
V_{IH}("1") Input HIGH Voltage	S8284 S8285	V_{CCH} = 5.25 V, V_{CCL} = 4.75 V	2.0				2.0					2.0		Volts
	N8284 N8285				2.0		2.0			2.0				
V_{IL}("0") Input LOW Voltage	S8284 S8285	V_{CCH} = 5.25 V, V_{CCL} = 4.75 V		0.8					0.8				0.8	Volts
	N8284 N8285					0.8			0.8				0.8	
I_F("0") Input Load Current (CE,CP,U/D)	S8284 S8285	V_{CCH} = 5.25 V, V_F = 0.4 V		−1.6					−1.6				−1.6	mA
	N8284 N8285					−1.6			−1.6		−1.6			
I_F("0") Input Load Current (CI)	S8284 S8285	V_{CCH} = 5.25 V, V_I = 0.4 V		−3.2					−3.2				−3.2	mA
	N8284 N8285					−3.2					−3.2			
I_F("0") Input Load Current (SET, RESET)	S8284 S8285	V_{CCH} = 5.25 V, V_F = 0.4 V		−6.4					−6.4				−6.4	mA
	N8284 N8285					−6.4					−6.4			
I_R("1") Reverse Input Current (CE,CP,U/D)	S8284 S8285	V_{CCH} = 5.25 V, V_R = 4.5 V		25					25				25	nA
	N8284 N8285					25			25		25			
I_R("1") Reverse Input Current (CI)	S8284 S8285	V_{CCH} = 5.25 V, V_R = 4.5 V		75					75				75	nA
	N8284 N8285					75			75		75			
I_R("1") Reverse Input Current (SET, RESET)	S8284 S8285	V_{CCH} = 5.25 V, V_R = 4.5 V		125					125				125	nA
	N8284 N8285					125			125				125	
LV_{IN} Input Latch Voltage	S8284 S8285 N8284 N8285	V_{CC} = 5.0 V, I_{IN} = 10 mA (Refer to Note 8)					6.0							Volts
I_{SC} Output Short Circuit Current	S8284 S8285 N8284 N8285	V_{CC} = 5.0 V					−20		−70					mA
P_D Power Dissipation	S8284 S8285 N8284 N8285	V_{CCH} = 5.25 V						270	360					mW

Note 1. Maximum current defined by DC Input Voltage.
2. Pulse tested.
3. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
4. All measurements are taken with ground pin tied to zero volts.
5. Output source current is supplied through a resistor to ground.
6. Output sink current is supplied through a resistor to Vcc.
7. One DC fan-out is defined as 0.8 mA.
8. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
9. To set Q_3 and Q_2 HIGH on the 8285, connect Q_1 to CE, momentarily ground SET, and count down. The counter will stop at BCD-7 (0111).

Switc. , Characteristics	Test Conditions	+25 °C Min	Typ	Max	Units
t_{OFF} (Clock to Out)	V_{CC} = 5.0 V		20		nA
t_{ON} (Clock to Out)	Refer to Figure 1		20		nA
t_{OFF} (Set/Reset to Out)	V_{CC} = 5.0 V		15		nA
t_{ON} (Set/Reset to Out)	Refer to Figure 2		15		nA
t_{OFF} (CI to CO)	V_{CC} = 5.0 V		15		nA
t_{ON} (CI to CO)	Refer to Figure 3		15		nA
Count Frequency	V_{CC} = 5.0 V	20	30		MHz
Clock Min "1" Interval		20	15		ns
Set-Up Time CI, CE, U/D	V_{CC} = 5.0 V		15	25	ns
CI, CE, U/D Release Time	V_{CC} = 5.0 V		0		ns
Set/Reset Hold Time	V_{CC} = 5.0 V		20		ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

F Forward, applying to LOW inputs.

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to a LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

R Reverse, applying to HIGH inputs.

FUNCTIONAL TERMS:

Asynchronous Inputs Outputs (flip flops) change state on command from these inputs independent of the clock pulse.

CE Count Enable LOW inhibits the counter. Outputs Q_1, Q_2, Q_3, Q_4 and Q_4 remain unchanged.

CI Carry in LOW inhibits the counter and forces Carry Out (CO) to LOW. Outputs Q_1, Q_2, Q_3, Q_4 and $\overline{Q}_4$ remain unchanged.

CO Carry Out output is HIGH whenever Carry In (CI) is HIGH and the counter is either in the "Up" count mode and at maximum count (9 for 8285; 15 for 8284) or in the "Down" count mode and at minimum count of zero.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Hold Time The minimum time required for the logic level to be present in order for the outputs to respond.

Input Unit Load In the HIGH state it is equal to I_R and in the LOW state it is equal one half I_F.

Maximum Count The highest number the counter can attain (9 for 8285 and 15 for 8284).

Minimum Count The lowest number the counter can attaain (zero for both counters).

Q_1, Q_2, Q_3, Q_4 Outputs The four TRUE outputs.

$\overline{Q}_4$ Output The FALSE output of the most significant bit.

Reset Input A LOW on this input causes the counter to reset asynchronously to zero. Simultaneous Set and Reset LOW is an undefined condition.

Rd Asynchronous direct Reset Input. A LOW on this input causes output Q to go LOW.

Sd Asynchronous direct Set Input. A LOW on this input causes output Q to go HIGH.

Synchronous Counter All outputs (flip flops) change state on command from the clock.

T (trigger) Flop Flop The flip flop output changes state on the clock pulse when the T Input is HIGH. The output remains unchanged when the T input is LOW.

Set Input A low on this input causes the counter to preset asynchronously to maximum count (9 for 8285 and 15 for 8284). Simultaneous Set and Reset LOW is an undefined condition.

U/D (Up/Down) Input This input controls the count direction. A HIGH for up count and a LOW for down count.

OPERATIONAL TERMS:

I_F("0") Forward input load current for unit input load.

Input Latch Voltage The breakdown voltage of an input with other inputs of the same input transistor grounded.

I_{OH} Output HIGH current forced out of output in V_{OH} test.

I_{OL} Output LOW current forced into the output in V_{OL} test.

I_R("1") Reverse input load current with V_R applied to input.

Negative Current Current flowing out of the device.

Output Short Circuit Current The amount of current a HIGH output can source when shorted to ground.

Positive Current Current flowing into the device.

Power Dissipation The product of the worst case supply current and the maximum supply voltage.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH}("1") Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL}("0") Maximum logic LOW output voltage with output LOW current I_{OL} into output.

V_F Forward LOW input voltage, for forward input current (I_F) test.

V_R Input reverse HIGH voltage applied for input leakage current (I_R) test.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

Clock Min "1" Interval The minimum clock pulse width required for proper counter operation.

Count Frequency The maximum clock input frequency allowed for proper counter operation.

Release Time The maximum time allowed for the logic level to be present at the input prior to the clock transition from HIGH to LOW in order for the counter not to respond.

Set Up Time Minimum time required for the logic level to be present at the input prior to the clock transition from HIGH to LOW in order for the counter to respond.

t_{OFF} (Clock to Out) The propagation delay from the clock signal HIGH-LOW transition to an output LOW-HIGH transition.

t_{ON} (Clock to Out) The propagation delay from the clock signal HIGH-LOW transition to an output HIGH-LOW transition.

t_{OFF} (Set/Reset to Out) The propagation delay from the Set or Reset signal HIGH-LOW transition to the output signal LOW-HIGH transition.

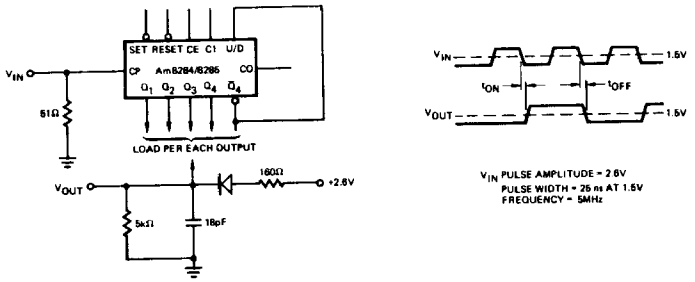
t_{ON} (Set/Reset to Out) The propagation delay from the Set or Reset signal HIGH-LOW transition to the output signal HIGH-LOW transition.

t_{OFF} (CI to CO) The propagation delay from the Carry In signal LOW-HIGH transition to the Carry Out signal transition.

t_{ON} (CI to CO) The propagation delay from the Carry In signal HIGH-LOW transition to the Carry Out signal HIGH-LOW transition.

SWITCHING TIME TEST CIRCUITS/WAVEFORMS

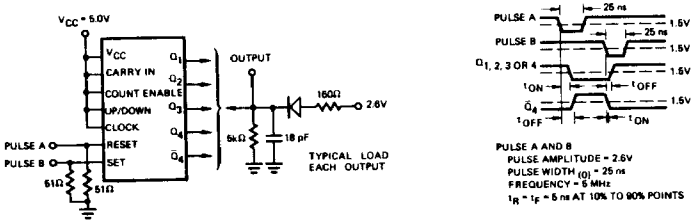
Clock Q Outputs Propagation Delay (t_{ON} and t_{OFF})



V_{IN} PULSE AMPLITUDE = 2.6V
PULSE WIDTH = 25 ns AT 1.5V
FREQUENCY = 5MHz

Figure 1

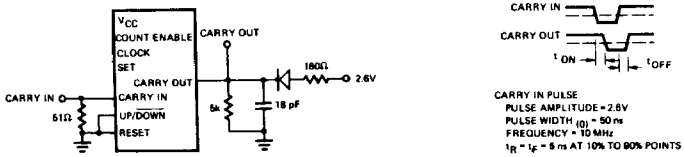
Set/Reset Mode (t_{ON} and t_{OFF})



PULSE A AND B
PULSE AMPLITUDE = 2.6V
PULSE WIDTH (Q) = 25 ns
FREQUENCY = 5 MHz
$t_R = t_F$ = 5 ns AT 10% TO 90% POINTS

Figure 2

Carry In/Carry Out (t_{ON} and t_{OFF})



CARRY IN PULSE
PULSE AMPLITUDE = 2.6V
PULSE WIDTH (Q) = 50 ns
FREQUENCY = 10 MHz
$t_R = t_F$ = 5 ns AT 10% TO 90% POINTS

Figure 3

TRUTH TABLES

Asynchronous	Input Set	Input Reset	Output Q_1	Output Q_2	Output Q_3	Output Q_4
Am8284/8285	1	0	0	0	0	0
Am8284 only	0	1	1	1	1	1
Am8285 only	0	1	1	0	0	1

TABLE I

Synchronous	Input Set	Reset	CI	CE	U/D	Output Function
Am8284/8285	1	1	0	X	X	No Change
Am8284/8285	1	1	X	0	X	No Change
Am8284/8285	1	1	1	1	0	Count Down
Am8284/8285	1	1	1	1	1	Count Up

X = Don't Care

TABLE II

Am8284/85 LOADING RULES

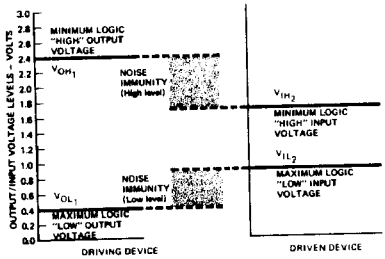
Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
CE	1	2	1	—	—
CI	2	4	3	—	—
CO	3	—	—	20	12
Q_1	4	—	—	20	12
Q_2	5	—	—	20	12
U/D	6	2	1	—	—
GND	7	—	—	—	—
CP	8	2	1	—	—
Q_3	9	—	—	20	12
Q_4	10	—	—	20	12
Q_5	11	—	—	20	12
Set	12	8	5	—	—
Reset	13	8	5	—	—
V_{CC}	14	—	—	—	—

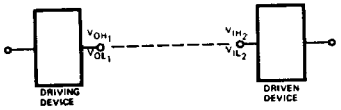
MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices Series 9300	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

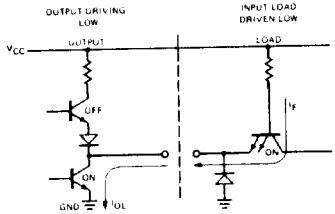
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH

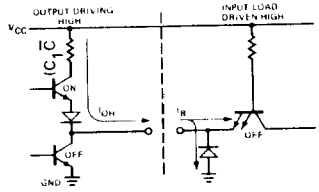




Current Interface Conditions — LOW

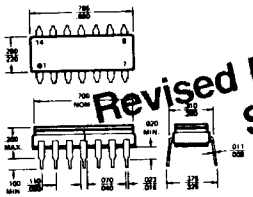


Current Interface Conditions — HIGH

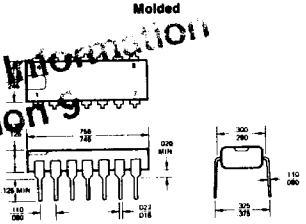


PHYSICAL DIMENSIONS
Dual-In-Line

Hermetic

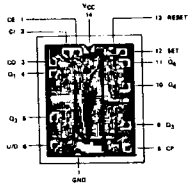


Molded



Metallization and Pad Layout

85 x 107 Mils



ADVAN
MI
DEVICES
901 Thompson I
Sunn
California 9
(408) 732-
TWX: 910-339-
TELEX: 34-