OKI Semiconductor

FEDL81221GD-01
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ML81221GD

High Isolation DPDT RF Switch

GENERAL DESCRIPTION

The ML81221GD is a DPDT (Double-Pole Double-Throw) MOSFET RF (Radio Frequency) switch IC. This switch is designed to cover a broad range of applications from DC through 2GHz, and integrates on-chip CMOS control logic with a low voltage CMOS compatible control interface. This switch can be used in antenna diversity systems, such as FM/TV tuners and wireless receiver systems.

The ML81221GD MOSFET RF switch IC is manufactured in UTSi® CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

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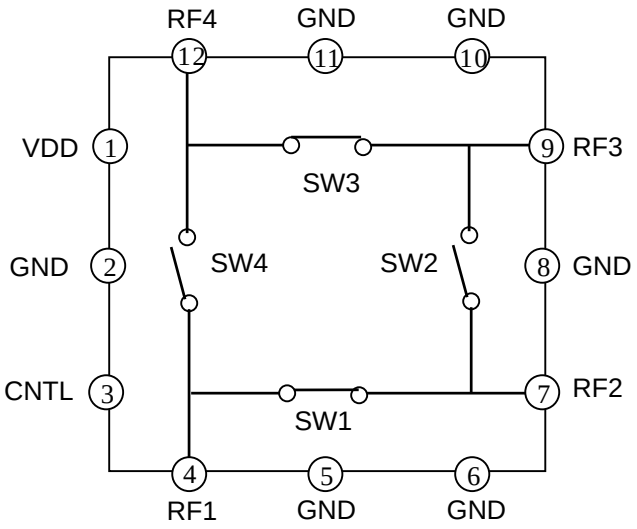
FEATURES

- High isolation: >30dB at 900MHz. >22dB at 1.9GHz.
- Low insertion loss: 0.5dB at 900MHz, 0.8dB at 1.9GHz.
- Single-pin CMOS logic control input.
- Low voltage operation: 2.7V (min.)
- Low power consumption: 15µA (typ.).
- No blocking capacitors required for all RF ports.
- Lead (Pb) free small package: Lead (Pb) free 12-pin plastic WQFN (P-WQFN12-0303-0.50-63).

BLOCK DIAGRAM AND PIN CONFIGURATION (TOP VIEW)



TRUTH TABLE

CTRL (Pin 3)	Signal Path	SW1	SW2	SW3	SW4
High	RF2 to RF3, RF4 to RF1	Off	On	Off	On
Low	RF1 to RF2, RF3 to RF4	On	Off	On	Off

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VDD	Power supply
2	GND	Groud
3	CTRL	Switch control signal input
4	RF1	RF port 1
5	GND	Ground
6	GND	Ground
7	RF2	RF port 2
8	GND	Groud
9	RF3	RF port 3
10	GND	Ground
11	GND	Ground
12	RF4	RF port 4

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 to +4.0	V
Control Voltage	V_{CTL}	Ta = 25°C	−0.3 to V_{DD} + 0.3	V
Input Power	P_{IN}	Ta = 25°C, Z_S = Z_L =50ohm	< 17	dBm
Power Dissipation	P_D	Ta = 25°C, Z_S = Z_L =50ohm	0.2	W
Operating Temperature	T_{OP}	—	−40 to +85	°C
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=−40 to +85°C)

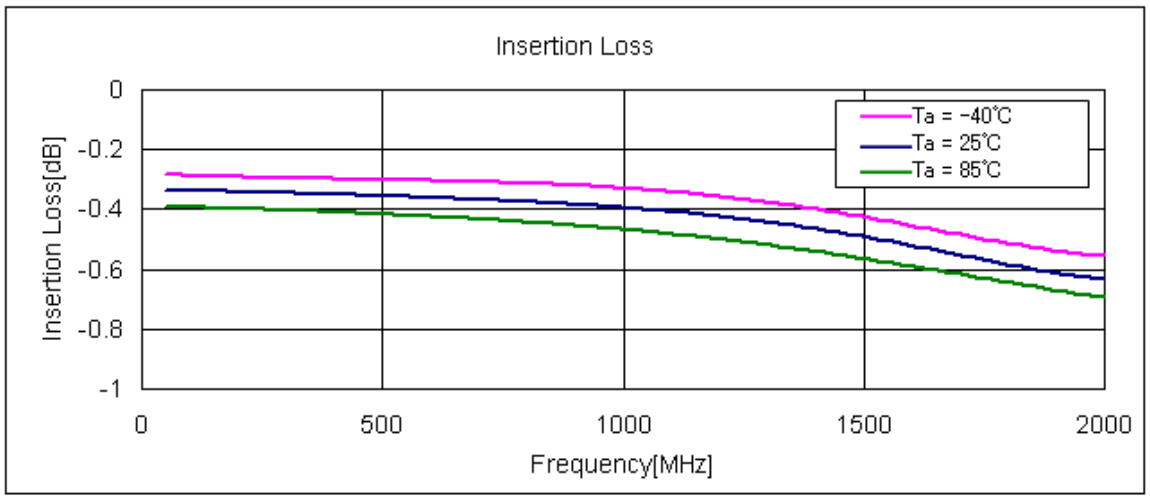
Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	GND = 0 V	2.7 to 3.3	V
Input Power	P_{IN}	Z_S = Z_L = 50ohm	< 15	dBm
Control Voltage High	V_{CTL} (H)	—	0.8 x V_{DD} to V_{DD}	V
Control Voltage Low	V_{CTL} (L)	—	0 to 0.2 x V_{DD}	V
Switching Period	T_{SWP}	—	< 50	Hz

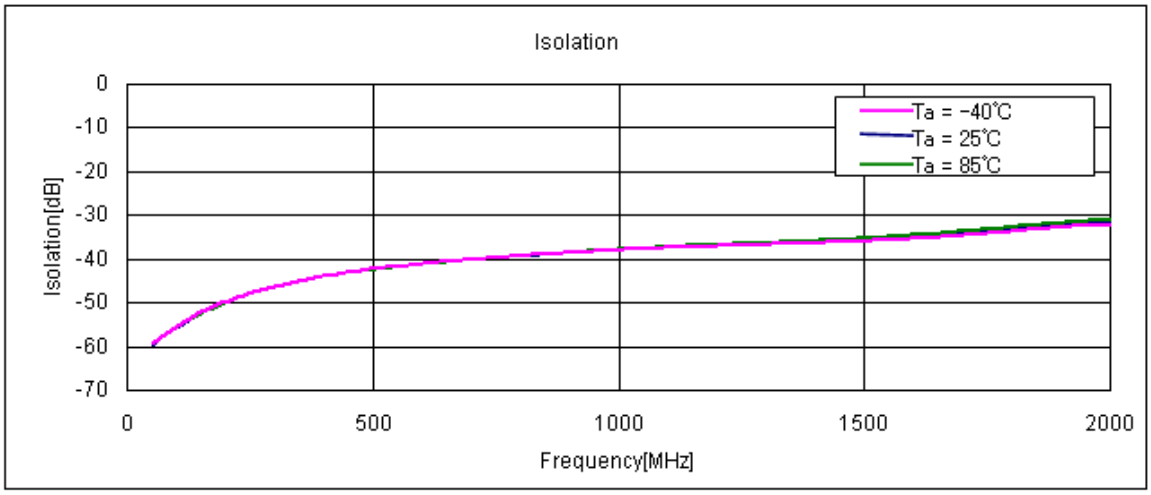
ELECTRICAL CHARACTERISTICS

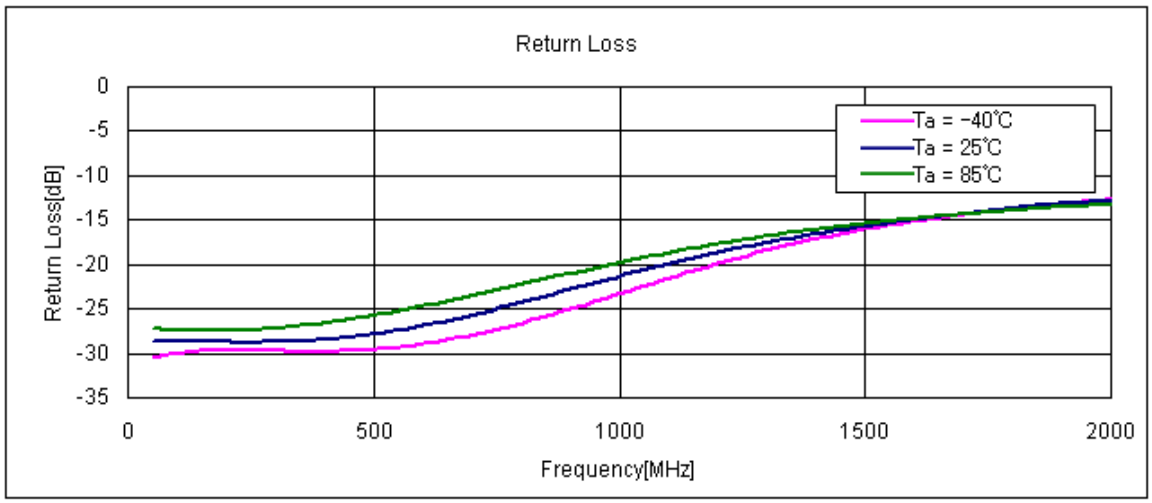
(Ta=25°C, V_{DD}=V_{CTL} (H)=3V, V_{CTL} (L)=0V, Z_S=Z_L=50Ω)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Insertion Loss	I_L	P_{IN}=0dBm, 900MHz		0.5		dB
		P_{IN}=0dBm, 1900MHz		0.8		dB
Isolation	I_{SO}	P_{IN}=0dBm, 900MHz	30	39		dB
		P_{IN}=0dBm, 1900MHz	22	32		dB
Return Loss	R_L	P_{IN}=0dBm, 900MHz		22		dB
		P_{IN}=0dBm, 1900MHz		12		dB
2nd Harmonic	$2f_0$	P_{IN}=5dBm, 900MHz		−80		dBc
		P_{IN}=5dBm, 1900MHz		−80		dBc
3rd Harmonic	$3f_0$	P_{IN}=5dBm, 900MHz		−80		dBc
		P_{IN}=5dBm, 1900MHz		−80		dBc
3rd Order Intermodulation Intercept	IIP3	P_{IN}=10dBm, 900MHz, 1MHz spacing		45		dBm
		P_{IN}=10dBm, 1900MHz, 1MHz spacing		45		dBm
1dB Compression Input Power	P1dB	900MHz	15			dBm
		1900MHz	15			dBm
Switching Time	T_{sw}	OFF to ON: 0% control to 90% RF, ON to OFF: 0% control to 10% RF, 900MHz/19000MHz		1.5		μsec
Power Supply Current	I_{DD}	P_{IN}=5dBm, 900MHz/1900MHz		15	30	μA
ESD Tolerance	—	HBM		1.5		kV

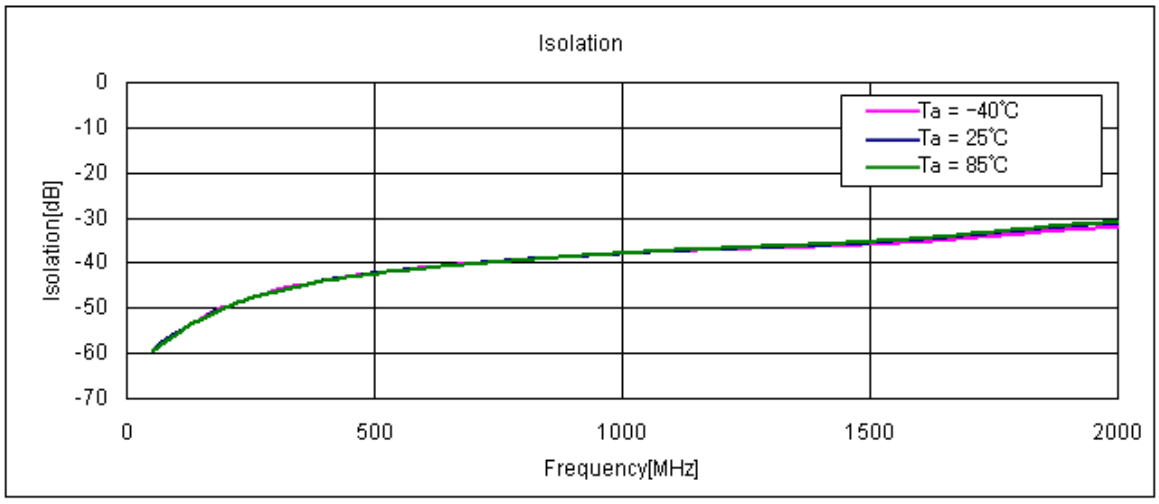
TYPICAL PERFORMANCE DATA @ V_{DD} = 2.7V, Ta = – 40 / 25 / 85 °C

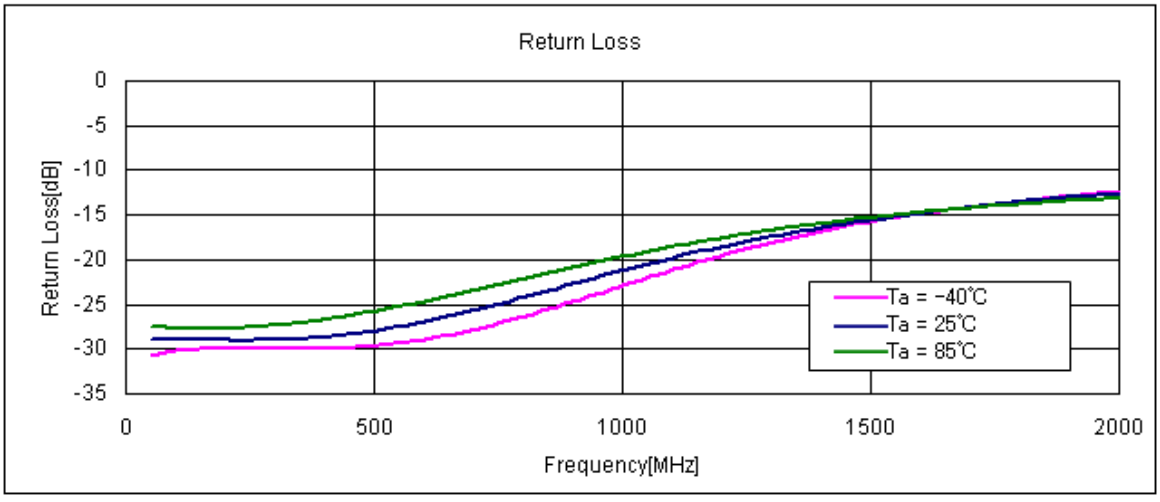




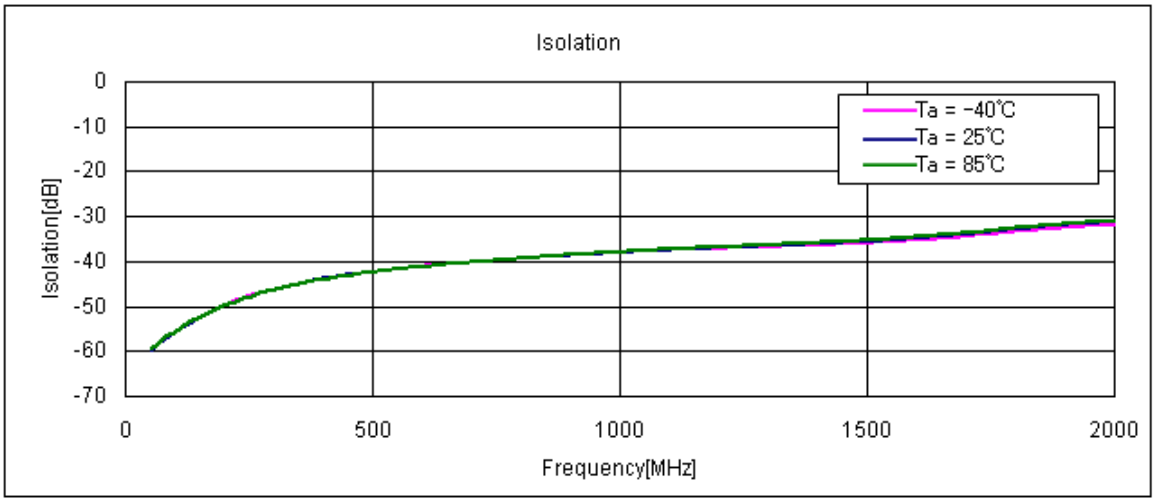


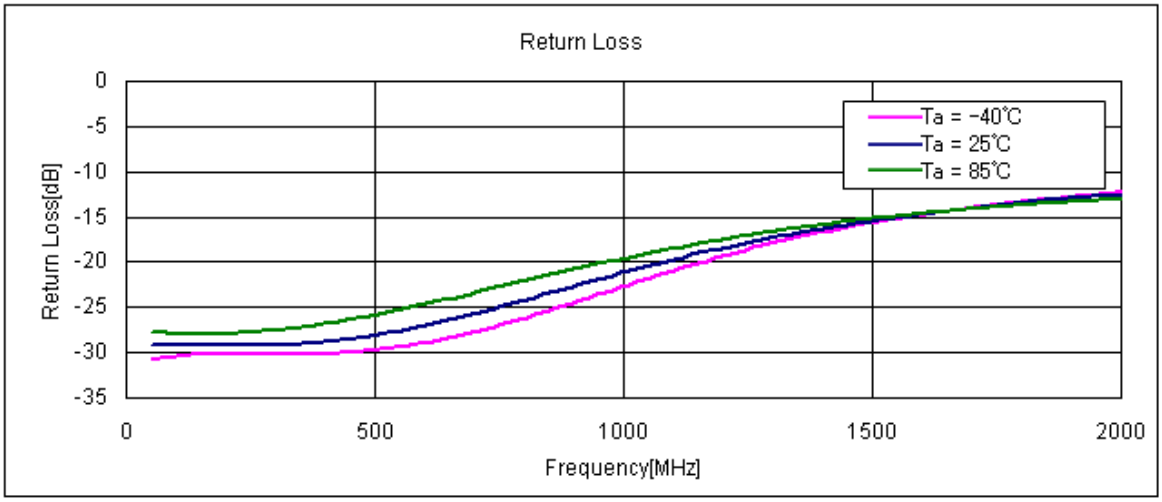
TYPICAL PERFORMANCE DATA @ V_{DD} = 3.0V, Ta = – 40 / 25 / 85 °C



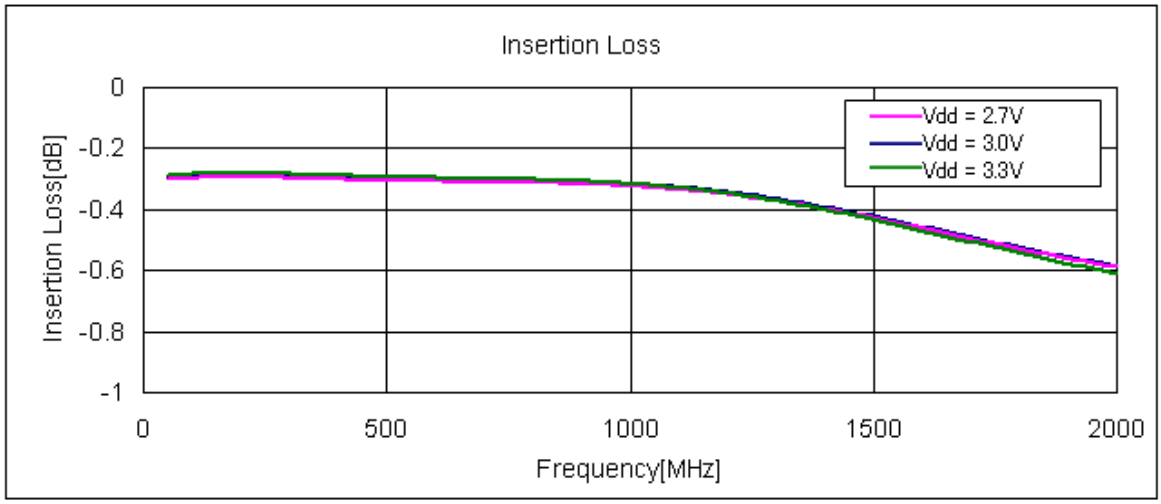


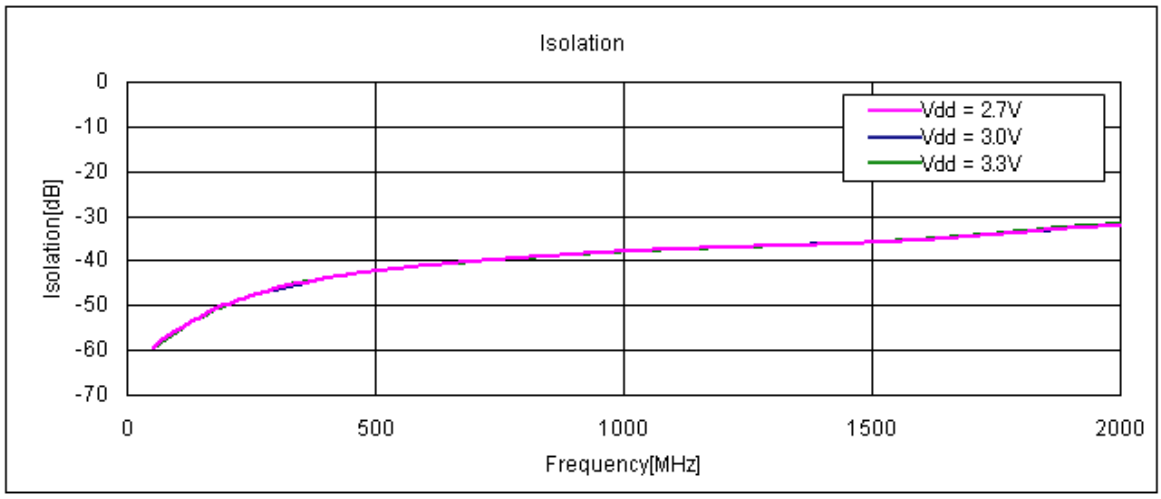
TYPICAL PERFORMANCE DATA @ V_{DD} = 3.3V, Ta= – 40 / 25 / 85 °C

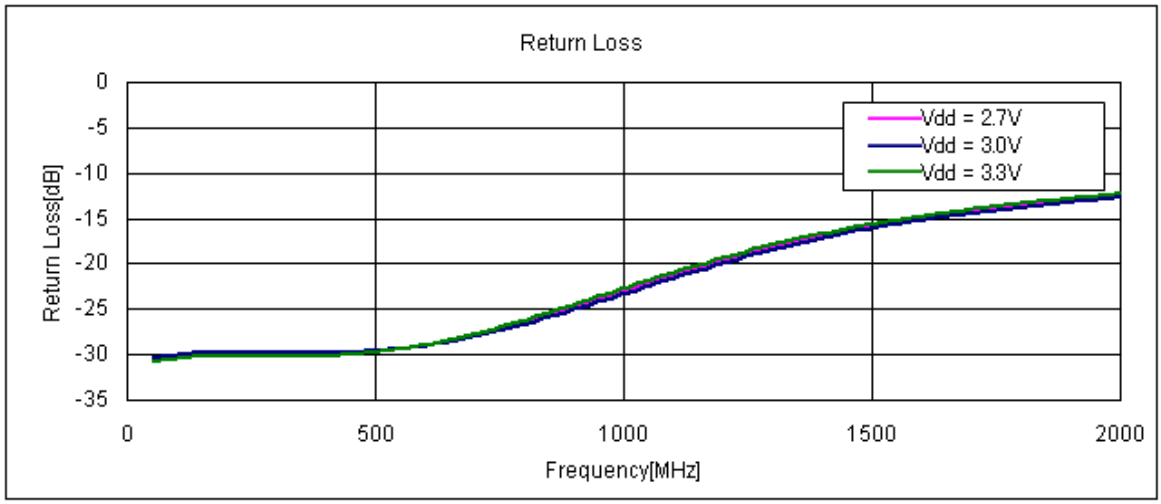




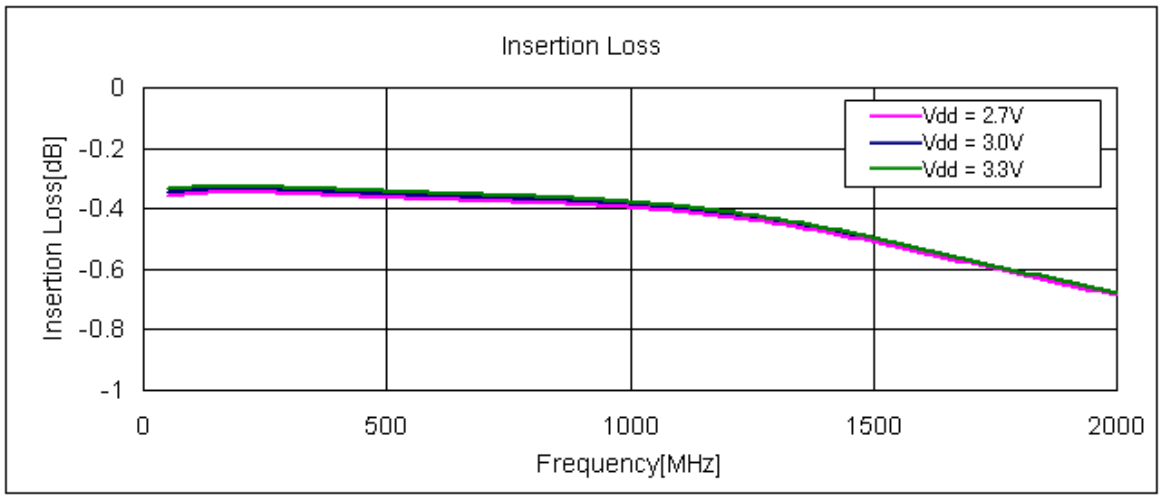
TYPICAL PERFORMANCE DATA @ V_{DD} = 2.7 / 3 / 3.3V, Ta= – 40°C

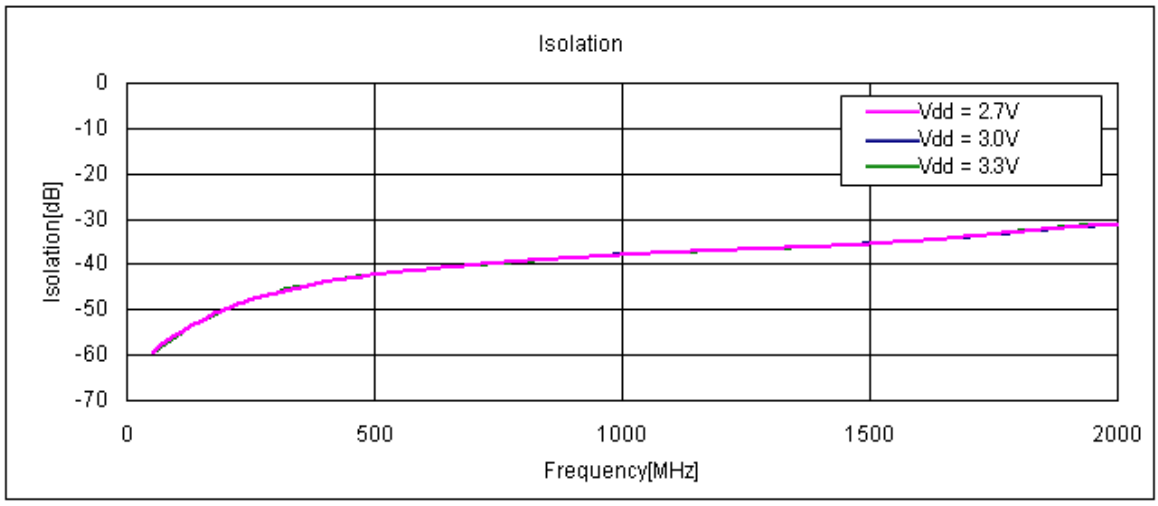


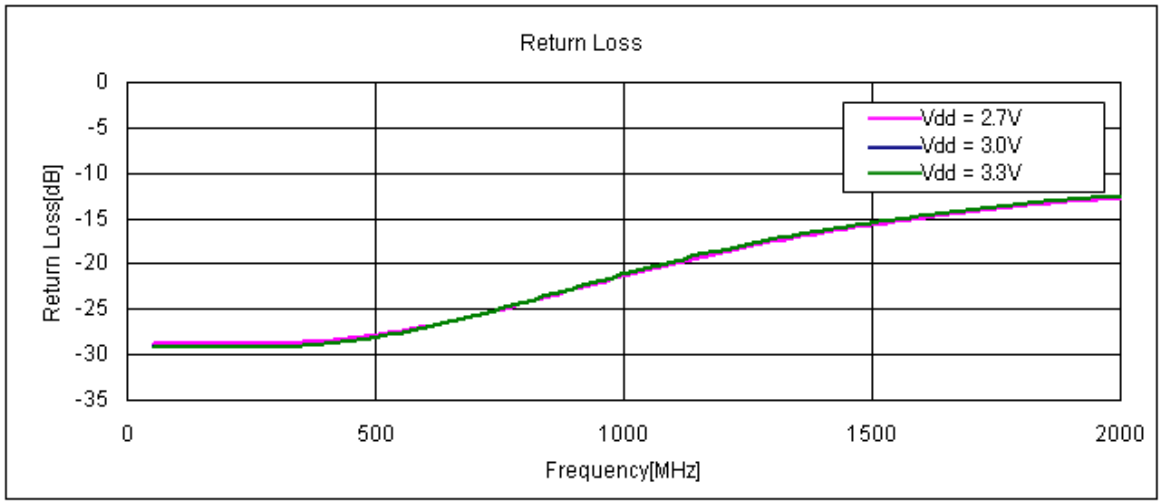




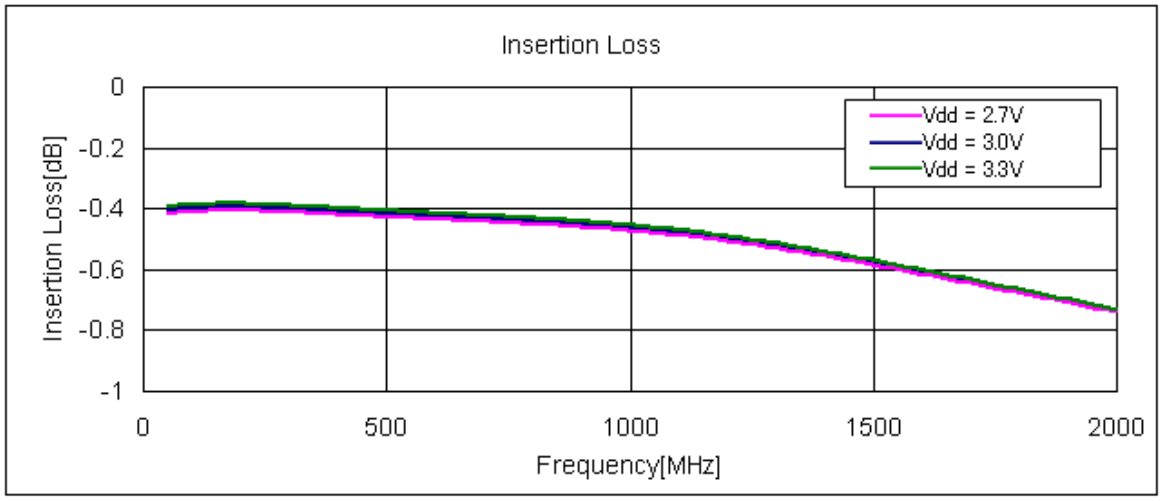
TYPICAL PERFORMANCE DATA @ V_{DD} = 2.7 / 3 / 3.3V, Ta = 25°C

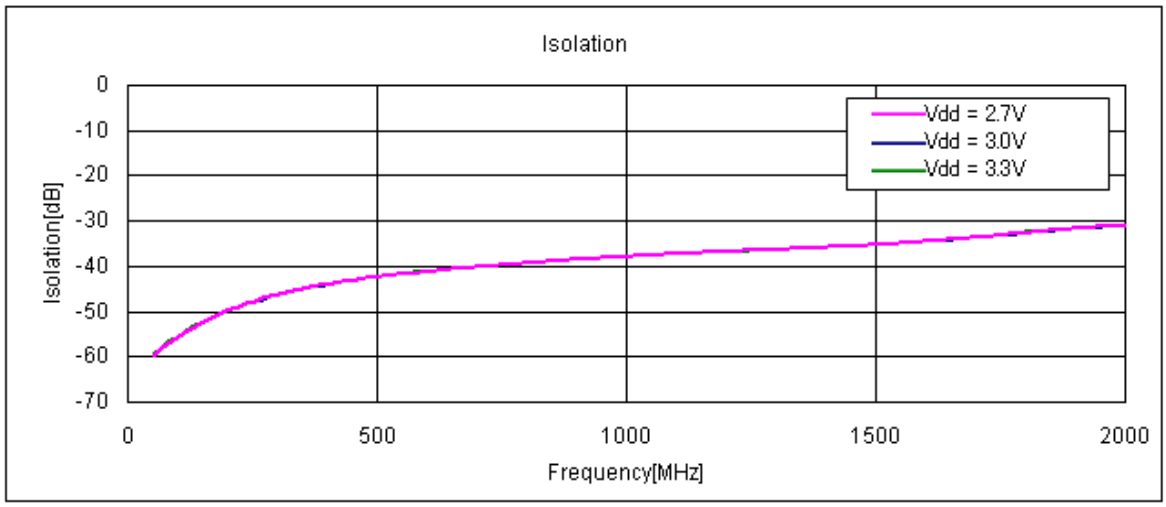


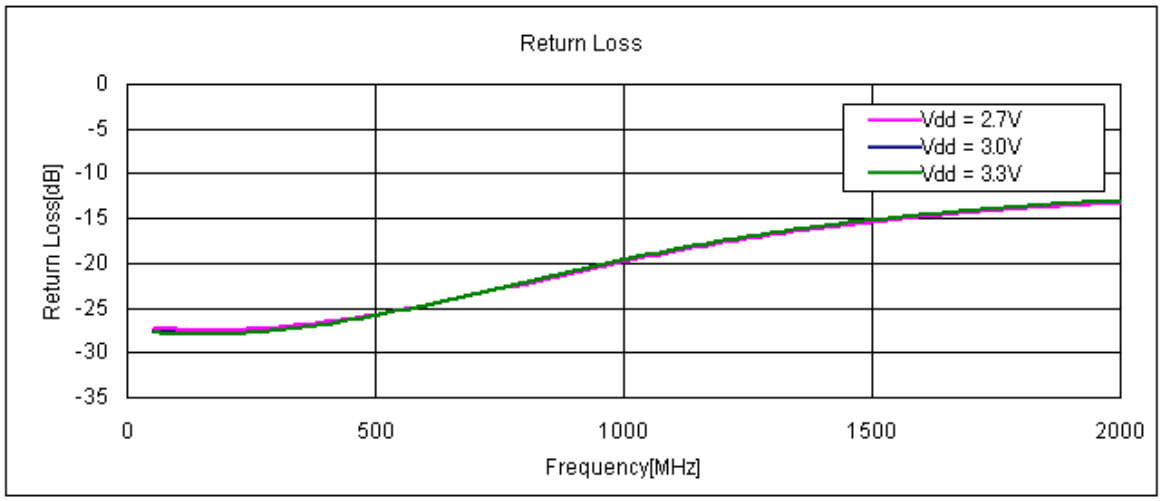




TYPICAL PERFORMANCE DATA @ V_{DD} = 2.7 / 3 / 3.3V, Ta = 85°C







POWER ON

It needs to wait for more than 0.5msec due to avoid irregular operation after V_{DD} voltage is applied to the power supply pin. When RF signals are applied to RF ports under such irregular operation, the electrical characteristics are not guaranteed.

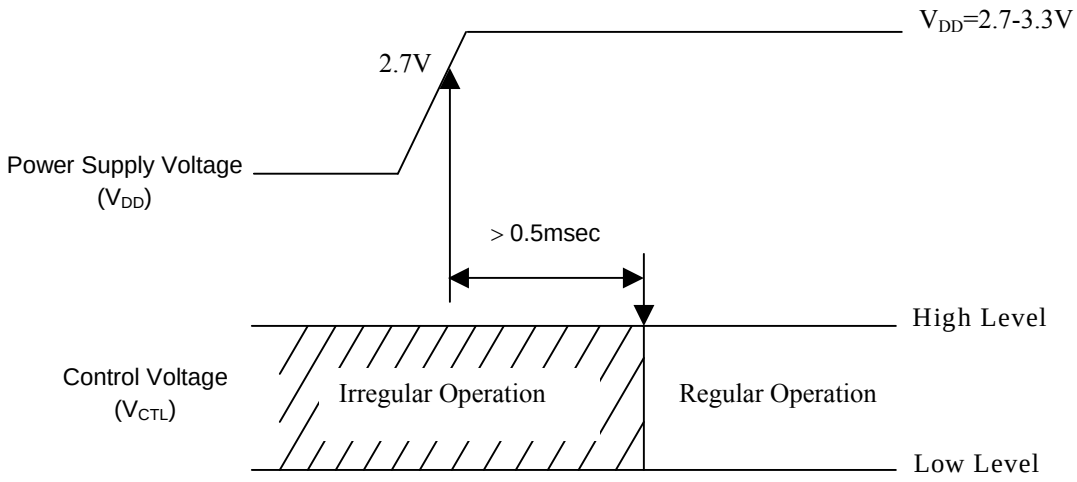


Figure 1. Power on Timing Chart

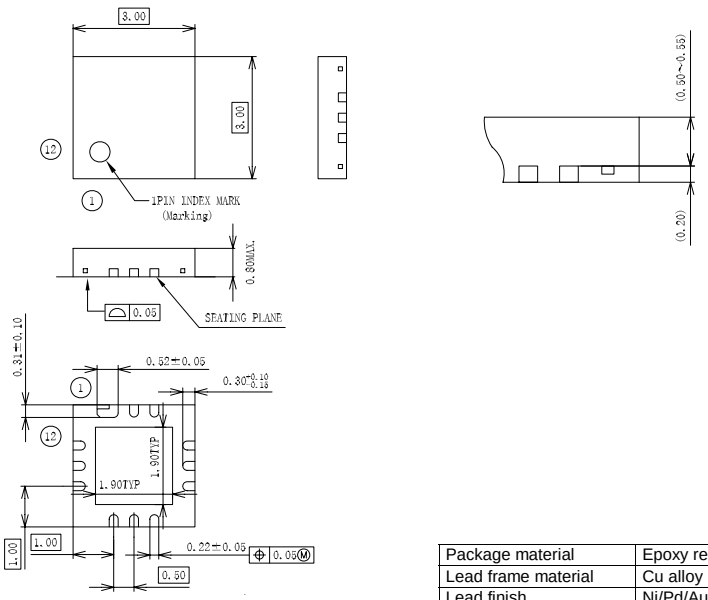
MISCELLANEOUS

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi® CMOS devices are immune to latch-up.

PACKAGE DIMENSIONS

P-WQFN12-0303-0.50-63



(Unit: mm)

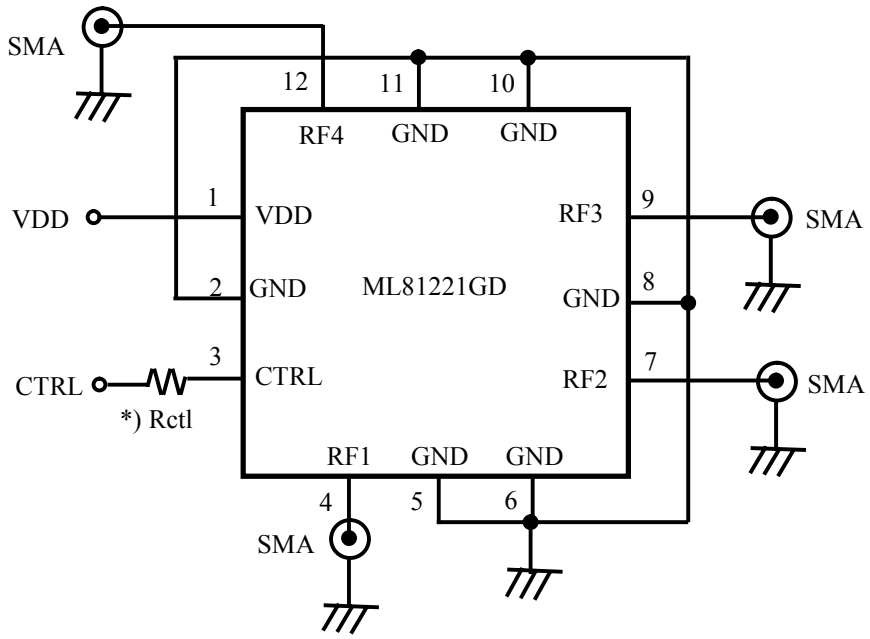
Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Ni/Pd/Au
Pin treatment	Au/Pd Max.0.01/Max.0.15 (μm)
Package weight (g)	0.01980 TYP.
Rev. No./Last Revised	2/Jun. 19, 2007

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

EVALUATION BOARD SCHEMATIC



* Rctl: Stabilization resistor for control signal. Recommended value = 1kΩ.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL81221GD-01	Feb. 8,2008	–	–	Final edition 1

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