HJ6xxM2PCH00 Series

High density MROM Card

■ DESCRIPTION

The Hitachi HJ6xxM2PCH00 is a high density Mask Programmamble Read Only Memory (MROM) card series organized as a x8 or x16 data bus. The HJ6xxM2PCH00 meets the requirements of PCMCIA 2.0 and JEIDA 4.1 in a Type I form.

The HJ6xxM2PCH00 series achieves high speed access, low power consumption, and a high level of reliability by employing the advanced MNOS memory technology and CMOS process and circuitry technology of Hitachi's HN624116N.

The low power of the HJ6xxM2PCH00 series makes it ideal for use in portable, battery powered equipment giving the user the longest possible system operating time. The high speed makes it possible to execute programs directly out of the card giving you the highest possible system performance.

The HJ6xxM2PCH00 includes the PCMCIA 2.0 Level 1 $\overline{CIS}$ (card information structure) data preprogramed in the card in a non volatile area.

The HJ6xxM2PCH00 series is offered in PCMCIA 68 pin card in the Type I form.

■ FEATURES

- Single Power Supply:
  V_{cc} = 5V ± 10%
- Fast Access Time:
  150/180ns (max)
- NibbleAccess Time:
  105/120ns (max)
- Low Power Dissipation:
  Active Current: 140 mA/MHz (typ)
  Standby Current: 110 uA (max) (4MB card)
- User selectable organization:
  x8 (byte mode)
  x16 (word mode)
  Switchable with CE1 & CE2 lines
- CIS preprogrammed
  Accessed with $\overline{REG}$ line.
- Pinouts:
  PCMCIA Standard 68 pin
- Packages:
  PCMCIA Type I (85.6 x 54 x 3.3mm)

■ ORDERING INFORMATION

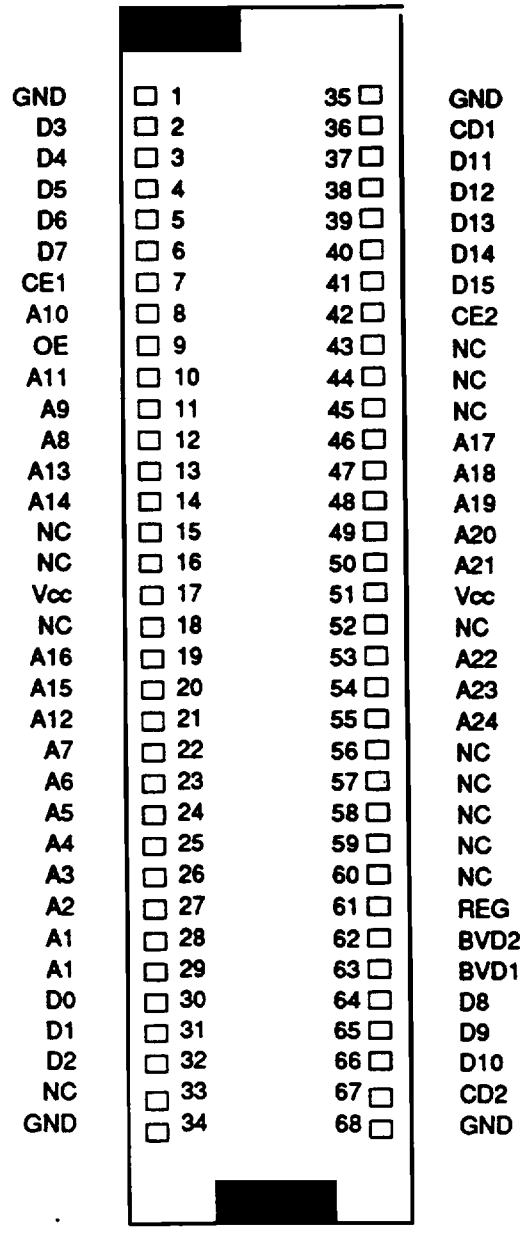
Type No.	Access Time
HJ6xxM2PCH00 -15	150 ns

xx = density in megabytes (i.e. HJ604M2PCH00 =4MB)

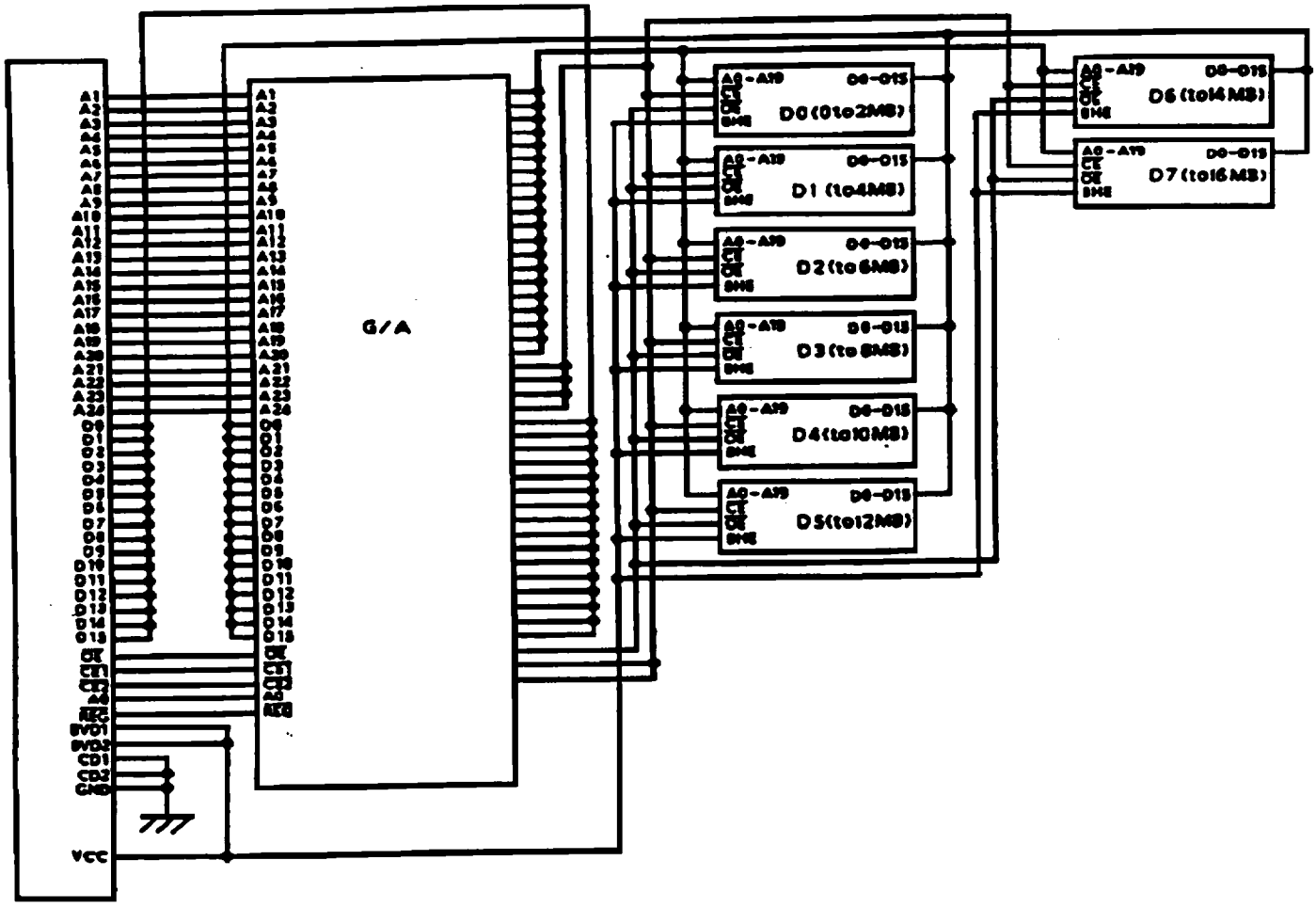
■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{20}	Address
D_0 - D_{15}	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE1,2}$	Card Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
CD1,2	Card detect
$\overline{REG}$	Attribute memory

■ PIN ARRANGEMENT



■ Block Diagram (ex . 16MB)



■ COMMON MEMORY READ

Mode	$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	$\overline{OE}$	$\overline{REG}$	A_0	D_{15}-D_8	D_7-D_0
Read (8 bit mode)	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	V_{IL}	High-Z	Even Byte
	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	High-Z	Odd Byte
Read (16 bit mode)	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	X	High-Z	High-Z
Read (odd byte only)	V_{IH}	V_{IL}	X	V_{IL}	V_{IH}	X	High-Z	High-Z
Standby	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	High-Z	High-Z

Note: 1. X = Don't Care

■ ATTRIBUTE MEMORY READ

Mode	$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	$\overline{OE}$	$\overline{REG}$	A_0	D_{15}-D_8	D_7-D_0
Read (8 bit mode)	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	V_{IL}	High-Z	Even Byte
	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	High-Z	Odd Byte
Read (16 bit mode)	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	X	High-Z	High-Z
Read (odd byte only)	V_{IH}	V_{IL}	X	V_{IL}	V_{IH}	X	High-Z	High-Z
Standby	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5 to +7.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	15	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	20	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	10	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current[1]	I_{CC1}	-	-	110	µA	$\overline{CE}$ = V_{CC}
Operating V_{CC} Current[1]	I_{CC3}	-	-	140	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 150 ns
Input Voltage	V_{IL}	-0.3 [2]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 3	V	
	VI_H	V_{CC} - 0.5	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. Based on 4MB card density.
2. V_{IL} min = -1.0 V for pulse width 50 ns.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

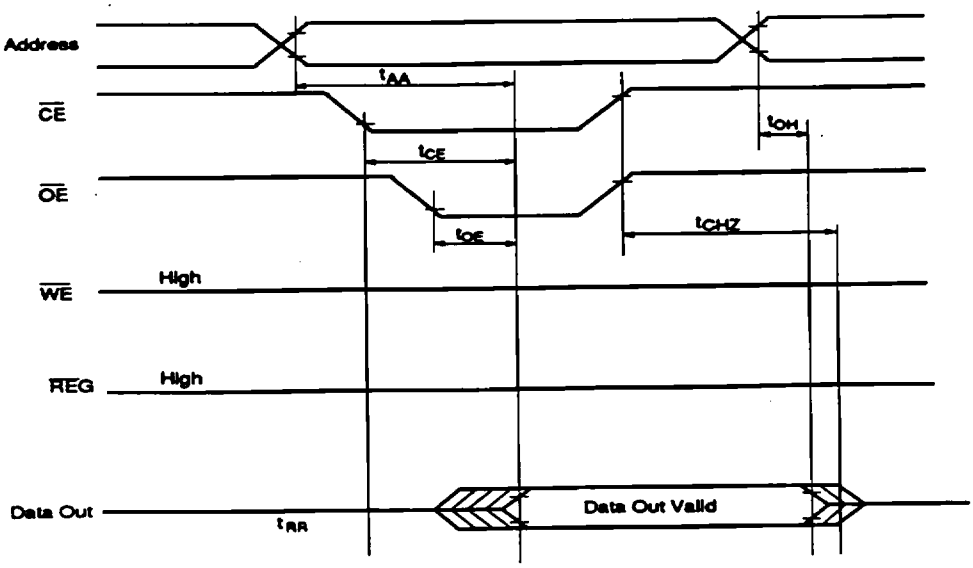
(T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

Test Conditions

- Input pulse levels: 0.6 V to 2.4 V
- Input rise and fall times: 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	Min.	Max.	Unit	Test Condition
Address Access Time	t_{AA}	-	150	ns	CE = OE = V_{IL}, WE = V_{IH}
Chip Enable Access Time	t_{CE}	-	150	ns	OE = V_{IL}, WE = V_{IH}
Output Enable Access Time	t_{OE}		70	ns	CE = V_{IL}, WE = V_{IH}
Output Hold to Address Change	t_{OHA}	0	-	ns	CE = OE = V_{IL}, WE = V_{IH}
Output Disable to High-[1]	t_{CHZ}	0	70	ns	CE = V_{IL}, WE = V_{IH}
Card Disable to High-Z	t_{OHZ}	0	70	ns	OE = V_{IL}, WE = V_{IH}

■ READ TIMING WAVEFORM (Common memory)



■ READ TIMING WAVEFORM (Attribute memory)