Signetics

74LS1802
Bit Stream Manager

Serializer/Deserializer
Product Specification

Logic Products

DESCRIPTION

The 74LS1802 Serializer/Deserializer (Figure 1) incorporates speed, flexibility, and proven ISL technology into a general-purpose device that performs many of the functions necessary for the implementation of a disk or communications controller. On-chip serializing/deserializing, programmable ECC and CRC operation, and bit comparison logic (useful for address-mark or header comparisons) make for a truly versatile device. A selectable 8- or 16-bit data bus and associated control lines allow for a DMA interface which requires little external hardware — a minimum system may be easily built with a microcontroller, a DMA controller, a RAM buffer, disk control lines and interface logic.

FEATURES

- **Data rates up to 10MHz**
- **Selectable CRC-16 or CRC-CCITT polynomials**
- **Full Duplex operation with CRC/ECC on receive data**
- **Programmable ECC polynomial register**
- **Programmable control register**
- **On-chip bit comparator**
- **8- or 16-bit selectable data bus**
- **48-pin DIP**

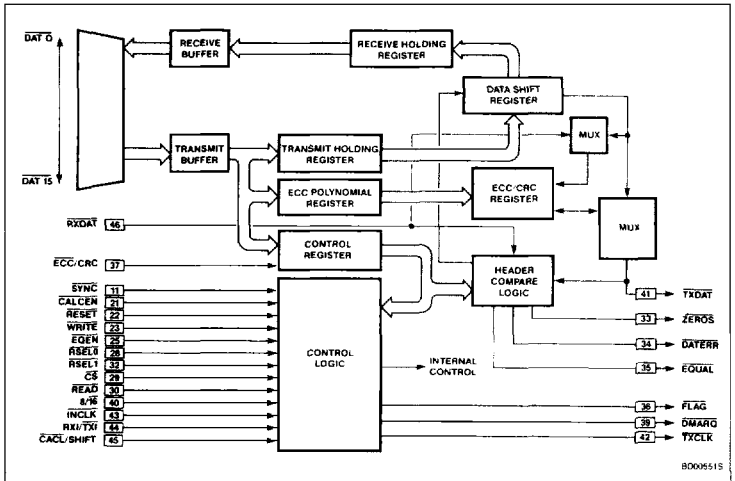
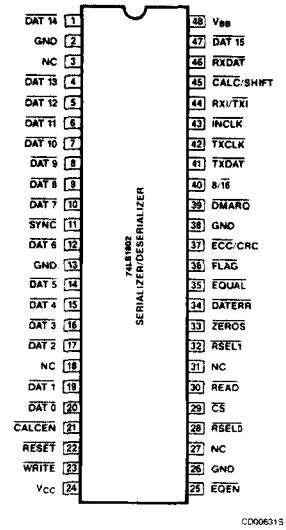
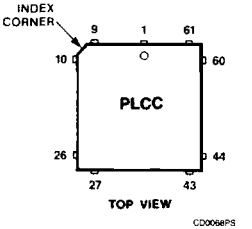


Figure 1. 74LS1802 Serializer/Deserializer Block Diagram

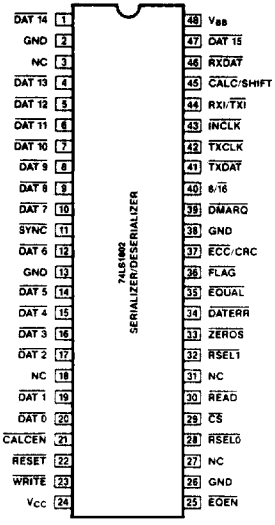
PIN CONFIGURATION





PLCC	FUNCTION	PLCC	FUNCTION	PLCC	FUNCTION
1	VBB	24	DAT 2	47	ZEROS
2	DAT 14	25	NC	48	DATERR
3	GND	26	NC	49	EQUAL
4	NC	27	NC	50	FLAG
5	DAT 13	28	DAT 1	51	ECC/CRC
6	DAT 12	29	DAT 0	52	NC
7	DAT 11	30	CALCEN	53	GND
8	NC	31	NC	54	DMARQ
9	NC	32	RESET	55	NC
10	NC	33	NC	56	8/16
11	NC	34	WRITE	57	TXDAT
12	DAT 10	35	VCC	58	TXCLK
13	DAT 9	36	EOEN	59	NC
14	DAT 8	37	GND	60	NC
15	NC	38	NC	61	NC
16	DAT 7	39	RSEL0	62	NC
17	SYNC	40	CS	63	INCLK
18	DAT 6	41	READ	64	RXI/TXI
19	GND	42	NC	65	CALC/SHIFT
20	NC	43	NC	66	RXDAT
21	DAT 5	44	NC	67	NC
22	DAT 4	45	NC	68	DAT 15
23	DAT 3	46	RSEL1		

PIN DESCRIPTION



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PIN NO.	IDENTIFIER	DESCRIPTION
1, 4–10 12, 14–17 19–20, 47	$\overline{DAT0}$ – $\overline{DAT15}$	DATa Bus — bidirectional, tri-state lines that communicate serialized/deserialized data, control and ECC polynomial information.
2	GND	Ground.
3	NC	Not connected.
11	$\overline{SYNC}$	SYNChronization Input – active low; generated by the 74LS1801 in the receive mode, and generated externally for transmit mode.
13	GND	Ground.
18	NC	Not connected.
21	$\overline{CALCEN}$	CALCulate ENable – when active low, this input enables the error detection circuit to calculate/compare CRC check bits for data or ID fields.
22	$\overline{RESET}$	When active low, this input clears the Data Shift Register and the $\overline{DMARQ}$ output.
23	$\overline{WRITE}$	When active low, this input latches data on the Data Bus into the Transmit Hold Register, the Control Register, or the ECC Polynomial Register.
24	V_{CC}	Supply voltage.
25	$\overline{EQEN}$	EQual ENable – when active low, this input enables the $\overline{EQUAL}$ output.
26	GND	Ground.

PIN NO.	IDENTIFIER	DESCRIPTION
27	NC	Not connected.
28 32	$\overline{RSEL0}$, $\overline{RSEL1}$	Register SELect — inputs that designate which input register (Control Register, Transmit Hold Register or ECC Polynomial Register) is to be written into.
29	$\overline{CS}$	Chip Select – when active low, this input enables $\overline{READ}$ and $\overline{WRITE}$ lines for data transactions.
30	$\overline{READ}$	When active low, this input enables data transfer from the Receive Hold Register onto the Data Bus.
31	NC	Not connected.
33	$\overline{ZEROS}$	When active low, this output indicates that both bits under comparison are in 0 state and vice versa.
34	$\overline{DATERR}$	DATa ERRor – when active low, this output indicates that an $\overline{ECC}$/CRC error has been detected.
35	$\overline{EQUAL}$	When active low, this output indicates that both bits in the bit comparator are in the same state.
36	$\overline{FLAG}$	An active low output pulse generated every 8- or 16-bits; $\overline{FLAG}$ indicates that data is available in receive mode or is requested in transmit mode.
37	$\overline{ECC}$/CRC	When this input is low, the 32-bit ECC circuit is selected; when high, the 16-bit CRC circuit is selected.
38	GND	Ground.
39	$\overline{DMARQ}$	DMA ReQuest – when active low, this output indicates that data is available either in receive mode or is requested in transmit mode. (See control register description.)
40	8/$\overline{16}$	When low, this input designates 16-bit operation; when high, 8-bit operation is selected.
41	$\overline{TXDAT}$	Transmit Data – NRZ transmit data.
42	$\overline{TXCLK}$	Output clock with frequency equal to receive and transmit data.
43	$\overline{INCLK}$	Input clock with frequency equal to receive and transmit data.
44	RXI/$\overline{TXI}$	When low, this input designates transmit mode; when high, receive mode is selected.
45	$\overline{CALC}$/SHIFT	When low, this input causes the error detection circuit to generate the syndrome bytes. At the end of a data or ID field, $\overline{CALC}$/SHIFT is forced high to shift out check bits (transmit mode), or compare these bits with received check bits (receive mode).
46	$\overline{RXDAT}$	Receive data – NRZ receive data.
48	V_{BB}	Supply voltage for internal circuits.

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FUNCTIONAL OPERATION

As shown in Figure 1, data I/O is facilitated by either an 8- or 16-bit bus. A high at 8/$\overline{16}$ input puts the 74LS1802 into an 8-bit mode; when low, a 16-bit mode is indicated. Incoming data on the bus takes one of three forms: transmit data to be serialized, ECC polynomial specification data, or control register information. The 74LS1802 is informed of the type of input data through the $\overline{RSEL0}$ and $\overline{RSEL1}$ inputs, and as shown in Table 1, data is placed in one of three registers:

Table 1. Input Data Register Designations

$\overline{RSEL0}$	$\overline{RSEL1}$	REGISTER NAME
L	H	Cont Reg
H	L	Xmit Hold Reg
H	H	ECC Polyn Reg

Control Register

The Control Register shown in the accompanying diagram is a 5-bit register which can be programmed to implement the following modes/functions.

MSB **LSB**

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Where,

Bit 0 = $\overline{LEDGE}$/TEDGE
Bit 1 = ECC PRESET
Bit 2 = CRC PRESET
Bit 3 = $\overline{EQUAL}$/LATCH
Bit 4 = $\overline{CRC16}$/CRC-CCITT

Bit 0 ($\overline{LEDGE}$/TEDGE)

The falling edge of $\overline{DMARQ}$ indicates to an external DMA device to perform a Read or a Write. If the $\overline{LEDGE}$/TEDGE bit is set to 0, $\overline{DMARQ}$ is terminated by the rising edge of $\overline{READ}$ or $\overline{WRITE}$; when this bit is set to 1, $\overline{DMARQ}$ is terminated by the falling edge of $\overline{READ}$ or $\overline{WRITE}$.

Bit 1 (ECC PRESET)

The ECC shift register must be preset to either all 0's or all 1's to be compatible with existing systems. When the ECC PRESET bit is set to 0, the ECC shift register is preset to 1's. When set to 1, the shift register is set to 0's.

Bit 2 (CRC PRESET)

To be compatible with existing systems, the CRC shift register must be preset to either all 0's or all 1's. For example, IBM 3740 and SYSTEM 34 compatible floppy disks require that the CRC shift register be preset to 1's, while Intel ISIS compatible disks require that this register be set to 0's. When the CRC PRESET bit is set to 0, the CRC shift register is preset to 1's; when set to 1, this register is set to 0's.

Bit 3 ($\overline{EQUAL}$/LATCH)

The $\overline{EQUAL}$ output indicates the status of an internal bit-comparator. When the $\overline{EQUAL}$/LATCH bit is set to 0, $\overline{EQUAL}$ reflects the status of the bit comparator on a per-bit basis. When set to 1, $\overline{EQUAL}$ is latched on the first miscompare between receive and transmit data – this condition is cleared (i.e., $\overline{EQUAL}$ is returned to a high state) when $\overline{SYNC}$ goes high.

Bit 4 ($\overline{CRC16}$/CCITT)

When set to 0, the CRC circuit selects the standard CRC-16 polynomial ($X^{16} + X^{15} + X^2 + 1$); when set to 1, the standard CRC-CCITT polynomial ($X^{16} + X^{12} + X^5 + 1$) is selected.

Transmit Hold Register

The main function of the Transmit Hold Register is to hold a byte/word in reserve, ready for transmission.

Before data is transmitted, it is loaded into the Transmit Hold Register. $\overline{SYNC}$ is externally activated to start the transmit process. This in turn activates $\overline{FLAG}$, and $\overline{DMARQ}$. Generation of $\overline{FLAG}$ and $\overline{DMARQ}$ indicates that the contents of the Transmit Hold Register have been loaded into the Data Shift Register. Hence, the next byte/word of data should be loaded into the Transmit-Hold Register.

ECC POLYNOMIAL REGISTER

This register is composed of 32 bits, each bit representing an X-term. It is selected by writing a one to the appropriate bit. An ECC polynomial is loaded by writing four consecutive bytes (least significant byte first) into the register. Thus the polynomial $X^{32} + X^{23} + X^{21} + X^{11} + X^8 + X^2 + 1$ would be programmed as follows:

BYTE NO.	DATA							
	MSB							LSB
	D7							D0
1	0	0	0	0	0	1	0	X
2	0	0	0	0	1	0	0	1
3	1	0	1	0	0	0	0	0
4	0	0	0	0	0	0	0	0

X = Don't care

The following would appear in the register as:

X^{32} X^{23} X^{21}
1 00000000 10100000
X^{11} X^8 X^2 X^0
00001001 00000101

with X^0 and X^{32} set to 1 by default.

ADDRESS MARK OR HEADER COMPARISONS

A bit comparator in the 74LS1802 compares one bit of received data with one bit of transmitted data; two status lines, $\overline{EQUAL}$ and $\overline{ZEROS}$, reflect the result of the comparison. When active low, $\overline{EQUAL}$ indicates both bits are in the same state, while $\overline{ZEROS}$ indicates the status of the bits under comparison. In this mode the chip is operating in a full duplex mode with CRC/ECC being performed on the receive data.

$\overline{EQUAL}$ can be used to detect a specific address mark or disk header. The expected header to be identified is loaded into the Transmit Hold Register, and RXI/$\overline{TXI}$ is set low for transmit mode. The $\overline{SYNC}$ input originates from the 74LS1801 Encoder/Decoder, and when active low, indicates that data following a preamble of 0's may be an address mark (see 74LS1801 Decoding Logic). Thus, $\overline{EQUAL}$ and $\overline{ZEROS}$ reflect the actual status of the bit comparator when $\overline{SYNC}$ is active low; when $\overline{SYNC}$ is inactive high, $\overline{EQUAL}$ and $\overline{ZEROS}$ are held active. Note that $\overline{SYNC}$ must be reset at the end of a header in preparation for a following read or write.

As specified by the $\overline{EQUAL}$/LATCH Bit in the Control Register, the bit comparator operates in one of two modes. When the control bit is 0, $\overline{EQUAL}$ reflects the status of the bit comparator on a per-bit basis. When the control bit is 1, $\overline{EQUAL}$ is latched on the first miscompare between received and transmitted data and stays in this mode until $\overline{SYNC}$ becomes inactive high.

TRANSMITTING DATA

To transmit data, several initializations must take place: RXI/$\overline{TXI}$ must be held low to indicate a transmit operation, $\overline{ECC}$/CRC is set to the appropriate state, and $\overline{CALC}$/SHIFT must be held low to put the $\overline{ECC}$/CRC circuit into "calculate mode." After the first byte/word of data has been loaded into the Transmit Hold Register, $\overline{SYNC}$ must be externally activated (low) to begin the transmit process. Activating $\overline{SYNC}$ forces the $\overline{FLAG}$ and $\overline{DMARQ}$ lines to go active, after which the next byte/word of data may be loaded into the device. Thereafter, $\overline{FLAG}$ and $\overline{DMARQ}$ will go active every 8 or 16 bits to request more data.

$\overline{CALCEN}$ may be activated to enable the $\overline{ECC}$/CRC circuit before the start of the byte that is to be included in the $\overline{ECC}$/CRC calculations. While the last byte of the data or header field is being shifted-out, $\overline{CALC}$/SHIFT must be forced high, causing the $\overline{ECC}$/CRC check bits to be shifted out after the data. As a result, $\overline{SYNC}$ must be held active low for at least 32 bits (ECC) or 16 bits (CRC) following the last bit of the data field. Typical timing for a transmit operation is shown in Figure 2.

RECEIVING DATA

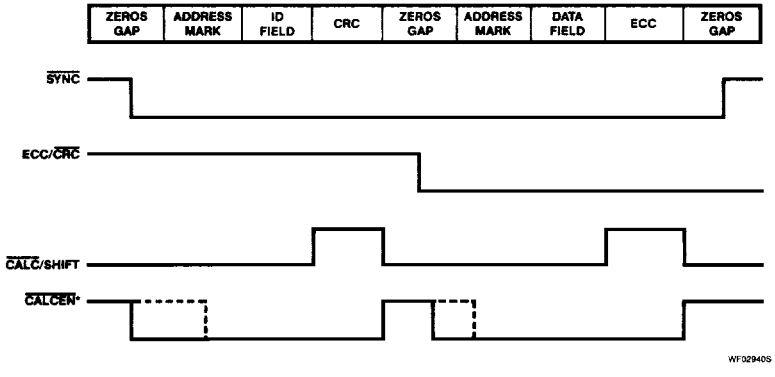
Several conditions must be fulfilled before a receive operation takes place. RXI/$\overline{TXI}$ is held high to indicate a receive operation, $\overline{ECC}$/CRC is set to the appropriate state, and $\overline{CALC}$/SHIFT is held low to put the $\overline{ECC}$/CRC circuit into "calculate mode." If the address mark is to be included in $\overline{ECC}$/CRC calculations, $\overline{CALCEN}$ may be activated low at this time. Once these conditions have been fulfilled, receive data can be enabled.

When $\overline{SYNC}$ is activated, a counter circuit sets up either 8- or 16-bits of data and generates active $\overline{FLAG}$ and $\overline{DMARQ}$ outputs to indicate data available in the Receive Hold Register. This continues until $\overline{SYNC}$ becomes high.

While the last byte of data is being received $\overline{CALC}$/SHIFT must be forced high to put the $\overline{ECC}$/CRC circuit into "checkmode" at the beginning of the next byte. At this time, check bits on receive data are compared to check bits appended to the end of the data field; if the two groups of bits do not match, $\overline{DATERR}$ is activated. $\overline{DATERR}$ is latched internally and is cleared when $\overline{SYNC}$ goes inactive.

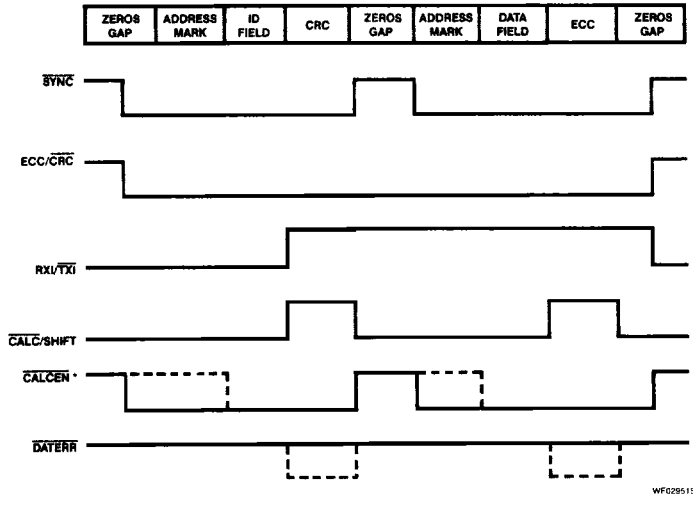
Note that $\overline{SYNC}$ must be held active until all check bits (32 for ECC, 16 for CRC) have been compared. The result of the bit comparison is held in the Receive Hold Register. If no error occurred, the Receive Hold Register will be set to 0's, otherwise these bytes are used in the correction process.

Typical timing for a header comparison (with CRC) is shown in Figure 3.



NOTE:
*$\overline{CALCEN}$ should be activated before or after the address mark, depending on whether or not the address mark is to be included in $\overline{ECC}$/CRC calculations.

Figure 2. Timing Example of a Transmit Operation



NOTE:
*$\overline{CALCEN}$ should be activated before or after the address mark, depending on whether or not the address mark is to be included in $\overline{ECC}$/CRC calculations.

Figure 3. Timing Example of a Header Comparison (with CRC)

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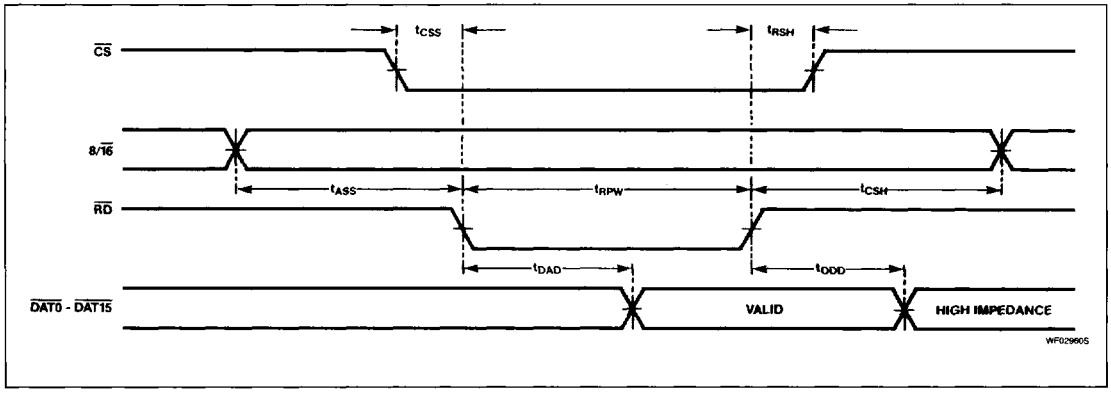
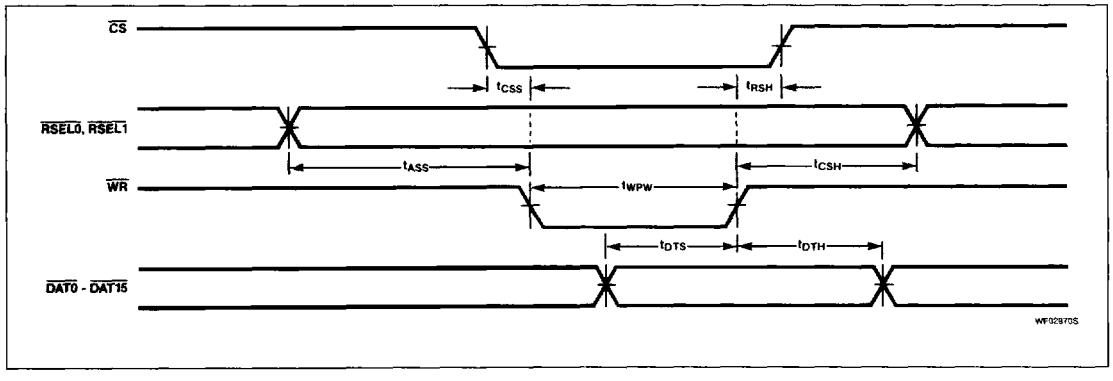
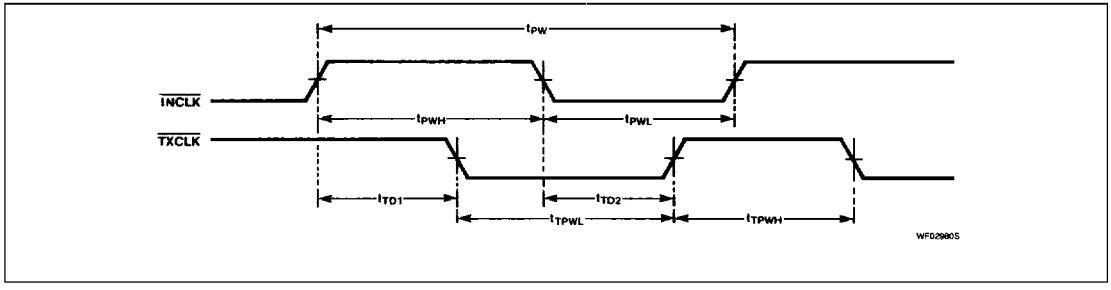
READ CYCLE TIMING



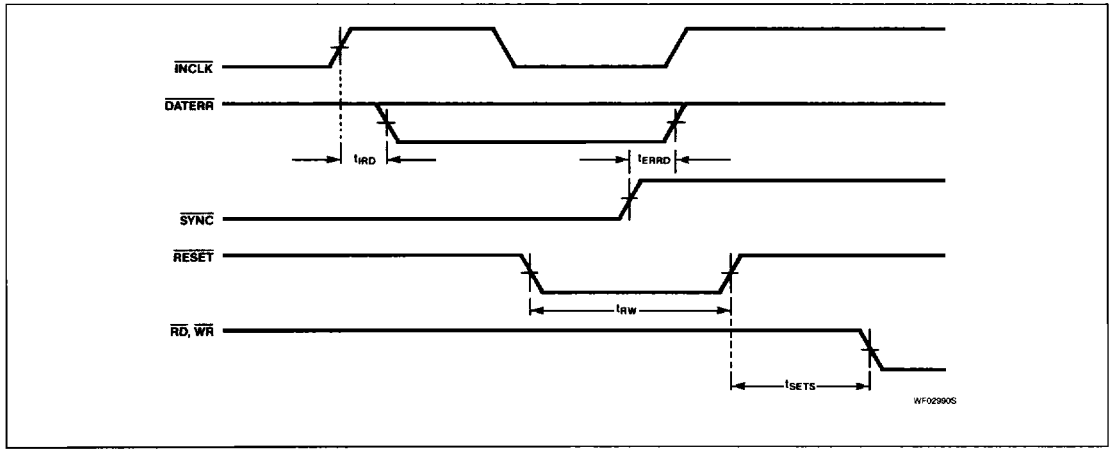
WRITE CYCLE TIMING



CLOCK CYCLE TIMING



OTHER TIMING



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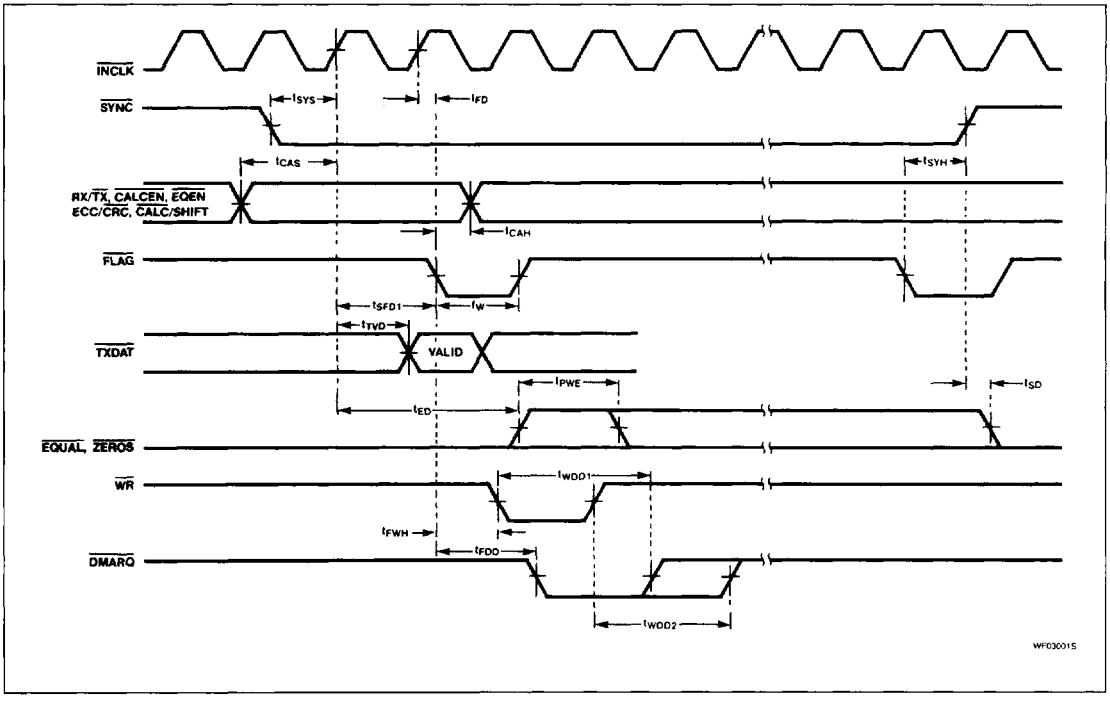
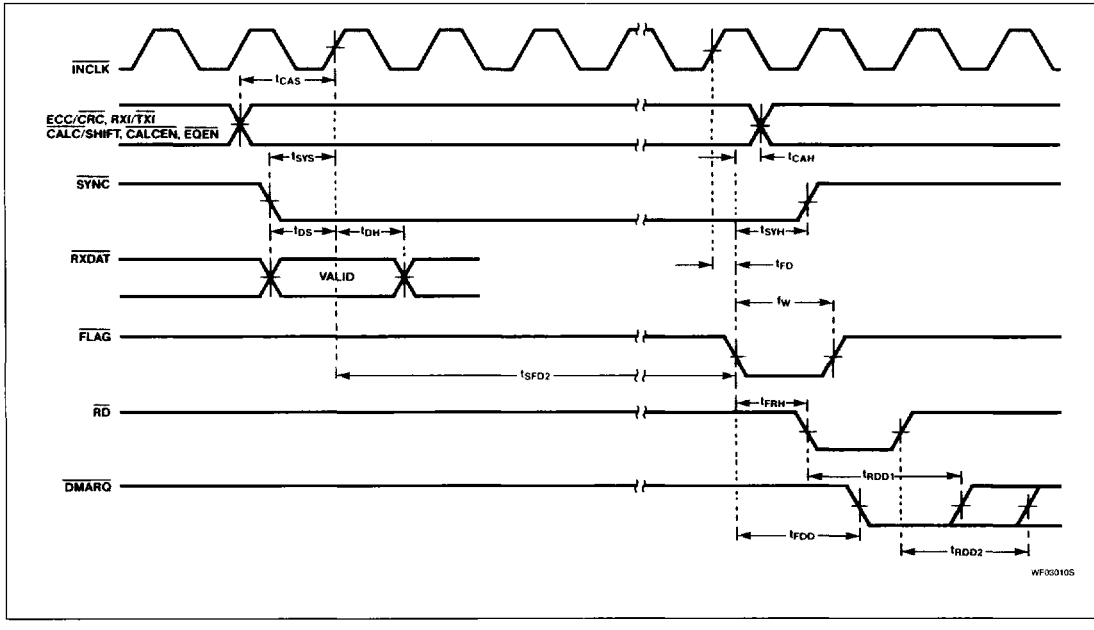
TRANSMIT, CRC/ECC CALCULATE AND SHIFT TIMING



RECEIVE, ECC/CRC CALCULATE AND RECEIVE TIMING



ABSOLUTE MAXIMUM RATINGS

PIN	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V
All other	Logic input pins	5.5	V

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±5%

PARAMETER		TEST CONDITIONS	LIMITS			UNIT	COMMENTS
			Min	Typ	Max		
V_{CD}	Input clamp diode voltage	I_{IN} = 18mA			-1.5	V	
V_{TH}	Input threshold voltage		0.8		2.0	V	
I_{IL}	Input low current	V_{IN} = 0.4V			-20	μA	
I_{IH}	Input high current	V_{IN} = 2.7V			20	μA	
I_I	Max input high current	V_{IN} = 5.5V			100	μA	
V_{OL}	Output low voltage	I_{OH} = 8mA			0.5	V	
V_{OH}	Output high voltage	I_{OL} = -400μA	2.7			V	
I_{OS}	Output short circuit current	V_{OUT} = 0V	-15		-100	mA	
I_{CC}	Power supply current (buffers)				75	mA	
I_{BB}	Power supply current (gates)				260	mA	

AC ELECTRICAL CHARACTERISTICS (all time in nanoseconds)

PARAMETER	DESCRIPTION	LIMITS		
		Min	Typ	Max
t_{PWH}	$\overline{INCLK}$ High time	50		
t_{PWL}	$\overline{INCLK}$ Low time	50		
t_{tPWH}	$\overline{TXCLK}$ High time	50		
t_{tPWL}	$\overline{TXCLK}$ Low time	50		
t_{PWE}	$\overline{EQUAL}$, $\overline{ZEROS}$ High time		t_{PW}	
f_W	$\overline{FLAG}$ Low time		98	
t_{RW}	$\overline{RESET}$ Low time		50	
t_{WPW}	$\overline{WR}$ Pulse width		50	
t_{RPW}	$\overline{RD}$ Pulse width		100	
t_{PW}	$\overline{INCLK}$ Cycle time	100		
t_{CSS}	$\overline{CS}$ set-up to $\downarrow$WR and $\downarrow$RD	0		
t_{ASS}	$\overline{RSEL0}$, $\overline{RSEL1}$ 8/$\overline{16}$ set-up to $\downarrow\overline{RD}$ and $\downarrow\overline{WR}$		35	
t_{SETS}	$\overline{RESET}$ set-up to $\downarrow\overline{RD}$, $\downarrow\overline{WR}$		52	
t_{DTS}	$\overline{DAT0}$ - $\overline{DAT15}$ set-up to $\uparrow\overline{WR}$		35	
t_{SYS}	$\overline{SYNC}$ set-up to $\uparrow\overline{INCLK}$		½ t_{PW}	
t_{CAS}	RX/$\overline{TX}$, ECC/$\overline{CRC}$, $\overline{CALC}$/SHIFT, $\overline{CALCEN}$, $\overline{EQEN}$ set-up to $\uparrow\overline{INCLK}$		t_{PW}	
t_{FD}	$\uparrow\overline{INCLK}$ to $\downarrow\overline{FLAG}$ delay		2	
t_{DS}	$\overline{RXDAT}$ VALID TO $\uparrow\overline{INCLK}$		½ t_{PW}	
t_{RDD1}	$\downarrow\overline{RD}$ to $\uparrow\overline{DMARQ}$		86	
t_{RDD2}	$\uparrow\overline{RD}$ to $\uparrow\overline{DMARQ}$		81	
t_{SFD1}	$\uparrow\overline{INCLK}$ to $\downarrow\overline{FLAG}$		t_{PW} + 2	
t_{ED}	$\uparrow\overline{INCLK}$ to $\uparrow\overline{EQUAL}$, $\overline{ZEROS}$ delay		t_{PW} + 91	
t_{TD1}	$\uparrow\overline{INCLK}$ to $\downarrow\overline{TXCLK}$		46	
t_{TD2}	$\downarrow\overline{INCLK}$ to $\uparrow\overline{TXCLK}$		33	
t_{RSH}	$\uparrow\overline{RD}$, $\uparrow\overline{WR}$ to $\overline{CS}$ hold	0		
t_{CSH}	$\uparrow\overline{RD}$, $\uparrow\overline{WR}$ to $\overline{RSEL0}$, $\overline{RSEL1}$, 8/$\overline{16}$ hold		19	
t_{DTH}	$\uparrow\overline{WR}$ to $\overline{DAT0}$ - $\overline{DAT15}$ hold		150	
t_{FWH}	$\downarrow\overline{FLAG}$ to $\downarrow\overline{WR}$	0		
t_{CAH}	$\downarrow\overline{FLAG}$ to $\overline{CALC}$/SHIFT, $\overline{EQUEN}$, $\overline{CALCEN}$, ECC/$\overline{CRC}$, RX/$\overline{TX}$ hold	0		
t_{DAD}	$\downarrow\overline{RD}$ to $\overline{DAT0}$ - $\overline{DAT15}$ valid		59	
t_{IRD}	$\uparrow\overline{INCLK}$ to $\downarrow\overline{DATERR}$		7	
t_{TVD}	$\uparrow\overline{INCLK}$ to $\overline{TXDAT}$ valid		49	
t_{ODD}	$\uparrow\overline{RD}$ to $\overline{DAT0}$ - $\overline{DAT15}$ changing		50	
t_{ERRD}	$\uparrow\overline{SYNC}$ to $\uparrow\overline{DATERR}$		44	
t_{DH}	$\uparrow\overline{INCLK}$ to $\overline{RXDAT}$ hold		½ t_{PW}	
t_{FRH}	$\downarrow\overline{FLAG}$ to $\downarrow\overline{RD}$	0		
t_{SYH}	$\downarrow\overline{FLAG}$ to $\overline{SYNC}$ hold	0		
t_{SD}	$\uparrow\overline{SYNC}$ to $\downarrow\overline{EQUAL}$		76	
t_{FDD}	$\downarrow\overline{FLAG}$ to $\downarrow\overline{DMARQ}$ delay		12	
t_{WDD1}	$\downarrow\overline{WR}$ to $\uparrow\overline{DMARQ}$ delay		86	
t_{WDD2}	$\uparrow\overline{WR}$ to $\uparrow\overline{DMARQ}$ delay		81	
t_{SFD2}	$\uparrow\overline{INCLK}$ to $\downarrow\overline{FLAG}$		9 t_{PW} +2	

NOTE:
All tabular entries are taken directly from simulation. No values are tested or guaranteed.

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