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FAST Products	

FAST 74F537

1-Of-10 Decoder (3-state)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F537	9 ns	44mA

DESCRIPTION

The 74F537 is one of ten decoder/demultiplexer with four active High BCD inputs and ten mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low or active High. The 'F537 has 3-state outputs, and a High signal on the Output Enable (\overline{OE}) input forces all outputs to the high impedance state. Two input Enables, active High (E_1) and active Low (\overline{E}_0), are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine causes all outputs to go to the inactive state (i.e., same polarity as the P input).

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
20-Pin Plastic DIP	N74F537N
20-Pin Plastic SOL	N74F537D

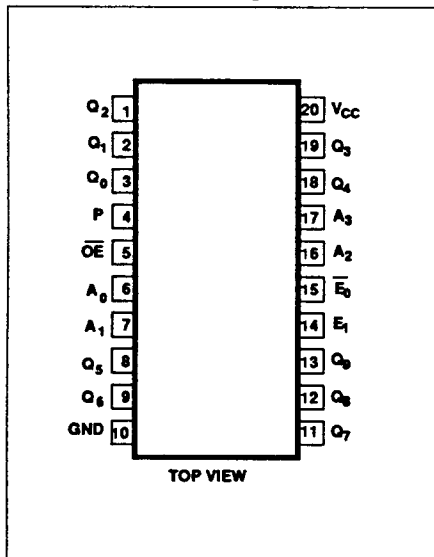
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	Data inputs	1.0/1.0	20 μ A/0.6mA
\overline{E}_0	Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
E_1	Enable input (active High)	1.0/1.0	20 μ A/0.6mA
P	Polarity control input	1.0/1.0	20 μ A/0.6mA
\overline{OE}	Output enable input	1.0/1.0	20 μ A/0.6mA
$Q_0 - Q_9$	Data outputs	150/40	3.0mA/24mA

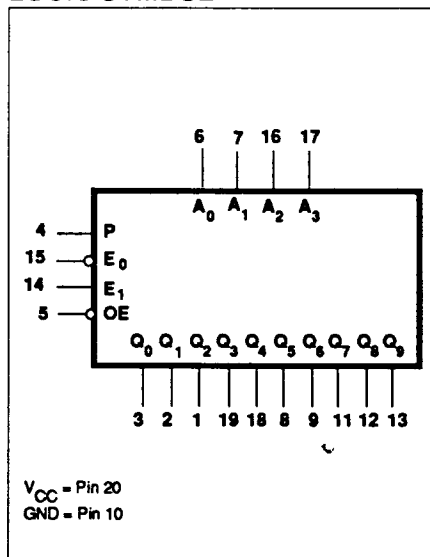
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

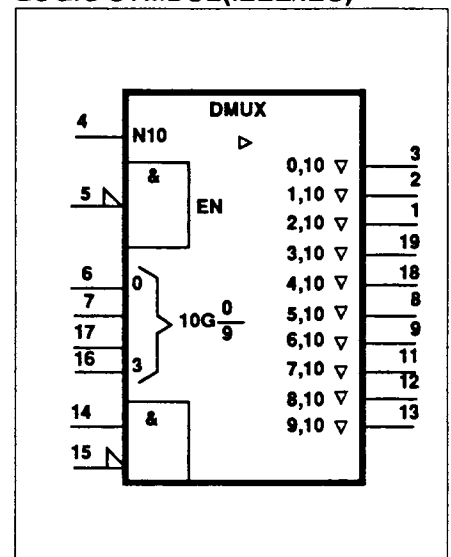
PIN CONFIGURATION



LOGIC SYMBOL



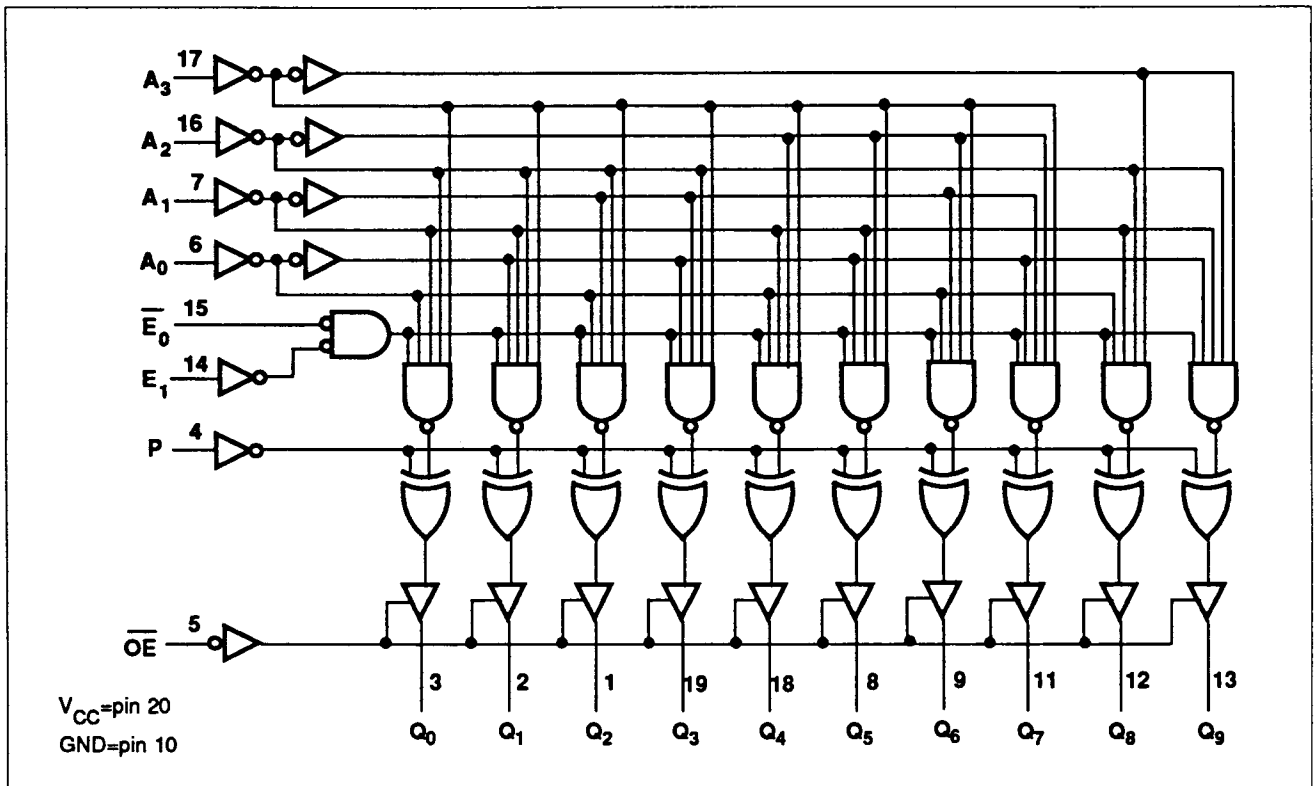
LOGIC SYMBOL (IEEE/IEC)



Decoder

FAST 74F537

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUTS												OPERATING MODE
OE	E ₀	E ₁	A ₃	A ₂	A ₁	A ₀		Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	Q ₈	Q ₉			
H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High impedance		
L	H	X	X	X	X	X	X	Outputs equal P input										Disable		
L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Active High output (P=L)		
L	L	H	L	L	L	H	L	L	H	L	L	L	L	L	L	L	L			
L	L	H	L	L	H	L	L	L	L	L	L	L	H	L	L	L	L			
L	L	H	L	L	H	H	L	L	L	L	L	L	L	L	L	H	L			
L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Active Low output (P=H)		
L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	L	L			
L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L	L			
L	L	H	H	L	X	X	L	L	L	L	L	L	L	L	L	L	L			
L	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	Active Low output (P=H)		
L	L	H	L	L	L	H	L	L	H	H	H	H	H	H	H	H	H			
L	L	H	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H			
L	L	H	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H			
L	L	H	L	H	H	L	L	H	H	H	H	H	H	L	H	H	H	Active Low output (P=H)		
L	L	H	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H			
L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L	L			
L	L	H	H	H	X	X	L	L	L	L	L	L	L	L	L	L	L			

H = High voltage level
L = Low voltage level
X = Don't care

Decoder

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_H	High-level input voltage	2.0			V
V_L	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			Min	Typ ²	Max		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$	2.4		V	
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\%V_{CC}$	2.7	3.3	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	0.50	V
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$			100	μA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$			-0.6	mA	
I_{OZH}	Off-state output current, High-level voltage applied	$V_{CC} = \text{MAX}, V_O = 2.7V$			50	μA	
I_{OZL}	Off-state output current, Low-level voltage applied	$V_{CC} = \text{MAX}, V_O = 0.5V$			-50	μA	
I_{OS}	Short circuit output current ³	$V_{CC} = \text{MAX}$		-60	-150	mA	
I_{CC}	Supply current (total)	$V_{CC} = \text{MAX}$		44	66	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_A = 25^\circ C$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

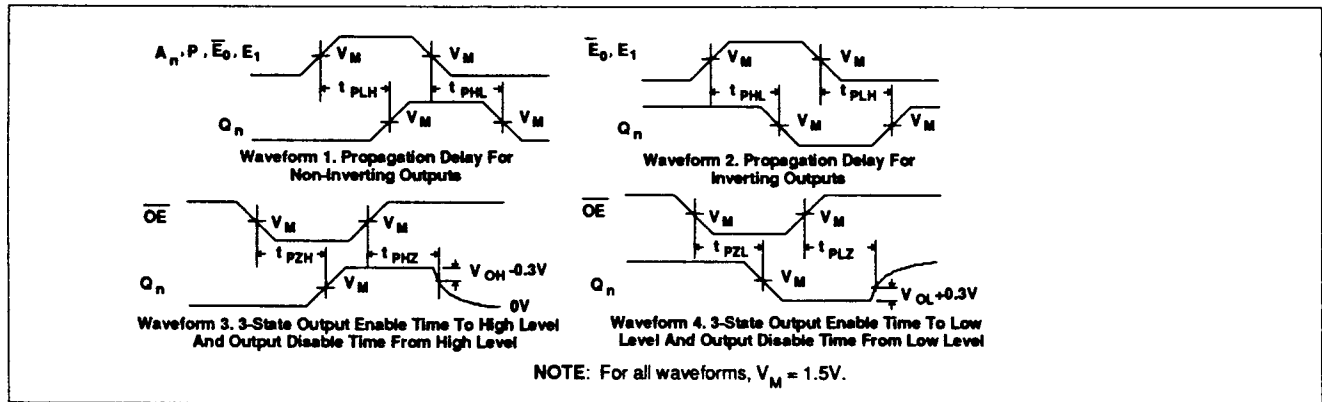
Decoder

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _A = +25°C V _{CC} = 5V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = 5V ±10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A _n to Q _n	Waveform 1	4.5 3.0	9.0 7.5	14.0 11.0	4.5 3.0	16.0 12.0	ns
t _{PLH} t _{PHL}	Propagation delay E ₀ to Q _n	Waveform 2	4.0 3.0	8.0 8.0	11.0 11.0	4.0 3.0	12.0 12.0	ns
t _{PLH} t _{PHL}	Propagation delay E ₁ to Q _n	Waveform 2	6.0 4.0	8.5 8.5	11.5 11.5	6.0 4.0	13.0 12.5	ns
t _{PLH} t _{PHL}	Propagation delay P to Q _n	Waveform 1	5.0 3.5	12.5 6.5	16.0 10.0	5.0 3.5	17.0 11.0	ns
t _{PZH} t _{PZL}	Output Enable time OE to Q _n	Waveform 3 Waveform 4	2.5 4.0	4.5 5.5	7.0 8.0	2.5 4.0	8.0 9.0	ns
t _{PHZ} t _{PLZ}	Output Disable time OE to Q _n	Waveform 3 Waveform 4	1.5 2.0	3.0 4.0	6.0 6.5	1.0 2.0	7.0 7.0	ns

AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

Test Circuit For 3-State Outputs

TEST	SWITCH
t _{PLZ} , t _{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

V_M = 1.5V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t _w	t _{TLH}	t _{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns