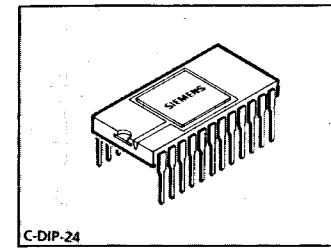
SIEMENS

# 8-Bit A/D Converter, 100 MHz — SDA 8010

**Preliminary Data** — **Bipolar IC**

## Features

- 100 MHz min. strobe frequency
- 6.3 effective bits at 30-MHz input frequency
- Excellent large-signal bandwidth
- ±1/2 LSB max. linearity error
- Balanced input voltage range
- ECL-100-K compatible output data
- Lower power dissipation



C-DIP-24

| Type | Ordering Code | Package |
|---|---|---|
| SDA 8010 | Q67000-A2566 | C-DIP-24 |

The SDA 8010 is an ultrafast A/D converter operating according to the parallel principle, with a resolution of 8 bits and a guaranteed strobe frequency of 100 MHz. The device is capable of digitizing full scale (±1 V) analog signals with frequency components up to 50 MHz at a power consumption of 1.3 W. Due to the symmetric input voltage range it can be driven directly by a customary 50-Ω source.

**Functional Description**

The SDA 8010 is an ultrafast A/D converter operating according to the "flash" or parallel principle: a field of 255 comparators simultaneously compares the analog signal with 255 reference voltages spread linearly over the input voltage range. The result of this comparison, delivered in the so-called thermometer code, is converted into binary representation by three encoding stages and is then available as a digital signal with ECL levels at the outputs **(see block diagram)**.

An individual comparator consists of a differential amplifier and a master/slave register stage. They are activated alternately by means of two strobe signals STR1 and STR2, thereby sampling the analog signal and holding the corresponding logical state. The sequence of the conversion process is given in the pulse diagram.

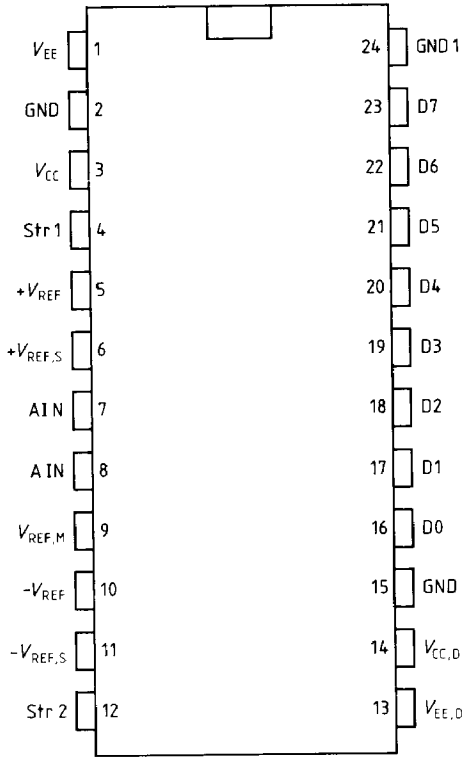
During the L phase of STR1, the analog signal is compared with the reference voltages. With the rising edge of STR1 the result of the comparison is passed into the first register stage and held there until the falling edge of STR1. Towards the end of this hold period the signal is accepted into the second flipflop with the L phase of the second strobe STR2 and stored with the rising edge. After a delay $t_{d,\,Q}$ this data appears at the output and remains valid for the period $t_{v,\,Q}$.

Driving the converter's analog input is an easy task. Due to the ground-symmetrical input voltage range and the low input capacitance, the converter can be operated in a customary 50-Ω system without any preamplifiers or level shifters. Nevertheless, lower impedance driving would be a means for further improving the device's specified dynamic parameters. Two input pins AIN ensure low lead inductance. The internal reference voltages are generated by an on-chip resistor string. The potential at its end points, $+V_{REF}$ and $-V_{REF}$, respectively, determine the input voltage range which is resolved with an accuracy of 8 bits. Additional sense pins $+V_{REF,\,S}$ and $-V_{REF,\,S}$ allow compensation of voltage drops across parasitic resistances at the top and bottom of the string. The assignment of the digital output code to the input voltage is shown in the transfer characteristic. As no overflow function is provided, the output will remain at a value of 255 when the reference voltage range is exceeded.

Connection $V_{REF,\,M}$ only serves for RF decoupling; no additional adjustment is required for maintaining the specified accuracy of $\pm 0.5$ LSB.

The use of two supply systems, $V_{CC}\,V_{EE}$ and $V_{CC,\,D}$, $V_{EE,\,D}$ and an additional ground line GND 1 for the output stages reduces the mutual influence of analog and digital signals. Additionally, the separate return of the analog signal ground line is recommended **(see test circuit)**.

**Figure 1**
**Pin Configuration**
(top view)



**Pin Definitions and Functions**

| Pin | Symbol | Function |
|---|---|---|
| 1 | $V_{EE}$ | Neg. supply voltage, analog section |
| 2 | GND | Ground |
| 3 | $V_{CC}$ | Pos. supply voltage, analog section |
| 4 | Str 1 | Strobe signal 1 |
| 5<br>6 | $+V_{REF}$<br>$+V_{REF,\,s}$ | Pos. reference voltage<br>Pos. reference voltage sense |
| 7<br>8 | A IN<br>A IN | Analog input<br>Analog input |
| 9 | $V_{REF,\,M}$ | Center tap of voltage divider |
| 10<br>11 | $-V_{REF}$<br>$-V_{REF,\,s}$ | Neg. reference voltage<br>Neg. reference voltage sense |
| 12 | Str 2 | Strobe signal 2 |
| 13<br>14 | $V_{EE,\,D}$<br>$V_{CC,\,D}$ | Neg. supply voltage, digital section<br>Pos. supply voltage, digital section |
| 15 | GND | Ground |
| 16 to 23 | D0 to D7 | Digital output signals |
| 24 | GND 1 | Ground connection for output emitter follower |

**Figure 2**
**Block Diagram**

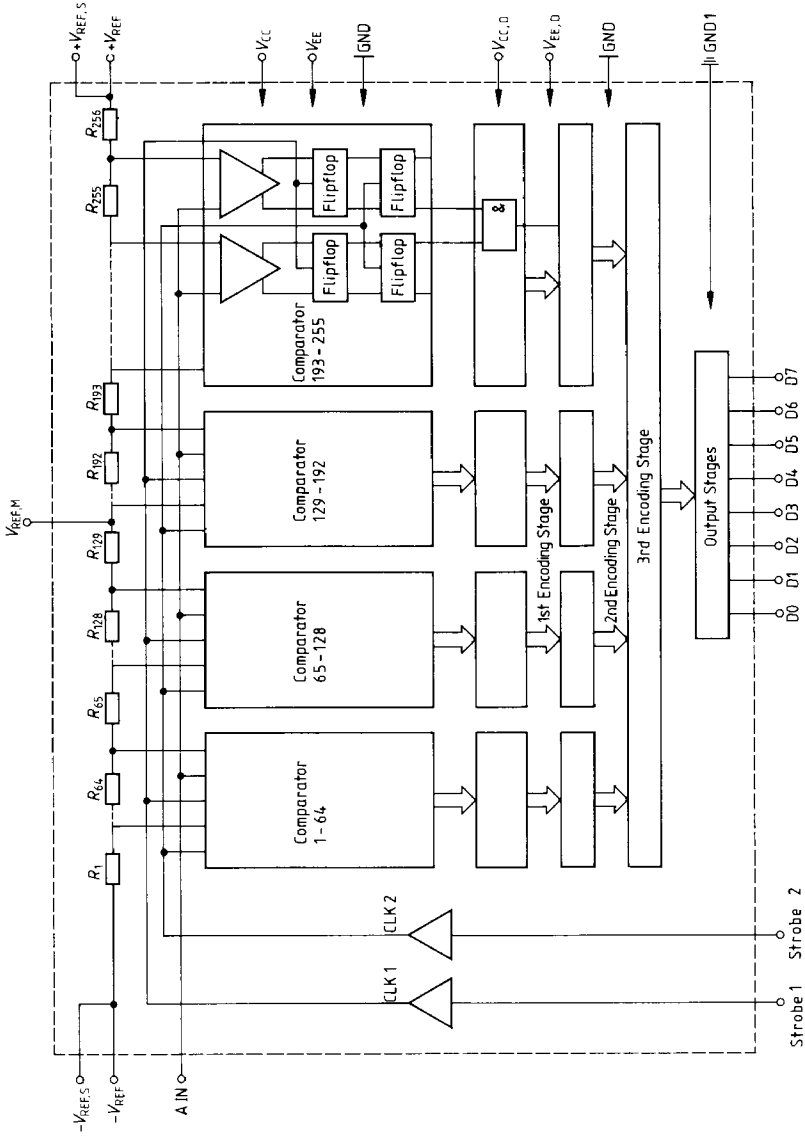
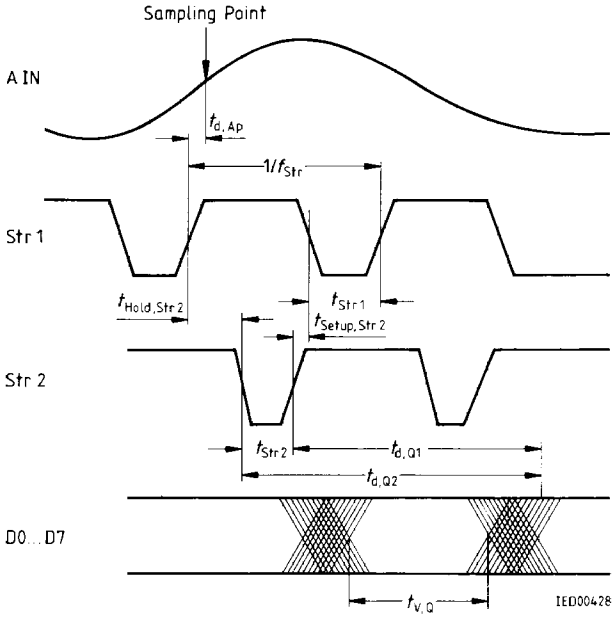


**Figure 3**
**Pulse Diagram**




**Strobe Timing**[1)]

| | min. | typ. | Unit |
|---|---|---|---|
| $t_{Str\ 1}$ | 4 | 5 | ns |
| $t_{Str\ 2}$ | 3 | 3.5 | ns |
| $t_{Set\ up,\ Str\ 2}$ | $-2.0$[2)] | $-1.5$[2)] | ns |
| $t_{Hold,\ Str\ 2}$ | 2 | 3 | ns |

1) This is recommended strobe setting for operation at 100 MHz. At lower strobe frequencies the timing becomes more and more uncritical. Below 75 MHz complementary strobe signals with a duty cycle of 50% may be used.

2) Negative values of $t_{Setup,\ Str\ 2}$ indicate that the rising edge of Str 2 should appear after the falling edge of Str 1.

## Absolute Maximum Ratings

| Parameter | Symbol | Limit Values min. | Limit Values max. | Unit |
|---|---|---|---|---|
| Pos. supply voltage | $V_{CC}$, $V_{CC,\,D}$ | −0.3 | 6.0 | V |
| Neg. supply voltage | $V_{EE}$, $V_{EE\,D}$ | −6.0 | 0.3 | V |
| Reference voltage[1]) | $+V_{REF}$, $V_{REF}$ | −2.5 | 1.5 | V |
| Analog input voltage | $V_{A\,IN}$ | −2.5 | 1.5 | V |
| Digital input voltage | $V_{Str\,1}$, $V_{Str\,2}$ | −3.5 | 0 | V |
| Output current | $I_{D0} \ldots I_{D7}$ | | 20 | mA |
| Junction temperature | $T_j$ | | 150 | °C |
| Ambient temperature (with heat sink) | $T_A$ | −25 | 50 | °C |
| Storage temperature | $T_{stg}$ | −25 | 125 | °C |
| Thermal resistance Junction – ambient (without heat sink) | $R_{th\,JA}$ | | 50 | K/W |

## Characteristics

$V_{CC}$, $V_{CC,\,D} = 5\ V \pm 5\%$, $V_{EE}$, $V_{EE}$, $V_{EE,\,D} = -4.5\ V \pm 5\%$, $T_j = 25\,°C$ to $125\,°C$

| Parameter | Symbol | Limit Values min. | Limit Values typ. | Limit Values max. | Unit |
|---|---|---|---|---|---|
| **Current Consumption** | | | | | |
| Pos. supply current, analog | $I_{CC}$ | | 95 | | mA |
| Pos. supply current, digital | $I_{CC,\,D}$ | | 85 | | mA |
| Total pos. supply current | $I_{CC} + I_{CC,\,D}$ | | 180 | 200 | mA |
| Neg. supply current, analog | $I_{EE}$ | | 70 | | mA |
| Neg. supply current, digital | $I_{EE,\,D}$ | | 20 | | mA |
| Total neg. supply current | $I_{EE} + I_{EE,\,D}$ | | 90 | 100 | mA |
| Power dissipation | $P_D$ | | 1.3 | 1.5 | W |
| Permissible supply voltage difference | $\Delta V_{CC}$, $\Delta V_{EE}$ | | | 100 | mV |
| **Reference Inputs** | | | | | |
| Reference voltages[1]) | $+V_{REF}$, $-V_{REF}$ | −2 | | 1 | V |
| Total reference resistance | $R_{REF}$ | 105 | 150 | 190 | Ω |
| Temperature coefficient of reference resistor | $TC$ | | $3 \times 10^{-3}$ | | 1/K |
| **Analog Input** | | | | | |
| Voltage range | $V$ | −2 | | 1 | V |
| Input current[2]) $V_{AIN} \geq +V_{REF}$ | $I_I$ | 150 | | 700 | µA |
| $V_{AIN} \leq -V_{REF}$ | $I_I$ | | | 1 | µA |
| Input capacitance $V_{AIN} \geq +V_{REF}$ | $C_{AIN}$ | | 45 | | pF |
| $V_{AIN} \leq -V_{REF}$ | $C_{AIN}$ | | 55 | | pF |

For comments see two pages hereafter.

**Characteristics** (cont'd)

$V_{CC}$, $V_{CC,\,D}$ = 5 V ± 5%, $V_{EE}$, $V_{EE,\,D}$ = −4.5 V ± 5%; $T_j$ = 25 °C to 125 °C

| Parameter | Symbol | Limit Values min. | typ. | max. | Unit |
|---|---|---|---|---|---|
| **Strobe Inputs** | | | | | |
| H-input voltage | $V_{IH}$ | −1.165 | | | V |
| L-input voltage | $V_{IL}$ | | | −1.475 | V |
| Max. strobe frequency | $f_{Str}$ | 100 | 125 | | MHz |
| H-input current $V_{Str} = V_{IH}$ | $I_{IH}$ | 2 | | 30 | µA |
| L-input current $V_{Str} = V_{IL}$ | $I_{IL}$ | | | 40 | nA |
| Aperture delay | $t_{d,\,ap}$ | | 1 | | ns |
| Aperture jitter | $t_{jit}$ | | 15 | | ps |
| **Data Outputs** | | | | | |
| H-output voltage (100-Ω resistor to −2 V) | $V_{QH}$ | −1.025 | | −0.880 | V |
| L-output voltage (100-Ω resistor to −2 V) | $V_{QL}$ | −1.810 | | −1.620 | V |
| Signal transition time[3] | $t_{d,\,Q1}$ | | | 10.5 | ns |
| | $t_{d,\,Q2}$ | | | 14 | ns |
| Time of valid output data[4] $f_{Str}$ = 100 MHz | $t_{V,\,Q}$ | 4 | 6 | | ns |
| **Conversion Characteristics** | | | | | |
| **Static Nonlinearity**[5] | | | | | |
| Integral nonlinearity $\Delta V_{REF}$ = 1.8 V | *I NL* | | | 0.5 | LSB |
| Differential nonlinearity $\Delta V_{REF}$ = 1.8 V | *D NL* | | 0.5 | 0.6 | LSB |
| **Dynamic Performance**[6] | | | | | |
| Large signal bandwidth | $f_{3\,dB}$ | 80 | | | MHz |
| Signal-to-noise ratio | | | | | |
| $f_{an}$ = 30 MHz | *SNR* | 40 | 43 | | dB |
| $f_{an}$ = 45 MHz | *SNR* | | 35 | | dB |
| Total harmonic distortion | | | | | |
| $f_{an}$ = 30 MHz | *THD* | | −43 | | dB |
| $f_{an}$ = 45 MHz | *THD* | | −30 | | dB |
| Effective bits | | | | | |
| $f_{an}$ = 1 MHz | $N_{eff}$ | | 7.4 | | bit |
| $f_{an}$ = 30 MHz | $N_{eff}$ | 6.0 | 6.3 | | bit |
| $f_{an}$ = 45 MHz | $N_{eff}$ | | 4.5 | | bit |

For comments see next page.

**Comments**

1) $+V_{REF}$ must always be more positive than $-V_{REF}$.
2) The input current is linearly dependent on the input voltage.
3) Delay from the rising edge ($t_{d, Q1}$) or falling edge ($t_{d, Q2}$) of Str2 to the beginning of validity of the associated output data.
4) Time interval, during which the conversion of a 30 MHz/2 $V_{pp}$ signal at 100 MHz sampling rate yields an *SNR* of more than 40 dB.
5) The actual transfer characteristic is measured by means of the servo loop principle at both low sampling rates (100 kHz) and slow strobe edges (> 500 ns).
6) Dynamic measurements are performed at 100 MHz sampling rate using the typical strobe timing. All specified parameters are derived from the FET of the converter's response to a full scale (2 $V_{pp}$) sine wave input. The analog source impedance is 25 Ω (50-Ω line with 50-Ω termination). The test circuit is shown in **figure 5.**

**Figure 4**
**Transfer Characteristic and Truth Table**

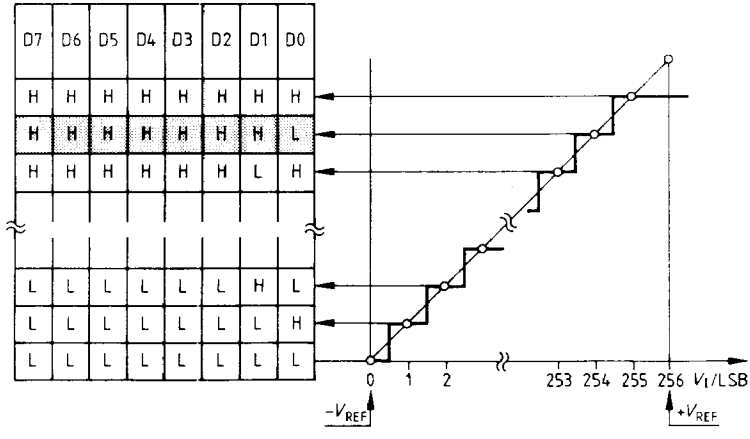


**Figure 5**
**Test Circuit**

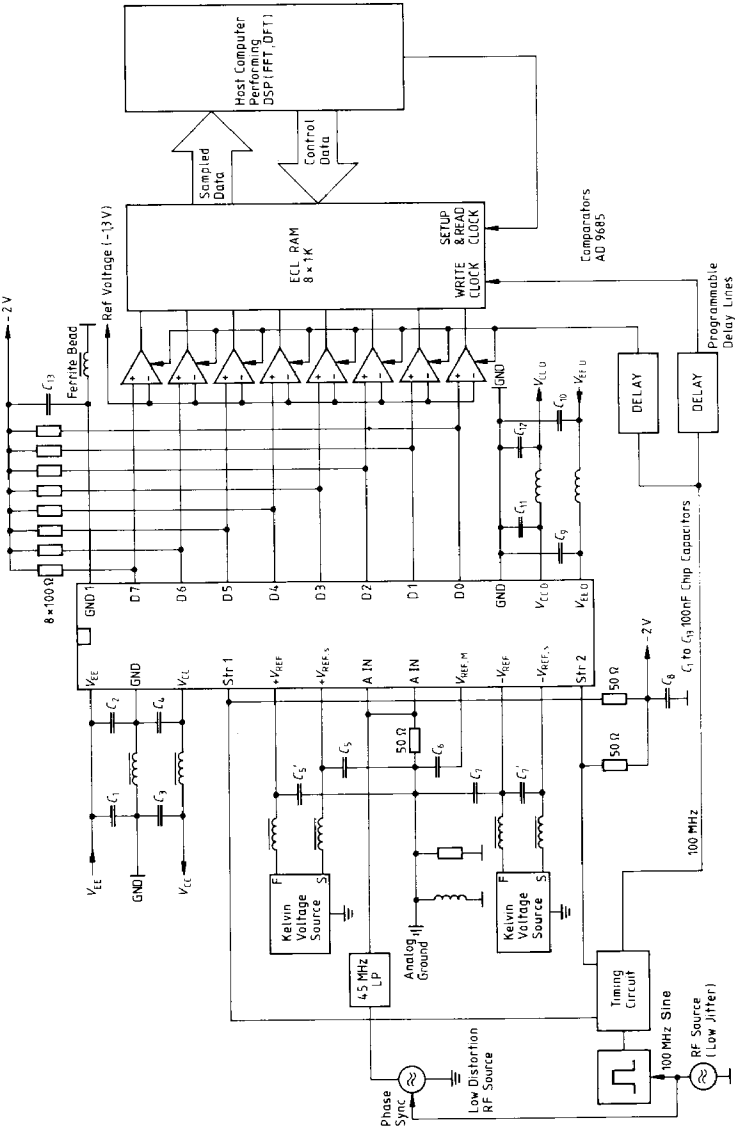


**Figure 6**
**Analog Input Capacitance versus Input Bias Voltage**
($+V_{REF} = 1$ V; $-V_{REF} = -1$ V)

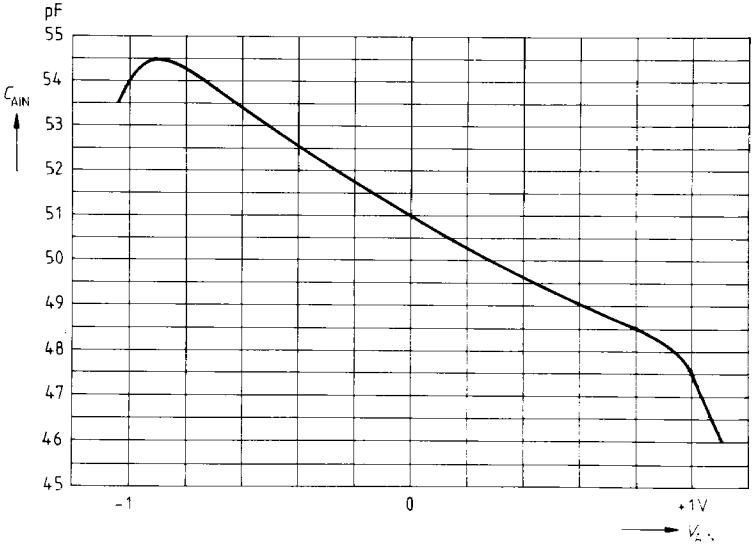



**Figure 7**
**Signal Transition Time $t_{d,Q1}$ and Valid Data Range $t_{V,Q}$ versus Junction Temperature**

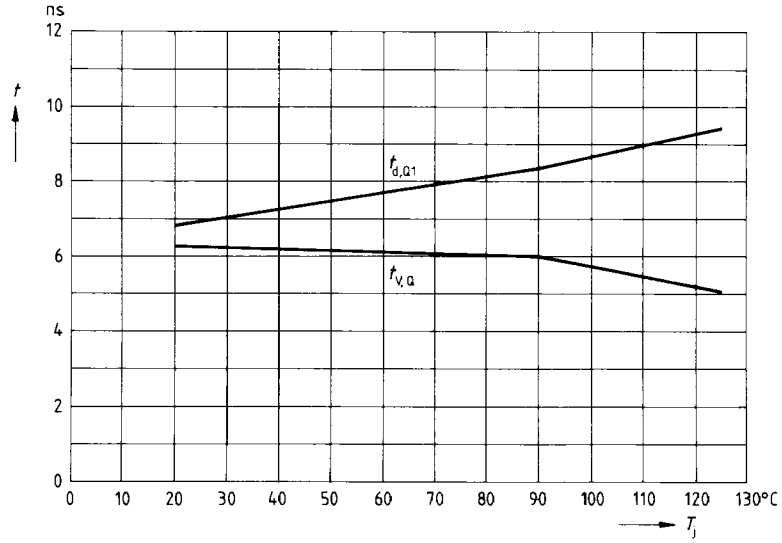


**Figure 8**
**Amplitude Response versus Analog Frequency**
a) including voltage drop across source impedance (25 Ω)
b) without voltage drop across source impedance (25 Ω)

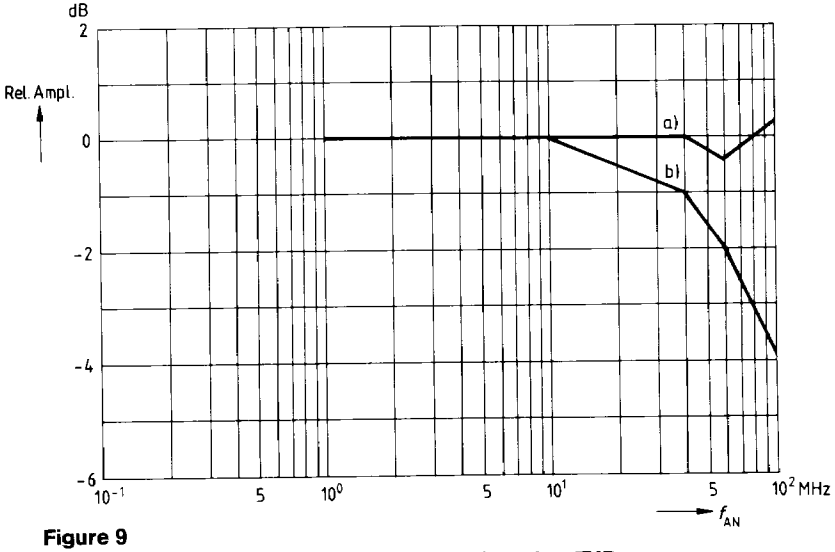



**Figure 9**
**Signal-to-Noise-Ratio *SNR* and Harmonic Distortion *THD* versus Analog Frequency**

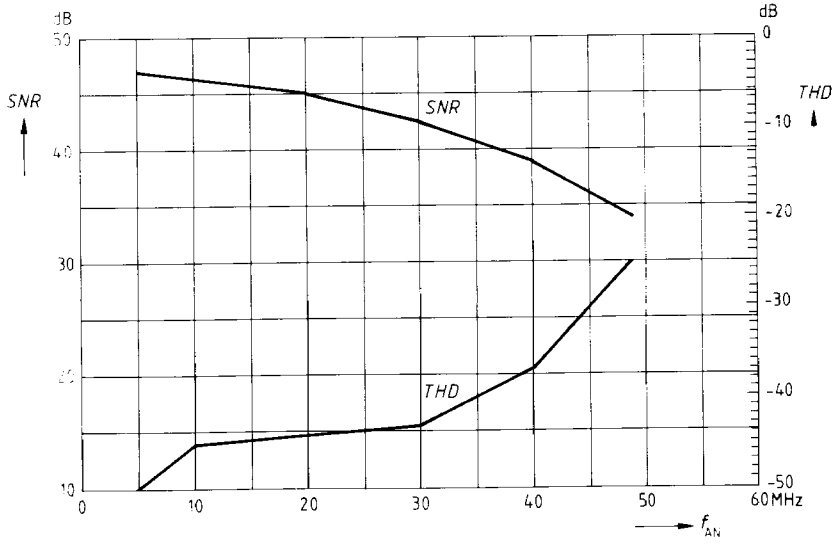


**Figure 10**
**Effective Resolution $N_{eff}$ versus Analog Frequency**