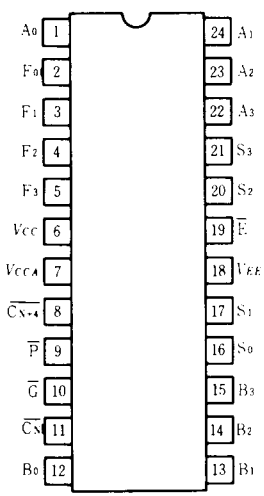
4-bit Binary/BCD ALU

The HD100181 performs eight logic operations and eight arithmetic operations on a pair of 4-bit words. The operating mode is determined by signals applied to the Select (Sn) inputs, as shown in the Function Select table. In addition to performing binary arithmetic, the circuit contains the necessary correction logic to perform BCD addition and subtraction. Output latches are provided to reduce overall package count and increase system operating speed. When the latches are not required, leaving the Enable ($\overline{E}$) input open makes the latches transparent.

The circuit uses internal lookahead carry to minimize delay to the F outputs and to the ripple Carry Output, $\overline{Cn+4}$. Group carry lookahead Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are also provided, which are independent of the carry In $\overline{Co}$. The $\overline{P}$ output goes low when a plus operation produces fifteen (nine for BCD) or when a minus operation produces zero. Similarly, $\overline{G}$ goes low when the sum of A and B is greater than fifteen (nine for BCD) in plus mode, or when their difference is greater than zero in a minus mode.

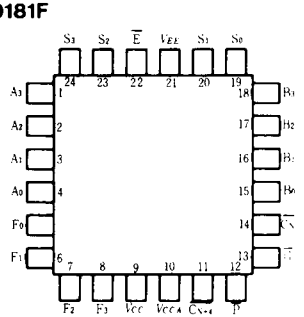
■PIN ARRANGEMENT

● HD100181



(Top View)

● HD100181F

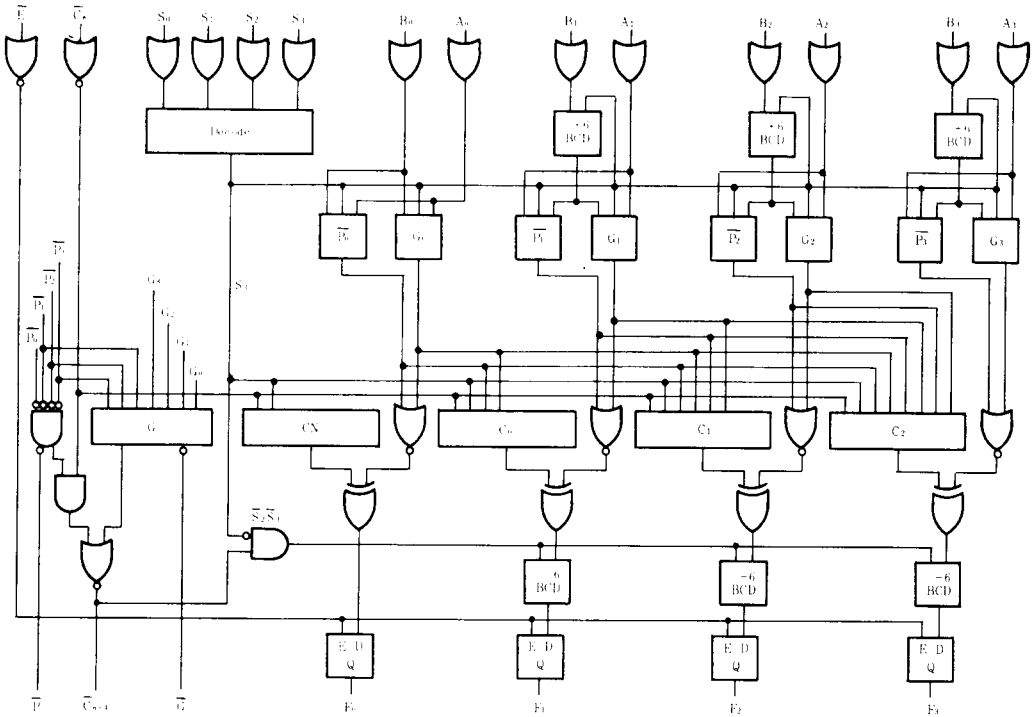


(Top View)

■FUNCTION SELECT TABLE

S_3	S_2	S_1	S_0	Function
L	L	L	L	A plus B BCD
L	L	L	H	A minus B BCD
L	L	H	L	B minus A BCD
L	L	H	H	0 minus B BCD
L	H	L	L	A plus B Binary
L	H	L	H	A minus B Binary
L	H	H	L	B minus A Binary
L	H	H	H	0 minus B Binary
H	L	L	L	$Fn = AnBn + \overline{An}\overline{Bn}$
H	L	L	H	$Fn = An\overline{Bn} + \overline{An}Bn$
H	L	H	L	$Fn = An + Bn$
H	L	H	H	$Fn = An$
H	H	L	L	$Fn = \overline{Bn}$
H	H	L	H	$Fn = Bn$
H	H	H	L	$Fn = AnBn$
H	H	H	H	Fn = Low

■LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		135	195	270	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	S_n, $\overline{E}$ input	—	—	350	μA
			Other inputs	—	—	250	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100181

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$\overline{C_n}$→F_n	1.50	5.00	1.60	3.00	5.20	1.60	5.40	ns
			$\overline{C_n}$→$\overline{C_{n+1}}$	1.10	2.80	1.30	1.80	3.00	1.30	3.00	
			A_n, B_n→$\overline{P}$, $\overline{G}$	1.30	3.80	1.40	2.50	3.90	1.40	3.90	
			S_n→$\overline{P}$, $\overline{G}$	1.80	4.90	2.00	3.50	5.10	2.00	5.40	
			A_n, B_n→$\overline{C_{n+1}}$	2.00	5.00	2.00	3.50	5.10	2.10	5.30	
			S_n→$\overline{C_{n+1}}$	2.70	6.50	2.80	4.00	6.75	2.80	6.90	
			A_n, B_n→F_n	2.10	6.20	2.10	4.00	6.20	2.20	6.40	
			S_n→F_n	1.30	6.20	1.50	4.00	6.50	1.50	6.90	
			$\overline{E}$→F_n	0.90	2.50	1.00	1.50	2.50	1.00	2.50	
Transition Time	t_{THL}, t_{TLH}			0.45	3.60	0.45	1.00	3.50	0.45	3.60	ns
Setup Time	t_{SU}	A_n, B_n→$\overline{E}$		5.20		5.50			6.00		ns
		S_n→$\overline{E}$		6.00		6.00			6.50		
		$\overline{C_n}$→$\overline{E}$		4.30		4.50			4.80		
Hold Time	t_h	A_n, B_n→$\overline{E}$		0.10		0.10			0.10		ns
		S_n→$\overline{E}$		0.60		0.60			0.60		
		$\overline{C_n}$→$\overline{E}$		0.60		0.60			0.60		
Pulse Width	$t_{W(L)}$	$\overline{E}$		2.00		2.00			2.00		ns

● HD100181F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$\overline{C_n}$→F_n	1.50	4.80	1.60	3.00	5.00	1.80	5.50	ns
			$\overline{C_n}$→$\overline{C_{n+1}}$	1.25	2.50	1.35	1.80	2.80	1.35	2.90	
			A_n, B_n→$\overline{P}$, $\overline{G}$	1.30	3.40	1.40	2.20	3.70	1.60	3.90	
			S_n→$\overline{P}$, $\overline{G}$	1.90	4.80	2.00	2.80	5.00	2.20	5.80	
			A_n, B_n→$\overline{C_{n+1}}$	2.00	5.20	2.00	3.60	5.70	2.40	6.00	
			S_n→$\overline{C_{n+1}}$	2.70	6.40	2.80	4.50	6.75	3.00	7.40	
			A_n, B_n→F_n	2.00	6.00	2.10	4.50	6.30	2.30	6.80	
			S_n→F_n	1.30	7.00	1.50	5.00	7.20	1.70	7.80	
			$\overline{E}$→F_n	0.85	2.50	0.90	1.50	2.80	0.90	2.80	
Transition Time	t_{THL}, t_{TLH}			0.45	3.50	0.45	1.50	3.50	0.45	3.50	ns
Setup Time	t_{SU}	A_n, B_n→$\overline{E}$		7.00		7.40			8.20		ns
		S_n→$\overline{E}$		8.00		8.00			8.30		
		$\overline{C_n}$→$\overline{E}$		5.00		5.20			6.20		
Hold Time	t_h	A_n, B_n→$\overline{E}$		0.00		0.00			0.00		ns
		S_n→$\overline{E}$		0.50		0.50			0.30		
		$\overline{C_n}$→$\overline{E}$		0.50		0.50			0.20		
Pulse Width	$t_{W(L)}$	$\overline{E}$		2.00		2.00			2.00		ns

Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m s (500 linear fpm) is maintained.