Ordering number: EN 2301B

Monolithic Linear IC

SANYO No.2301B

LA5665

Multifunction Multiple Voltage Regulator

Use

- Especially suited for use in micorcomputer-controlled tuners, receivers, preamp and the like

Functions and Features

- Two independent voltage regulators contained in a single chip (15.5V/350mA, 5.6V/100mA)
- Reset circuit which delivers the reset signal on the positive transition, negative transition of the 5.6V output
- Muting circuit which detects the 15.5V output and reset output to deliver the muting signal
  (We have the LA5666 whose detection function for reset, muting is provided on the input voltage side.)

Maximum Ratings at Ta=25°C

				unit
Input Voltage	$V_{IN1,2}$		35	V
Output Current	$I_{OUT1,2}$	Internal		
Allowable Power Dissipation	Pdmax	IC only	1.6	W
Operating Temperature	Topr		-30 to +80	°C
Storage Temperature	Tstg		-40 to +125	°C

Operating Conditions at Ta=25°C

				unit
Input Voltage	V_{IN1}	I_{OUT1}=200mA	19 to 35	V
	V_{IN2}	I_{OUT2}=50mA	8.7 to 35	V

Operating Characteristics at Ta=25°C, V_{IN1}=20V, V_{IN2}=10V

			min	typ	max	unit
Quiescent Current	I_{IN1}		1.8	2.8	3.8	mA
	I_{IN2}		3.8	5.8	7.8	mA
Output Voltage	V_{o1}	I_{OUT1}=200mA	14.5	15.5	16.5	V
	V_{o2}	I_{OUT2}=50mA	5.1	5.6	6.2	V
Line Regulation	V_{ol1}	V_{IN2}=19 to 27V		6	20	mV
	V_{ol2}	V_{IN2}=9 to 18V		2	20	mV
Load Regulation	V_{old1}	Io=0 to 350mA		10	30	mV
	V_{old2}	Io=0 to 100mA		2	20	mV
Ripple Rejection	Rr1	f=120Hz, Io=200mA	56	65		dB
	Rr2	f=120Hz, Io=50mA	60	75		dB

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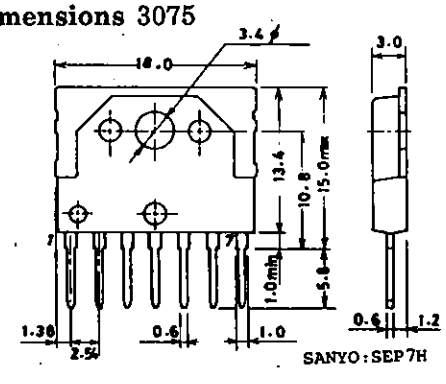
Package Dimensions 3075
(unit: mm)



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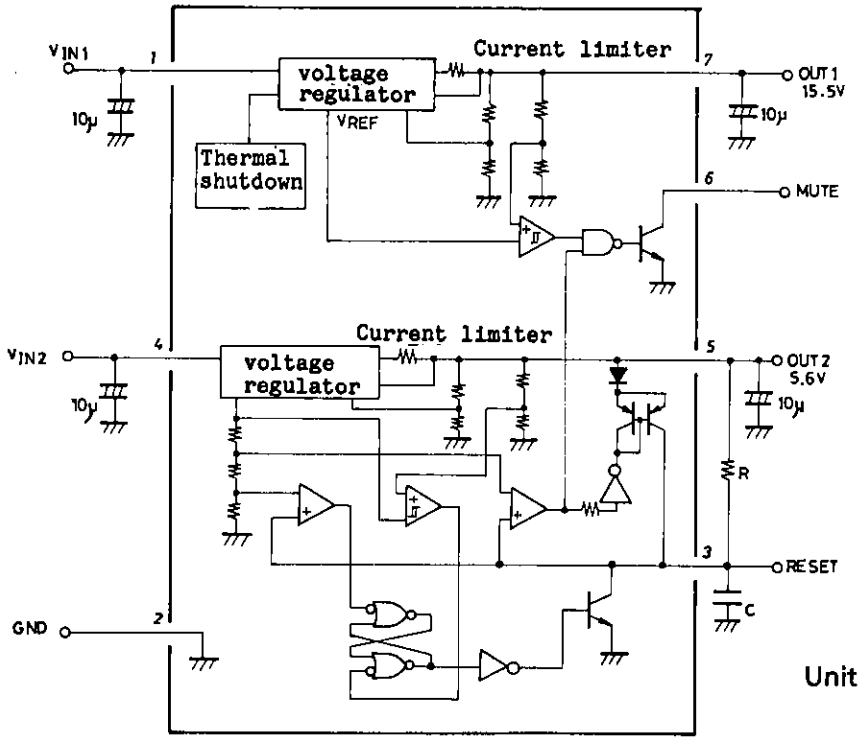
			min	typ	max	unit
Input-Output Voltage Drop	Vdr1	Io=200mA		1.6	2.5	V
	Vdr2	Io=50mA		1.5	2.5	V
Reset Detect Voltage	V_R	(Note 1)	4.9	5.1	5.5	V
Timer Compare Voltage	V_{C1}		1.0	1.2	1.4	V
	V_{C2}		0.06	0.13	0.18	V
Timer Input Bias Current	I_{TB}				250	nA
Muting Detect Voltage	V_M	(Note 2)	13.5	14.5	15.5	V
Muting Output Voltage	V_{OMUTE}	I_{OMUTE}=5mA		0.1	0.15	V

Note 1: V_R is the voltage of V_{O2} at the time reset is turned OFF.
Note 2: V_M is the voltage of V_{O1} at the time muting is turned OFF.

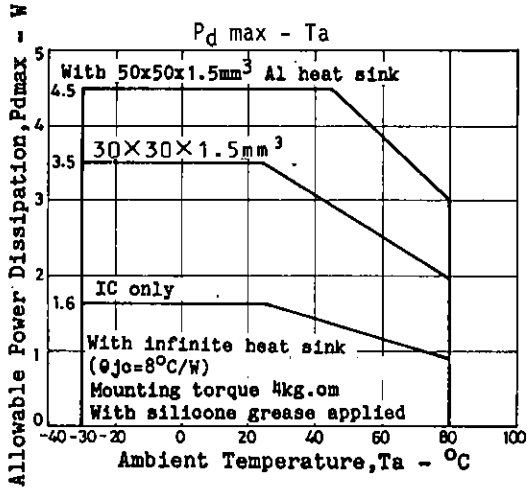
Equivalent Circuit Block Diagram, Pin Assignment, and Peripheral Circuit



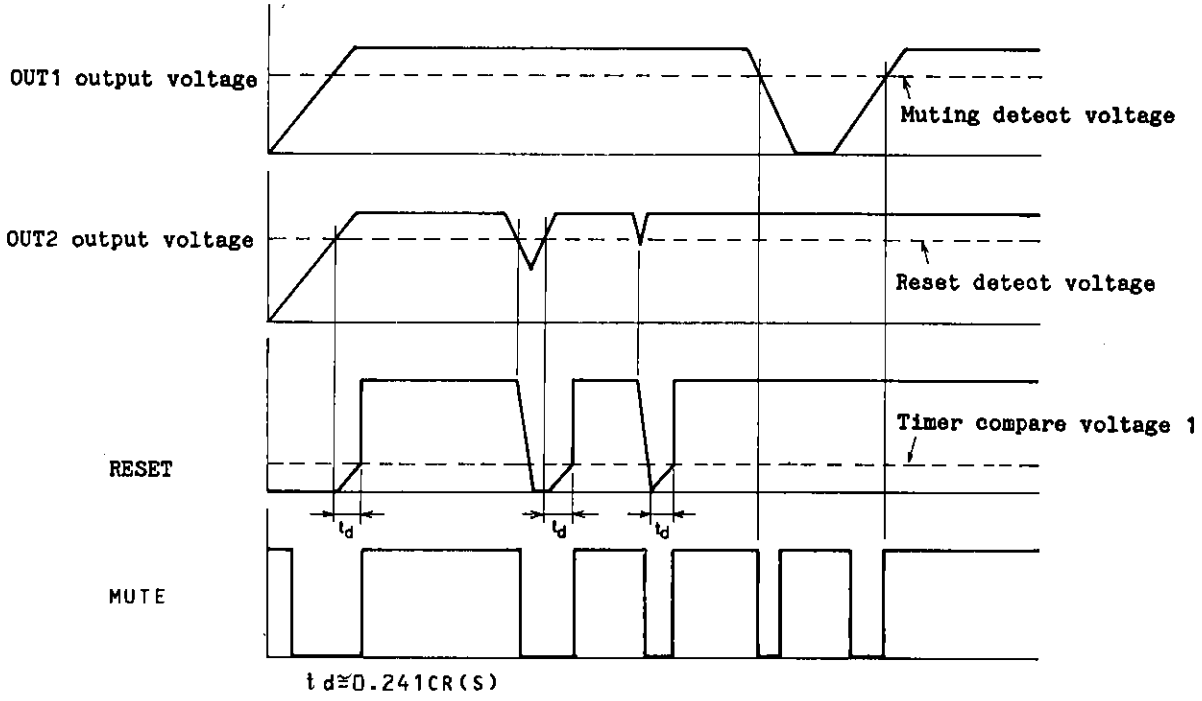
Unit (capacitance: F)

(Note) The reset delay time is set by R, C.

Pin No.	Name	Description
1	V_{IN1}	Input pin for 15.5V output line
2	GND	Ground
3	RESET	Reset delay time and output pin
4	V_{IN2}	Input pin for 5.6V output line
5	OUT2	5.6V output pin
6	MUTE	Muting signal output pin
7	OUT1	15.5V output pin



Operating Waveforms



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