NT6828

I²C Bus Controlled On-Screen Display

Features

- I²C Bus Interface with Slave Address $7A (Receiver Only)
- Horizontal Frequency Range: 30KHz ~ 120KHz
- Flexible Display Resolution: up to 1524 dots per row
- Internal PLL Generating a Stable and Wide-Ranged System Clock (92.2 MHz)
- OSD Screen Comprising of Character Arrays of 15 Rows by 30 Columns
- 12 X 18 Dot Matrix Per Character
- Total of 256 Fonts Including 248 ROM Fonts and 8 RAM Fonts
- Programmable Vertical and Horizontal Position Adjustment for OSD Display Position
- 8-Color Selection for Each Character and 8-Color Control on Each Row with Overlapped by Windows
- Character Blinking, Shadowing & Bordering Display Effects
- Double Character Height and Width for Each Row
- Programmable Height of Characters Display
- Row To Row Spacing Control
- Four Overlapping and Programmable Windows with 8-Color Control
- Hsync & Vsync Input Polarity Selectable
- 8 Channels PWM DAC with 8 bits resolution & Open-Drain Output Structure
- 16 DIP and 24 Skinny DIP packages

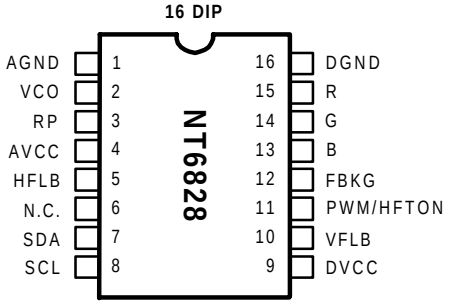
General Description

NT6828 is designed for displaying symbols and characters onto a CRT monitor. Its operation is controlled by the micro-controller with I2C bus interface. By sending the proper data and commands to NT6828, it can carry out the full screen display automatically while the time base is generated by the on-chip PLL circuit. There are many functions provided on this chip to fully support numerous user applications. These functions are: adjustment of OSD windows position, built-in ROM & RAM fonts, variable character height with row-to-row spacing adjustment, 8 color selections for each character, double height/width controls for each row, four available overlapping windows with color & size controls, as well as other I/O interfaces to compliment an external video chipset.

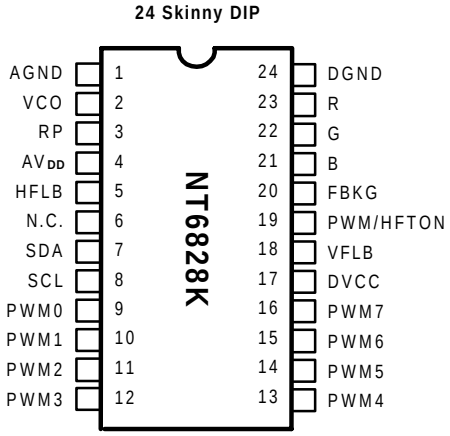
NT6828 provides eight optional PWM channels with 8-bit resolution for external digital to analog control.

Pin Configurations

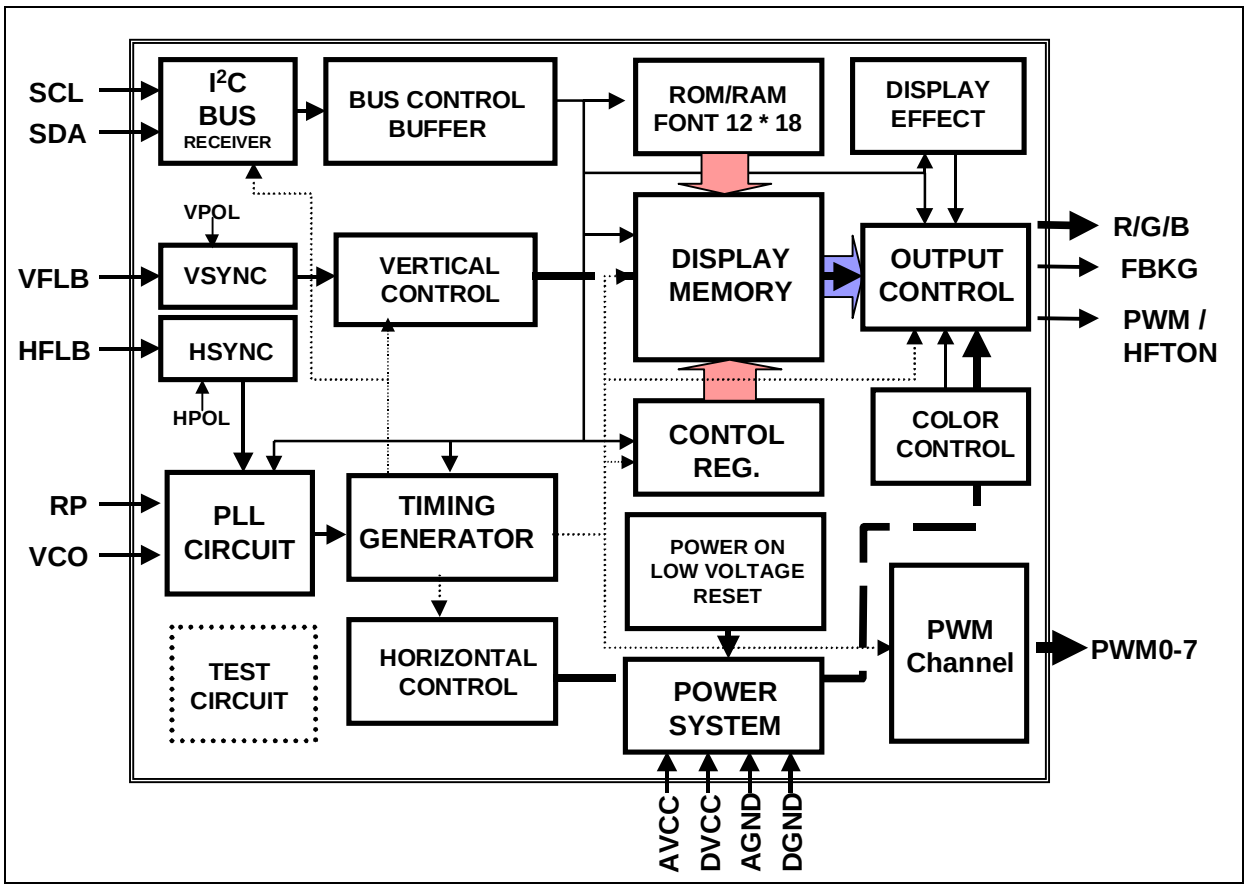
16 DIP



24 Skinny DIP



Block Diagram

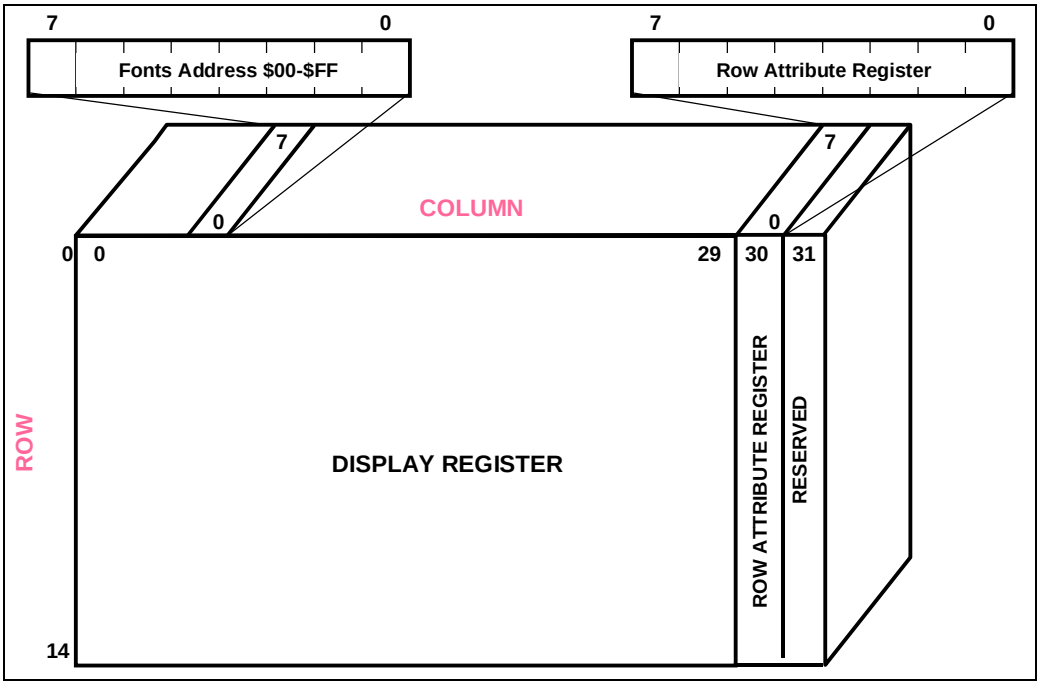


Pin Description

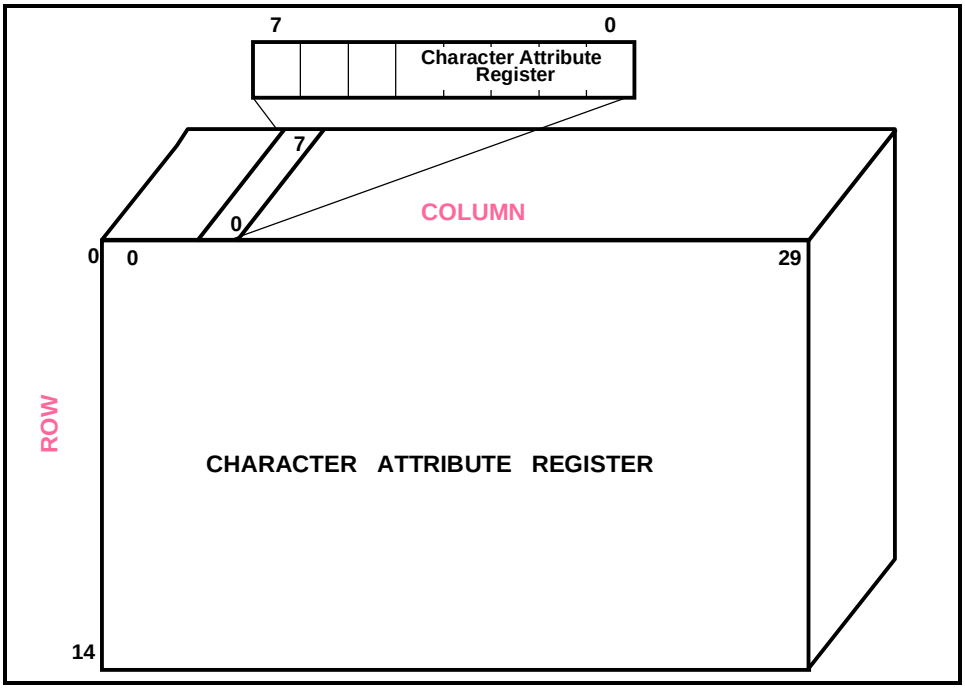
Pin No.		Designation	I/O/P/R	Description
16 Pin	24 Pin			
1	1	AGND	P	Analog Ground
2	2	VCO	-	Voltage I/P to Control Oscillator
3	3	RP	-	Bias Resistor. (To be used as a bias internal VCO to resonate at the specific range of pixel clock)
4	4	AVCC	P	Analog Power Supply (5V Typ.)
5	5	HFLB	I	Horizontal Fly-back Input (Schmitt Trigger Buffer)
6	6	N.C.	-	-
7	7	SDA	I	SDA Pin Of I^2C Bus (Schmitt Trigger Buffer) with internal 100K ohm pulled-high resistance
8	8	SCL	I	SCL Pin Of I^2C Bus (Schmitt Trigger Buffer) with internal 100K ohm pulled-high resistance
	9	PWM0	O	5V PWM Channel 0. Open-drain output structure
	10	PWM1	O	5V PWM Channel 1. Open-drain output structure
	11	PWM2	O	5V PWM Channel 2. Open-drain output structure
	12	PWM3	O	5V PWM Channel 3. Open-drain output structure
	12	PWM4	O	5V PWM Channel 4. Open-drain output structure
	14	PWM5	O	5V PWM Channel 5. Open-drain output structure
	15	PWM6	O	5V PWM Channel 6. Open-drain output structure
	16	PWM7	O	5V PWM Channel 7. Open-drain output structure
9	17	DVCC	P	Digital Power Supply (5V Typ.)
10	18	VFLB	I	Vertical Fly-back Input (Schmitt Trigger Buffer)
11	19	PWM/ HFTON	O	PWM output or gain controlled of R,G,B channels.
12	20	FBKG	O	Fast Blanking Output. (To be used as switching signal for the R,G,B OSD video signals.)
13	21	B	O	Blue Color Output with Push-Pull Output Structure
14	22	G	O	Green Color Output with Push-Pull Output Structure
15	23	R	O	Red Color Output with Push-Pull Output Structure
16	24	DGND	P	Digital Ground

Functional Description

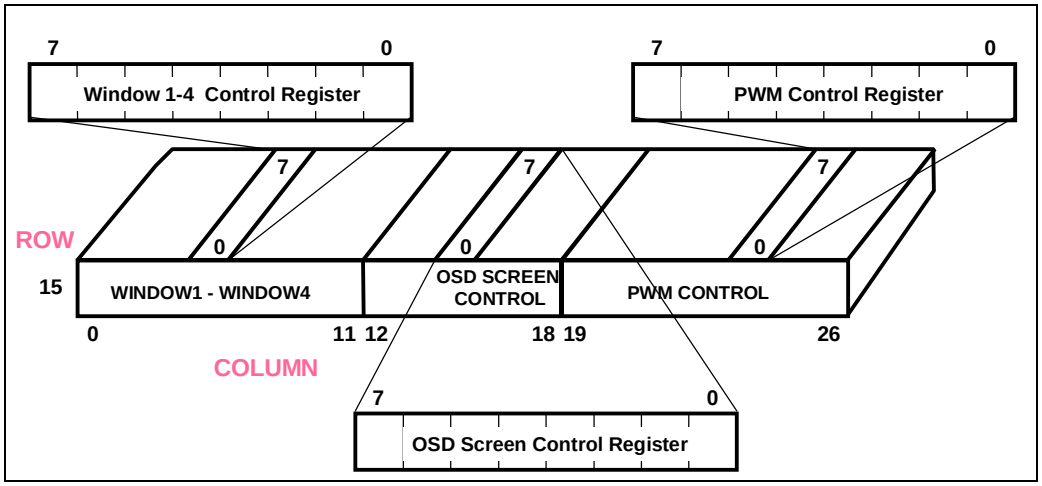
1. Memory Map



Memory Map of Display Register (Row 0 - 14)



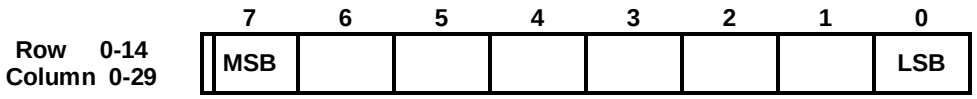
Memory Map of Attribute Register (Row 0 - 14)



Memory Map of Control Register (Row 15)

2. List of Control Registers:

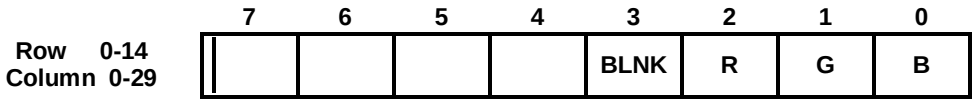
(1) Display Register: Row 0 - 14, Column 0 - 29



Fonts' Address $00 - $FF

Bit 7 - 0: In this eight bit address one of the 256 characters/symbols resided in the character ROM/RAM fonts. (Please refer to Figure 1.) Note that for 0 - 247 (ROM fonts) and 248 - 255 (RAM fonts) need to be programmed by the user. Each font consists of 12 x 18 dots matrix. (Please refer to Figure 2.)

(2) Character Attribute Register: Row 0 - 14, Column 0 - 29



Characters' Attribute Control

Bit 3: BLNK- This bit is to enable the blinking effect of the corresponding character/symbol as the bit is set to '1'. The blinking frequency is approximately 1Hz with 50/50 duty cycle at 80Hz vertical sync frequency.

Bit 2 - 0: R/G/B-These three bits define the color attributes of the corresponding character/symbol. (Please refer to Table 1 for the color selections.)

Table 1. Character/Windows Color Selection

COLOR	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

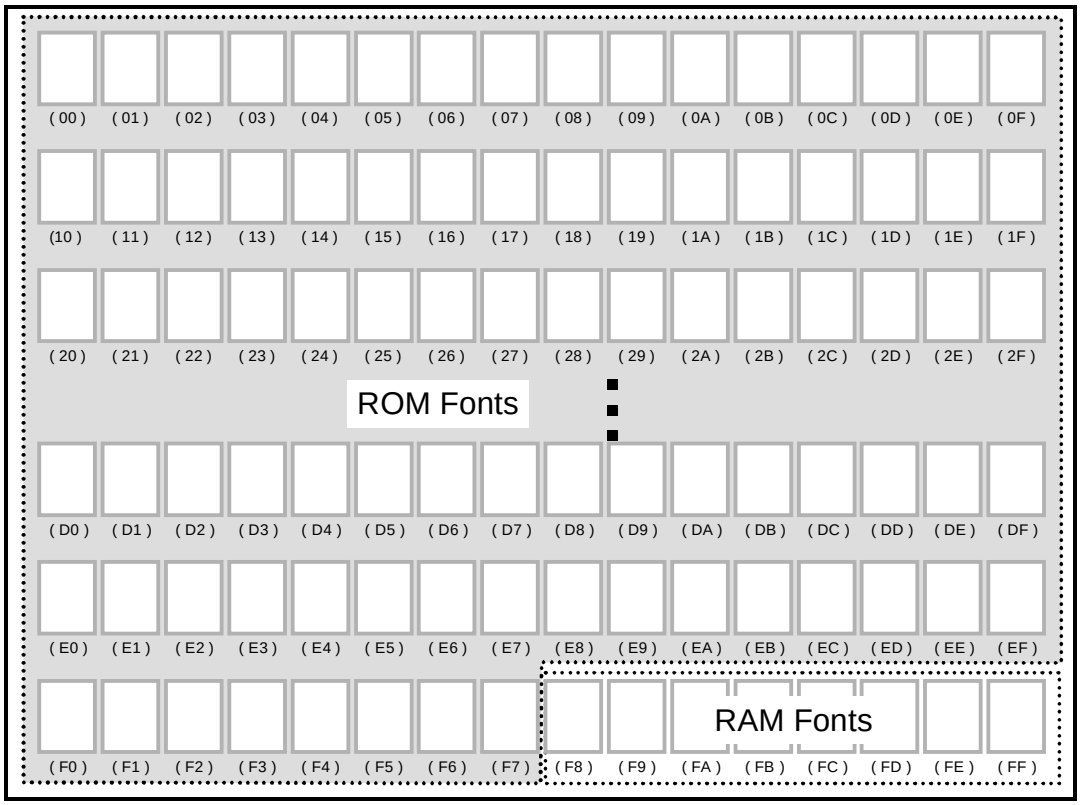


Figure 1. Font Configuration

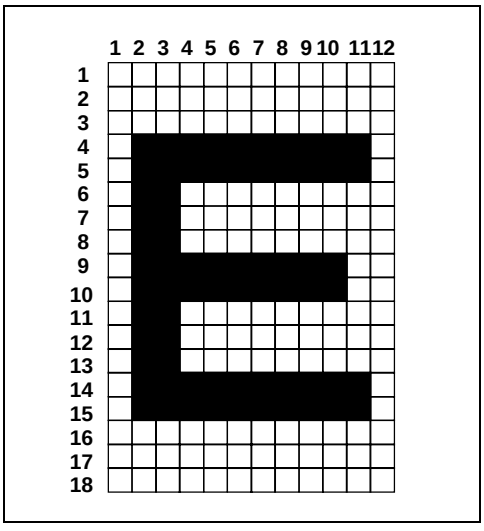
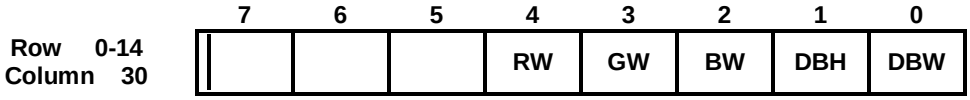


Figure 2. 12 x 18 Dots Matrix Font

(3) Row Attribute Register: Row 0 - 14, Column 30



Rows' Attribute Control

Bit 4 - 2: RW/GW/BW- These three bits define the color attributes of the corresponding character/symbol at each row when overlapped by window and its control bit $\overline{\text{ROW}}$ cleared to '0'. (Please refer to Table 2 for the color selections.)

Bit 1: DBH- This bit controls the height of the displayed character/symbol. When this bit is set, the character/symbol is displayed in double height. (Please refer to Figure 3.)

Bit 0: DBW- This bit controls the width of the displayed character/symbol. When this bit is set, the character/symbol is displayed in double width. (Please refer to Figure 3.)

Table 2. Character/Windows Color Selection

COLOR	RW	GW	BW
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

(4) Window 1 Registers: Row 15, Column 0

	7	6	5	4	3	2	1	0
Row 15 Column 0	Row Start Address MSB LSB				Row End Address MSB LSB			

Window 1 Row Size Control

Bit 7 - 4: These bits determine the row start position of window 1on the 15 x 30 OSD screen. (Please refer to Figure 4.)

Bit 3 - 0: These bits determine the row end position of window 1on the 15 x 30 OSD screen. (Please refer to Figure 4.)

	7	6	5	4	3	2	1	0
Row 15 Column 1	Column Start Address MSB LSB					WINEN	ROW_	

Window1 Column Size Control & Attribute Control

Bit 7 - 3: These bits determine the column start position of window 1on the 15 x 30 OSD screen. (Please refer to Figure 4.)

Bit 2: WINEN- This bit enables the window 1 as it is set.

Bit 1: $\overline{\text{ROW}}$ - This bit determines the row color attributes of the characters, which is overlapped by this window. Clear this bit to enable the row color attributes set by the control bit2~4 at the control registers at row 0 - 14, column 30.

	7	6	5	4	3	2	1	0
Row 15 Column 2	Column End Address MSB LSB					R	G	B

Window1 Column Size Control & Attribute Control

Bit 7 - 3: These bits determine the column end position of window 1on the 15 x 30 OSD screen. (Please refer to Figure 4.)

Bit 2 - 0: R/G/B- These bits control the background color of window 1. Please refer to the Table for color selection.

Note: Window 1 control registers occupy column 0 - 2 of row 15, Window 2 from column 3 - 5, Window 3 from 6 - 8 and Window 4 from 9 - 11. The function of Window 2 - 4 control registers is the same as Window 1. Window 1 has the highest priority, whereas Window 4, the least whereas window with higher priority will overlap window with lower if their display area have overlapped. The higher priority color will take occupy the overlapping window area.

If the start address of the row/column is greater than the end address then this window will not be displayed.

Set out of 15 Row & 30 Column OSD display range , the abnormal OSD screen will be displayed.

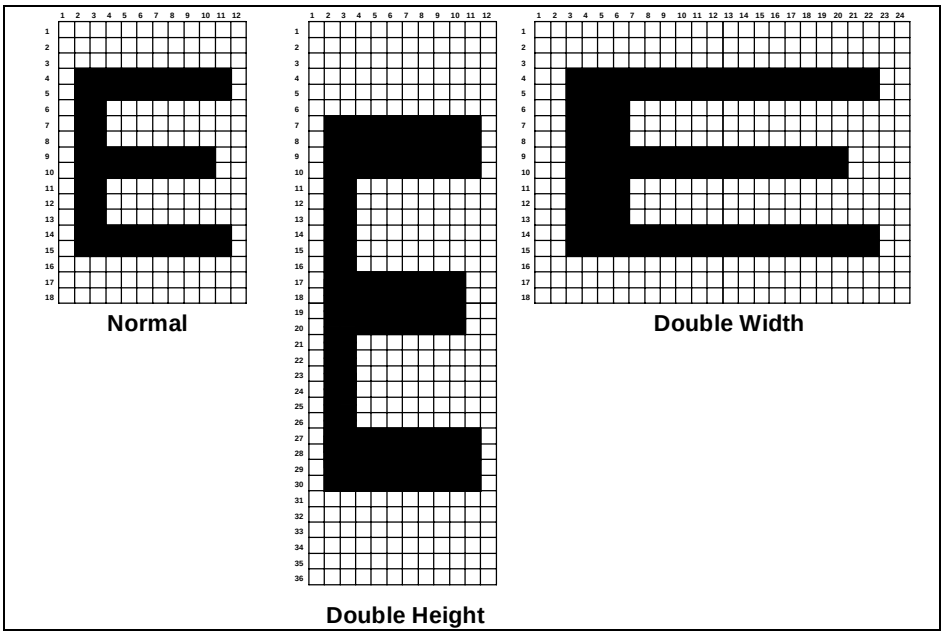


Figure 3. Double Height & Width Effect

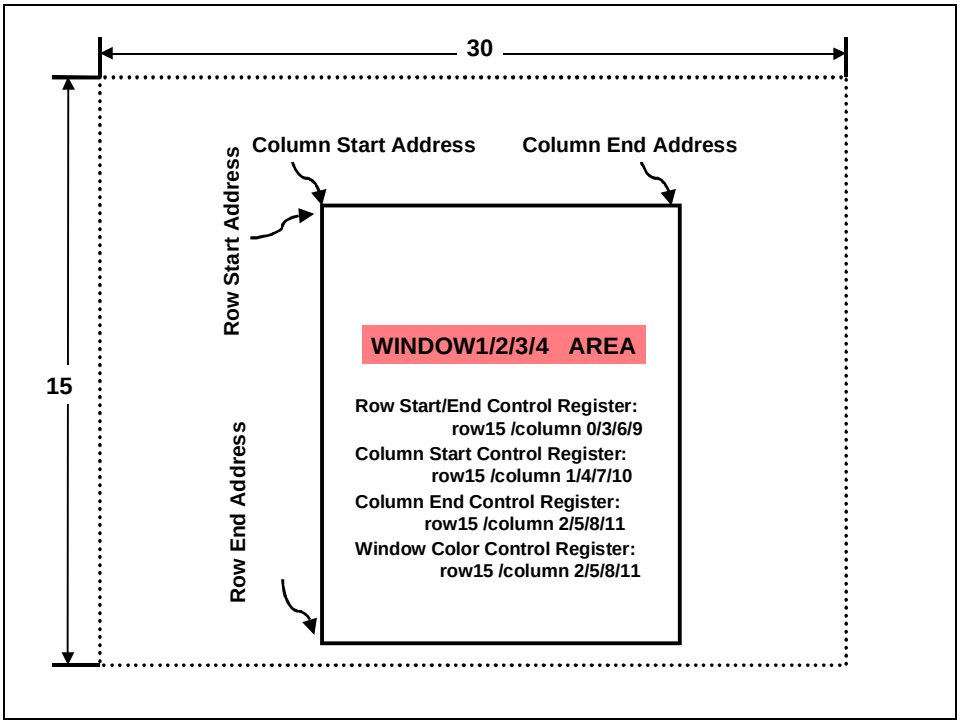


Figure 4. Windows' Size Setting

(5) OSD Screen Position Control Registers: Row 15, Column 12 - 13

	7	6	5	4	3	2	1	0
Row 15 Column 12	VPOS							
	MSB							LSB

Vertical Position Adjustment

Bit 7 - 0: VPOS - These bits determine the vertical starting position for the OSD screen display. It is the vertical delay starting from the leading edge of VFLB. The unit of this setting is 4 horizontal lines.
The equation is defined as:

Vertical delay = (Vpos x 4 +1) x Horizontal Line

The default value of it is 4 ($04) after power on. Please refer Figure 5.

	7	6	5	4	3	2	1	0
Row 15 Column 13	HPOS							
	MSB							LSB

Horizontal Position Adjustment

Bit 7 - 0: HPOS- These bits determine the horizontal starting position for the OSD screen display. It is the horizontal delay starting from the leading edge of HFLB. The unit of this setting is a 6-dot movement shift to the right on the monitor screen. The equation is defined as:

Horizontal delay = (Hpos x 6 + 49) / P.R.

Where the P.R. (pixel rate) is defined by the HDR & Horizontal Frequency.

P.R. (Pixel Rate) = HDR * 12 * FreqHFLB

Please refer to the HDR control register at row15 / column15 for the P.R. setting.
After power-on, the default value of these bits is 15 ($ 0F). (Please refer to Figure 5.)

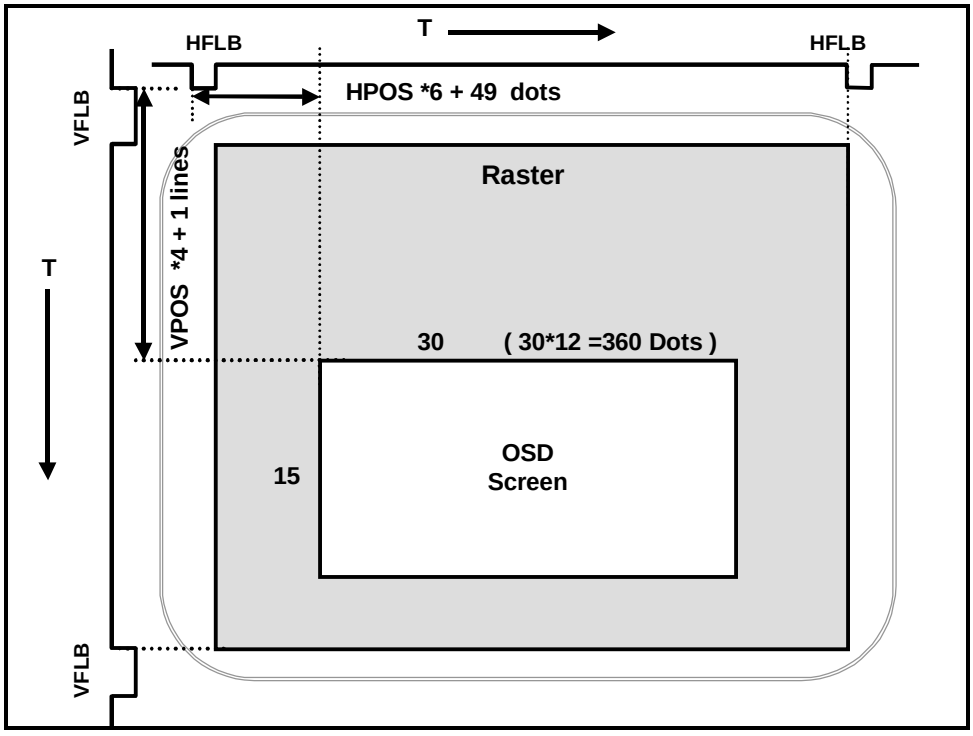


Figure 5. OSD Screen Position

Note: The figure above illustrates the positions adjustment of all displayed characters on the screen relative to the leading edge of horizontal and vertical fly-back signals.

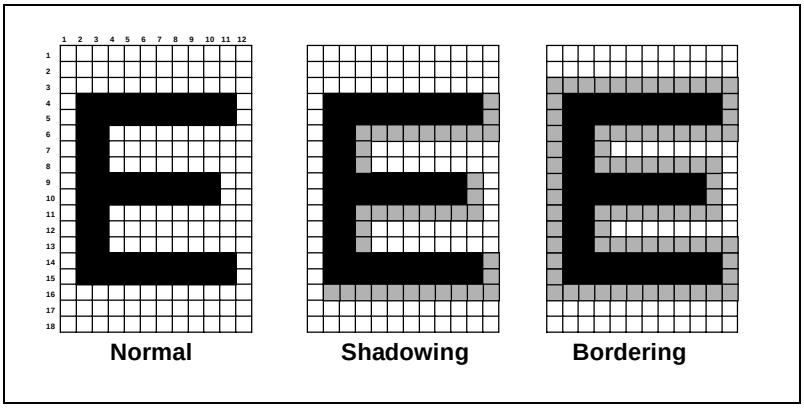


Figure 6. Shadowing & Bordering Effects

(6) Character Height Control: Row 15, Column 14

	7	6	5	4	3	2	1	0
Row 15 Column 14		CRH6	CRH5	CRH4	CRH3	CRH2	CRH1	CRH0

Characters' Height Control

Bit 6 - 0: CRH6-CRH0- These bits determine the displayed characters' height. The characters, originally 12 x 18 font matrix, can be expanded from 18 to 71 lines. (Please refer to Table 3 & 4 below.)

Table 3. Lines Expanded Control

CRH6 - CRH0	Lines Inserted
CRH6 = ' 1 ' , CRH5 = ' 1 '	All 18 lines repeat three times
CRH6 = ' 1 ' , CRH5 = ' 0 '	All 18 lines repeat twice
CRH6 = ' 0 ' , CRH5 = ' X '	All 18 lines repeat once
CRH4 = ' 1 '	Insert 16 lines
CRH3 = ' 1 '	Insert 8 lines
CRH2 = ' 1 '	Insert 4 lines
CRH1 = ' 1 '	Insert 2 lines
CRH0 = ' 1 '	Insert 1 lines

Table 4. Lines Expanded Position

No. of Lines Inserted	Repeat Position																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Insert 1 lines									!									
Insert 2 lines					!								!					
Insert 4 lines			!				!				!				!			
Insert 8 lines		!		!		!		!		!		!		!		!		
Insert 16 lines		!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	
Insert 17 lines	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	

Note: Please refer to Table 5, where there are listed examples for this line expanded algorithm.

Table 5. Line Expanded Example

Example 1: set CRH0 = 1, CRH2 = 1, CRH3 = 1

Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Original Font	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!
CRH0									!									
CRH2			!				!				!				!			
CRH3		!		!		!		!		!		!		!		!		
Result : 31 lines 18+ 8*CRH3+4*CRH2 +CRH0	!	!!	!!	!!	!	!!	!!	!!	!!	!!	!!	!!	!	!!	!!	!!	!	!

Example 2: set CRH0 = 1, CRH 3 = 1, CRH4 = 1

Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Original Font	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!
CRH0									!									
CRH3		!		!		!		!		!		!		!		!		
CRH4		!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	
Line >= 18	!																	!
Result : 45 lines 18+(18 * CRH4) + (8*CRH3)+(CRH0)	!!	!!!	!!	!!!	!!	!!!	!!	!!!	!!!	!!!	!!	!!!	!!	!!!	!!	!!!	!!	!!

(7) Flexible Display Control Register: Row 15, Column 15

Row 15, Column 15	7	6	5	4	3	2	1	0
		HDR						
		MSB						LSB

Horizontal Display Resolution Control

Bit 6 - 0: HDR- These bits determine the resolution of horizontal display line. The unit of this setting is 12 dots (1 character). With a total of 92, the user can adjust the resolution from 36 to 127 characters on each horizontal line steps ($24 - $7F: 36 - 127 steps; note that its value can not be smaller than 36 at any given time.) Also make a special note that the resolution adjustment must be joined together with the VCO setting at row15 / column18 control register. The default value is 40 after power-on.
(Please refer to the Table showing the control register at row15 / column18.)

(8) OSD Row to Row Space Control Register: Row 15, Column 16

Row 15, Column 16	7	6	5	4	3	2	1	0
				R2RSPACE				
				MSB				LSB

Row To Row Space Adjustment

Bit 4 - 0: R2RSPACE- These bits define the row to row spacing in unit of horizontal line. It means extra lines, defined by this 5-bit value, will be appended for each display row. The default value of it is 0 after power-on and there is no any extra line inserted between each row.

(9) Input/Output Control Register: Row 15, Column 17

Row 15, Column 17	7	6	5	4	3	2	1	0
	OSDEN	BSEN	SHADOW	RGBF	BLANK	CLRWIN	CLRDSPR	FBKGC

OSD Screen Control 1

Bit 7: OSDEN- This bit will enable the OSD circuit as it is set to '1'. The default value is '0' after power-on.

Bit 6: BSEN- This bit will enable the bordering and shadowing effect as it is set to '1'. The default value of this bit is '0' after power-on.

Bit 5: SHADOW- When the BSEN is set to '1', it will enable the shadowing effect as this bit set to '1'. Otherwise, it will enable the bordering effect as this bit cleared to '0'. The default value is '0' after power-on. (Please refer to Figure 6)

Bit 4: RGBF- This bit controls the driving state of the output pins, R, G, B and FBKG when the OSD is disabled. After power-on, this bit is cleared to '0' and all of the R, G, B and FBKG pins output at high impedance state while the OSD being disabled. If this bit is set to '1', these R, G, B pins will drive low while OSD is being disabled, but the FBKG pins will output '0' if the FBKGP bit is set to '1', whereas output '1', set to '0'.

Bit 3: BLANK- This bit will force the FBKG pin to output high as it is set to '1'. The default value of this bit is '0' after power-on.

Bit 2: CLRWIN- This bit will clear all of windows' WINEN control bit as it is set to '1'. The default value of this bit is '0' after power-on.

Bit 1: CLRDSPR- This bit will clear all of the contents in the display registers as it is set to '1'. The default value of this bit is '0' after power-on.

Bit 0: FBKGC This bit determines the configuration of FBKG output pin. When it is cleared, the FBKG pin will output high while displaying characters or windows. Otherwise, it will output high only while displaying characters. The default value is '0' after power-on. Please refer to Figure 7 for the FBKG O/P timing.

(10) Row 15, Column 18:

	7	6	5	4	3	2	1	0
Row 15 Column 18		FBKGOP	PWMCTRL	DBOUNCE	HPOL	VPOL	VCO1	VCO0

OSD Screen Control 2

Bit 6: FBKGOP- This bit selects the polarity of the output signal of FBKG pin. This signal is active low when the user clears this bit. Otherwise, active high set this bits. The default value is '1' after power-on. Please refer to Figure 7 for the FBKGOP control timing.

Bit 5: PWMCTRL- This bit selects the output option to PWM/HFTON pin. This bit will enable the PWM output as it is set to '1'. Otherwise, it will select the HFTON option. The default value is '0' after power-on. Please refer to Figure 7 for the HFTON O/P timing and refer to Figure 8 PWMCLK O/P timing.

Bit 4: DBOUNCE- This bit activates the debounce circuit of horizontal and vertical scan. It prevents from the OSD screen shaking when the user adjusts the horizontal phase or vertical position. This bit is cleared after power-on.

Bit 3: HPOL- This bit selects the polarity of the input signal of horizontal sync (HFLB pin). If the input sync signal has negative polarity, the user must clear this bit. Otherwise, set this bit to '1' to accept a positive polarity signal. After power-on, this bit is cleared to '0' and it will accept a negative polarity sync signal.

Bit 2: VPOL- This bit selects the polarity of the input signal of vertical sync (VFLB pin). If the input sync signal is negative polarity, the user must clear this bit. Otherwise, set this bit to '1' to accept the positive polarity signal. After power-on, this bit is cleared to '0' and it will accept a negative polarity sync signal.

Bit 1 - 0: VCO1/0- These bits select the VCO frequency range when the user sets the horizontal display resolution flexibly. It is related to the horizontal display resolution and the user must set the control register at row15 / column15 properly. The default value is VCO1 = 0 & VCO0 = 0 after power-on state. The relationship between VCO1/0 and display resolution is listed as follows:

$$P.R.\ (Pixel\ Rate) = HDR * 12 * Freq_{HFLB}$$

Table 6. VCO Section & Freq. Limitation

Section	VCO1	VCO0	VCO Freq. Min	VCO Freq. Max	Unit	P.R. Limit	HFLB Freq. Limit
Freq1	0	0	6	12	MHz	Min < P.R. < Max	(Min / HDR*12) < $Freq_{HFLB}$ < Max / (HDR*12)
Freq2	0	1	12	24			
Freq3	1	0	24	48			
Freq4	1	1	48	92.2			

If there are no signals at HFLB input, the PLL will generate an approximate 1.8 MHz clock to ensure the proper operation of the I2C bus and other control registers.

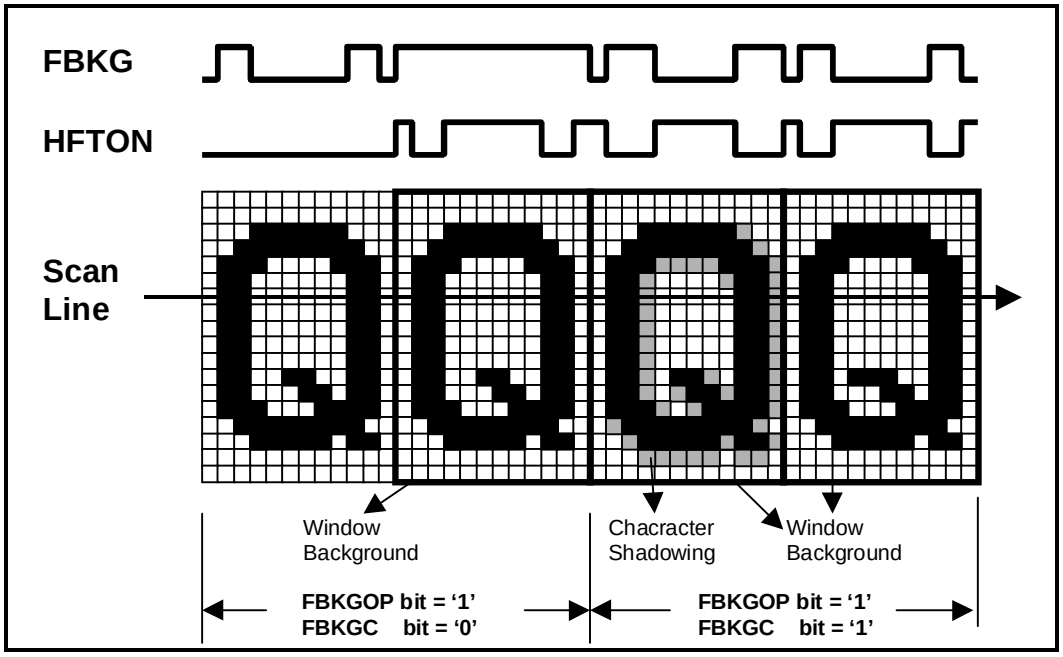


Figure 7. FBKG and HFTON Output Waveform under FBKGOP and FBKGC Bits Controlled

(11) PWM Channels Control Registers: Row 15, Column 19 - 26

	7	6	5	4	3	2	1	0
Row 15 Column 19-26	MSB							LSB

PWM Channel Control

Bit 7 - 0: These bits determine the output duty cycle and waveforms of PWM. When these bits are set to 00H, the DAC will output LOW (GND level). After power-on, all of PWM will output low ($00).

Table 7. PWM Clock & Pixel Clock Relationship

Section	VCO1	VCO0	VCO Freq. Min	VCO Freq. Max	Unit	PWM CLK	PWM Refresh Rate
Freq1	0	0	6	12	MHz	Freq1	Freq1 / 256
Freq2	0	1	12	24		Freq2/2	Freq2 / 2 / 256
Freq3	1	0	24	48		Freq3/4	Freq3 / 4 / 256
Freq4	1	1	48	92.2		Freq4 /8	Freq4 / 8 / 256

Note: Each of PWM channel will be separated by half of PWM clock. (Each has an 8-bit resolution.)

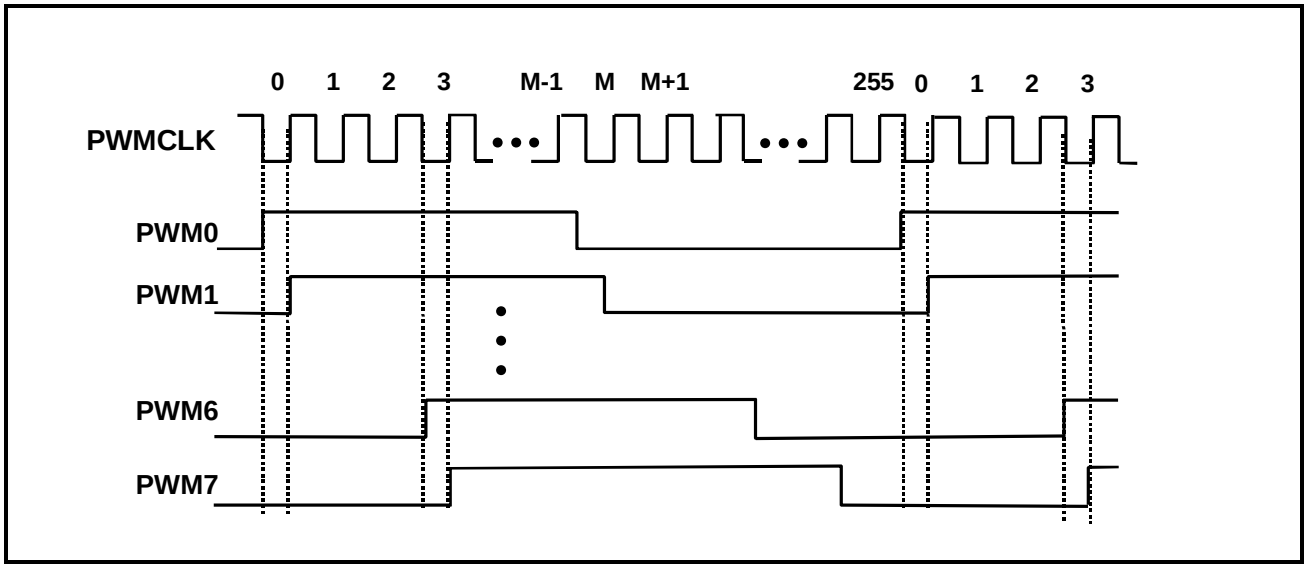


Figure 8. PWMCLK and PWM O/P timing

3. I²C Bus Communication:

The relative figure shows the I2C Bus transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, which makes up nine bits all together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in Figure "Access Register Operation". In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the displaying circuitry of NT6828, so that the received information can then be displayed.

(1) Access the Display Control Registers:

After proper identification by the receiving device, the data train of arbitrary length is transmitted from the master. There are three transmission formats from (a) to (c) as referred to Figure 9 & Table 8. The data train in each sequence consists of row addresses, column addresses, and data. In format (a), data must be preceded with the corresponding row address and column address. This format is particularly suitable for updating small amounts of data between different rows. However, if the current information byte has the same row address as the one before, format (b) is recommended. For a full screen pattern change (which requires a massive information update), or during a power-on situation, most of the row and column addresses on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. This sends the starting row and column addresses once only, and then treats all subsequent data as display information. The row and column addresses will be automatically incremented internally for each display information data from the starting location.

To differentiate the row and column addresses when transferring data from master, the MSB (Most Significant Bit) is set as in Table Transmission: '1' represents row, while '0' represents column address. Furthermore, to distinguish the column address between format (a), (b) and (c); the sixth bit of the column address is set to '1', which represents format (c), and a '0' for format (a) or (b). There is some limitation when using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

(2) Access the RAM Fonts Area:

There are some differences when accessing the RAM font. One font consists of 18 rows and 12 columns of dot matrix. At each row of one font, there are 18 bits of data which allocates 2 bytes of control data with 4 unavailable bits. Thus, each font occupies 36 bytes of control data. From the memory map of RAM fonts, font0 is allocated at row 0 & column 0 - 35, and font1, row 1 & column 0 ~ 35, etc. (Please refer to Figure 9.)

Table 8. Address Data Transmission for Registers

ITEM	No	ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0	Type
Display Register	1	Row	1	0	0	X	D	D	D	D	(a), (b), (c)
	2	Column	0	0	X	D	D	D	D	D	(a), (b)
	3	Column	0	1	X	D	D	D	D	D	(c)
Attribute / Control Register	4	Row	1	0	1	X	D	D	D	D	(a), (b), (c)
	5	Column	0	0	X	D	D	D	D	D	(a), (b)
	6	Column	0	1	X	D	D	D	D	D	(c)
RAM Fonts	7	Row	1	1	X	X	X	D	D	D	(a), (b), (c)
	8	Column	0	0	D	D	D	D	D	D	(a), (b)
	9	Column	0	1	D	D	D	D	D	D	(c)

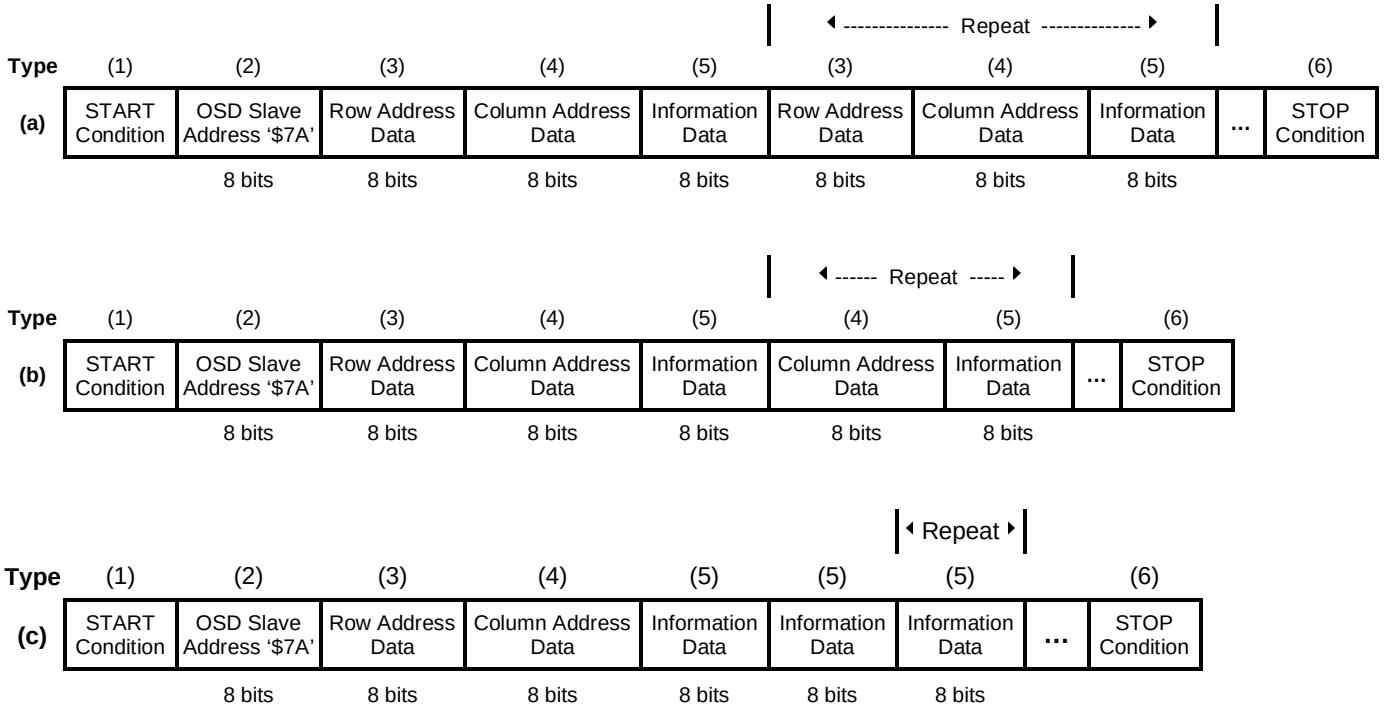


Figure 9. Access Register Operation

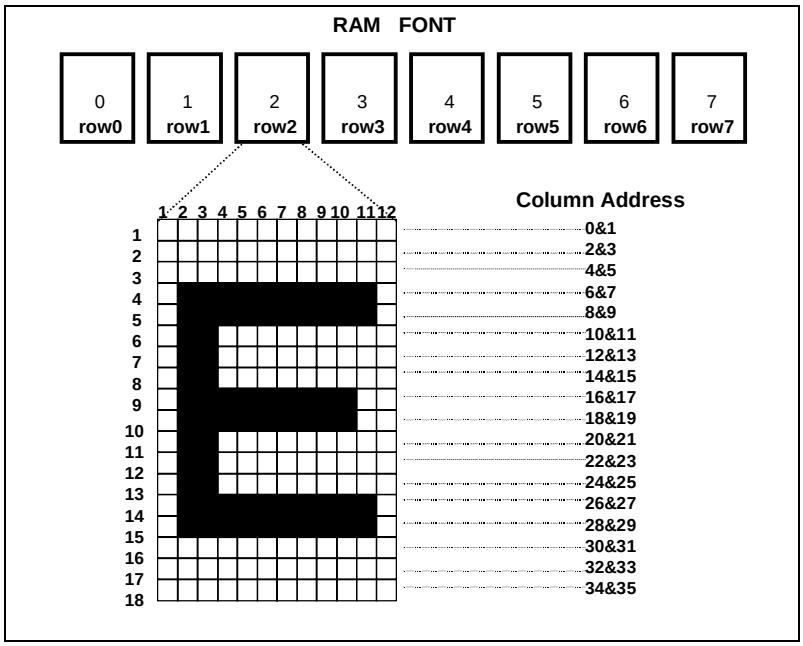


Figure 10. RAM Font Access

4. OSD Display Format:

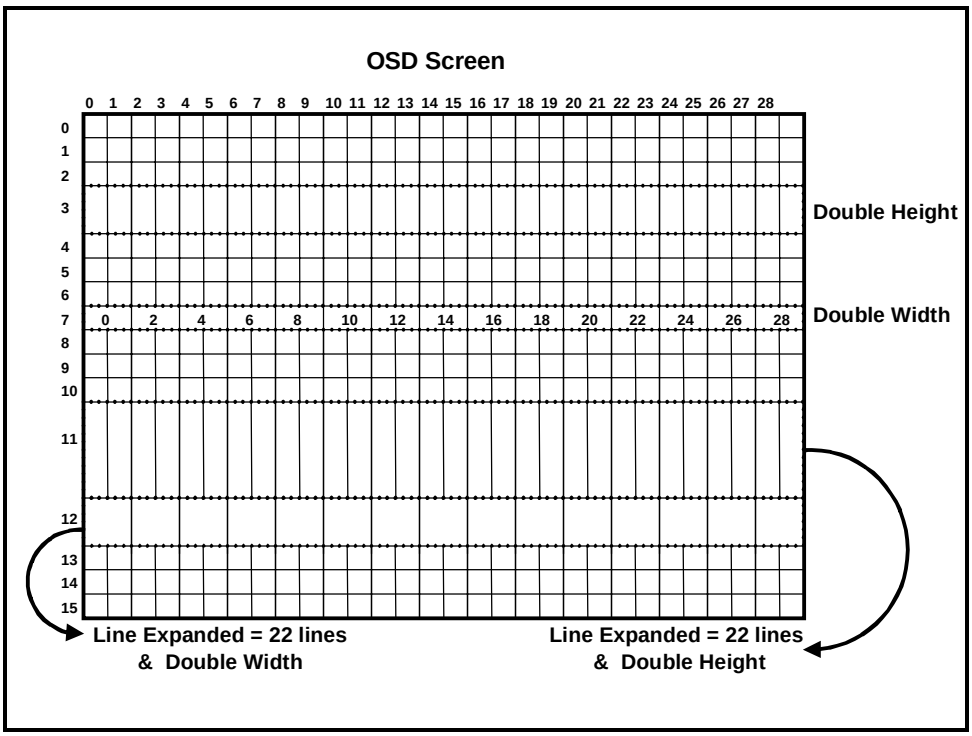


Figure 11. OSD Display Format

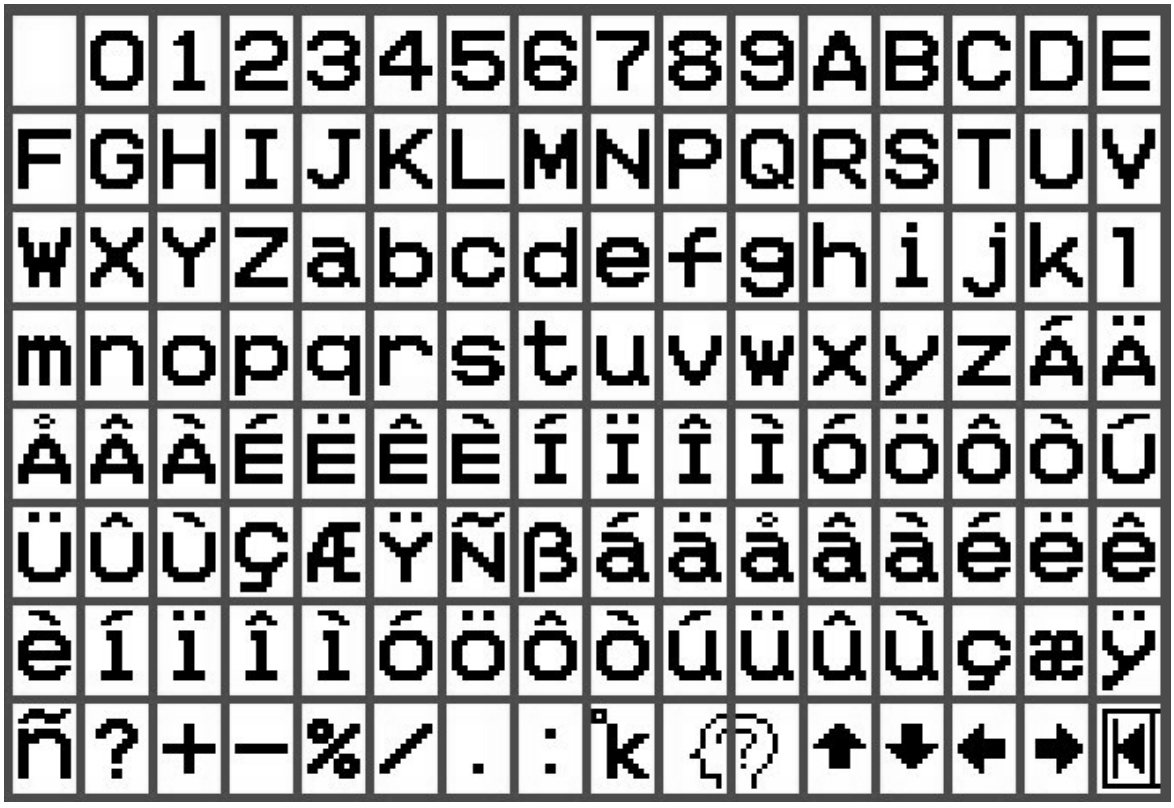


Figure 12-1. Font Code Example NT682800013

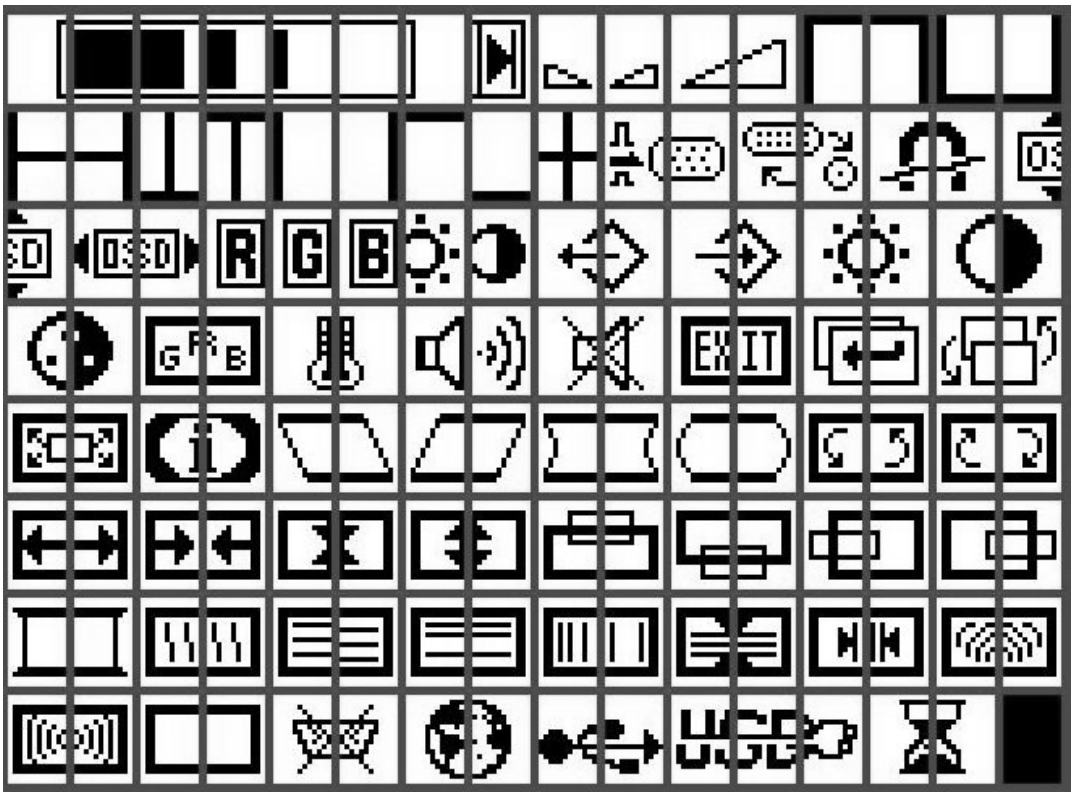


Figure 12-1. Font Code Example 682800013 (continued)

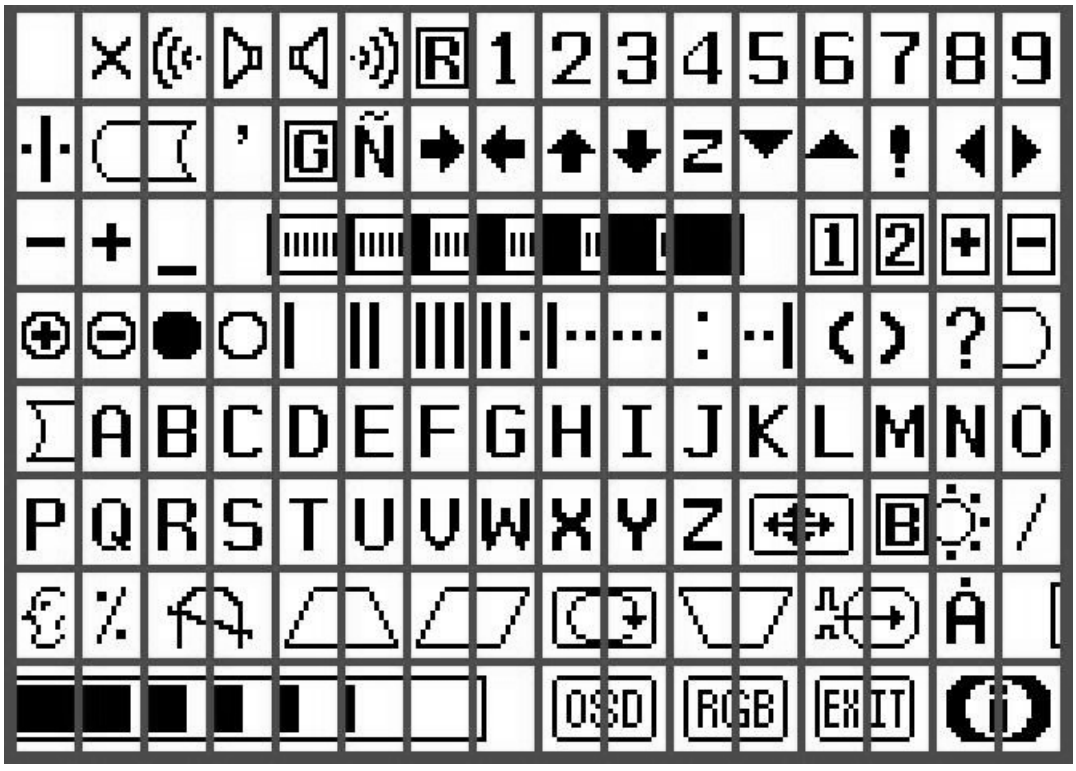


Figure 12-2. Font Code Example NT682800012

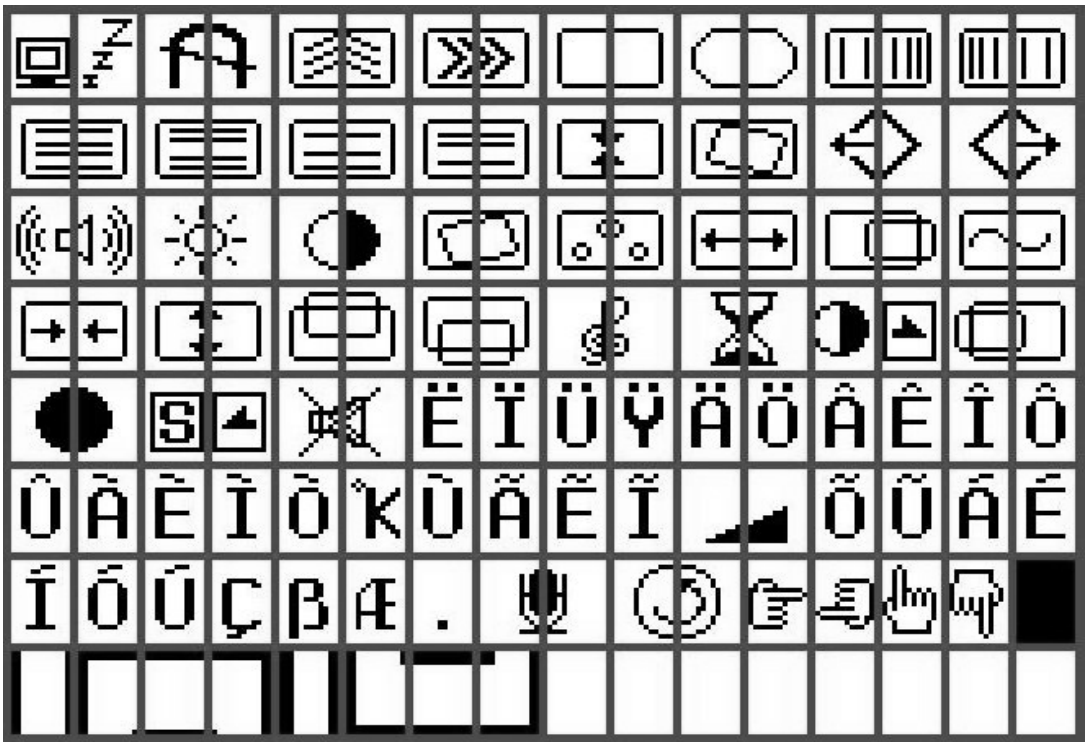


Figure 12-2. Font Code Example NT682800012 (continued)

Absolute Maximum Rating*

DC Supply Voltage . . . . . -0.3V to +7.0V

Vcc (measured to GND) . . . . . 4.75V to 5.25V

Operating Temperature . . . . . .0 to +70 ^{0}C

*Comments

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (Vcc = 5V, Tamb = 25°C)

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
Vcc	Supply Voltage	4.75	5	5.25	V	

DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{DD}	Operating Current		22	25	mA	No loading
VIH1	Input High Voltage	2			V	VFLB, HFLB with Schmitt Trigger Buffer
VIL1	Input Low Voltage			0.8	V	VFLB, HFLB Schmitt Trigger Buffer
VIH2	IIC Bus Input High Voltage	3			V	SCL, SDA
VIL2	IIC Bus Input Low Voltage			1.5	V	
Idrive1	Driving current of R, G, B, FBKG, HFTON output pins at 2.4V output voltage	80			mA	
Isink1	Sinking current of R, G, B, FBKG, HFTON output pins at 0.4V output voltage	20			mA	
Isink2	Sinking current of PWM output pins at 0.4V output voltage	4			mA	
Ileak	Leakage current of R, G, B, FBKG pins at Hi-Z state			10	uA	Output Floating State & Measured at 2.5V
Iiicl	IIC Bus Output Sink Current		5		mA	Viicoutl = 0.4 V
Vth	Input Threshold Voltage at HFLB & VFLB pin	1.8	2.0	2.2	V	
VSTIH	Schmitt Trigger Input High Voltage		1.7	2	V	
VSTIL	Schmitt Trigger Input Low Voltage	0.8	1.1		V	
Iin	Input Current of Hsync, Vsync, SDA, SCL pins	-10		+10	uA	Schmitt Trigger Buffer

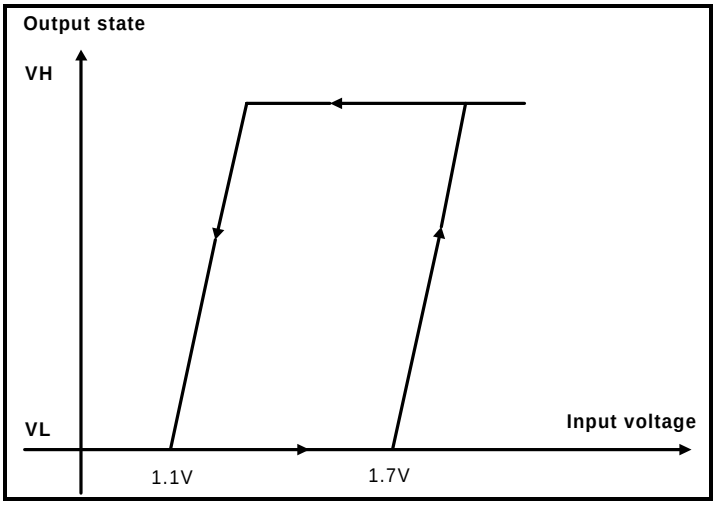


Figure 13. Schmitt Trigger Diagram

AC Characteristics

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
Fhfy	Horizontal Fly-back Frequency	30		120	KHz	
Vhfly	Horizontal Fly-back Input			5	V	
		0			V	
Thflymin	Minimum Pulse Width of Horizontal Fly-back	0.7			us	
Thflymax	Maximum Pulse Width of Horizontal Fly-back			5.5	us	
Fvfy	Vertical Fly-back Frequency	50		200	Hz	
Vvfly	Vertical Fly-back Input			5	V	
		0			V	
Tvflymin	Minimum Pulse Width of Vertical Fly-back	20			us	
Tvflymax	Maximum Pulse Width of Vertical Fly-back			1	ms	

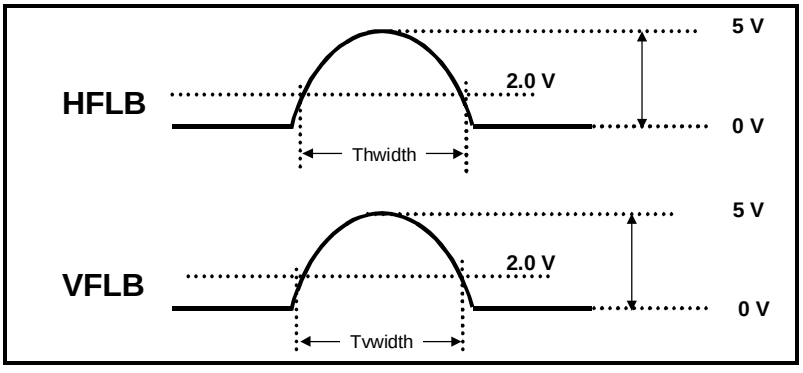
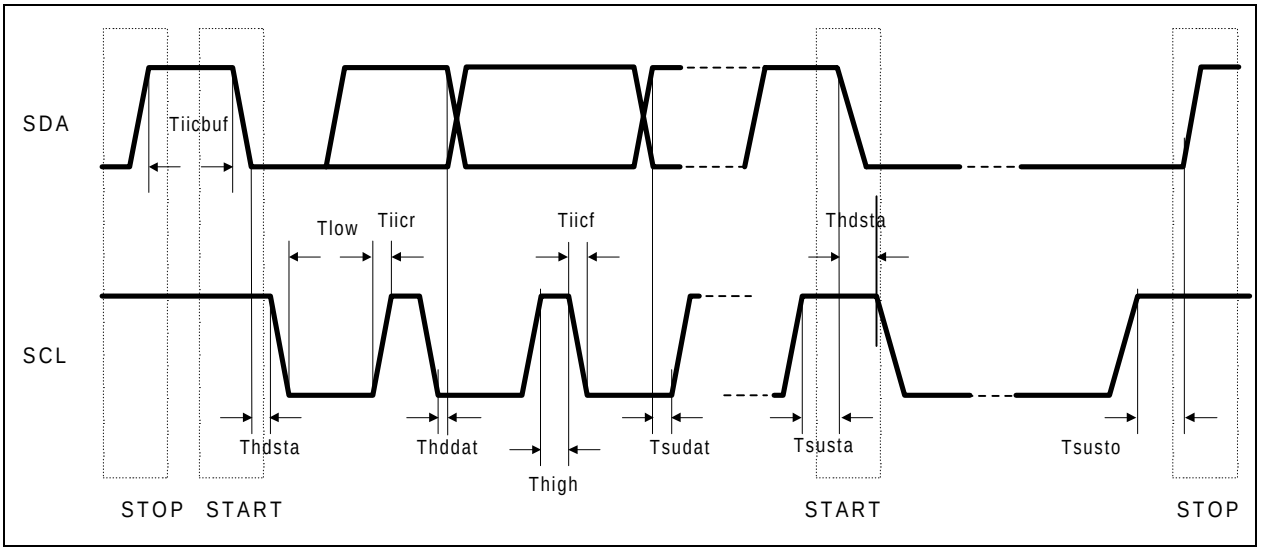


Figure 14. H/V Fly-Back Signal

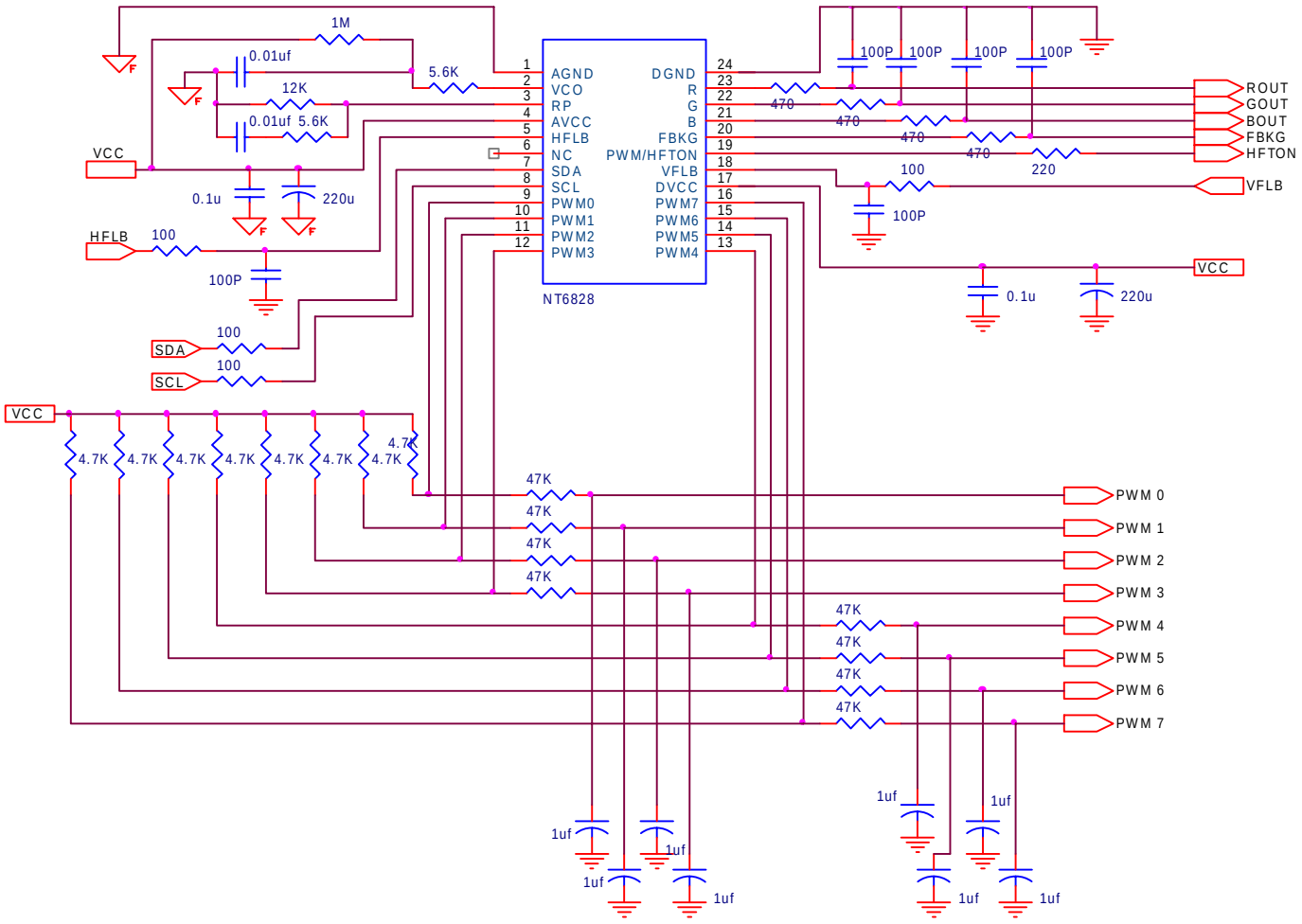
I²C Bus – Slave Receiver (Slave address: $7A)

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
Fmaxcl	Maximum SCL Clock Frequency			100	KHz	
VIL	Input Low Voltage	-0.5		1.5	V	
VIH	Input High Voltage	3.0		5.5	V	
Tlow	Low Period of the SCL Clock	4.7			us	SCL,SDA
Thigh	High Period of the SCL Clock	4.0			us	
Tsudat	Data Setup Time	250			ns	
Thddat	Data Hold Time	300			ns	
Tiicr	Rise Time of IIC Bus			1000	ns	
Tiicf	Fall Time of IIC Bus			300	ns	
Tsusta	Setup Time for Repeated START Condition	1.3			us	
Thdsta	Hold Time for START Condition	4.0			us	
Tsusta	Set-up Time for START Condition	4.7			us	
Tsusto	Set-up Time for STOP Condition	4.0			us	
Tiicbuf	The time that the IIC bus must be free before next new transmission can start	4.7			us	
Iiicl	IIC Bus Sink Current	4	5		mA	Viicoutl = 0.4 V
Tfilter	Input filter spike suppression			100	ns	SCL,SDA

Note: Please refer to I2C Table Control and I2C Sub Address Control.



Application Circuit

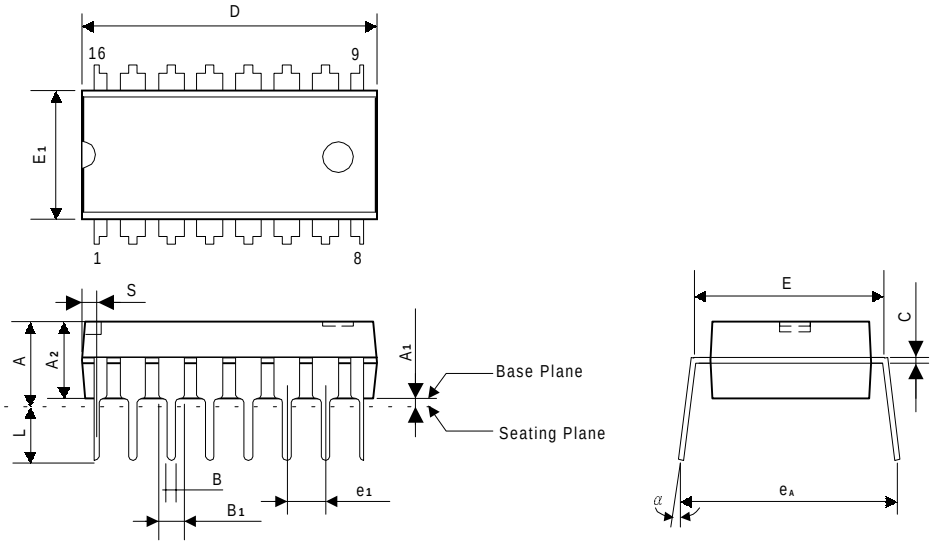


Ordering Information

Part No.	Packages
NT6828	16 DIP
NT6828K	24 Skinny DIP

Package Information

P-DIP 16L Outline Dimensions **unit: inches/mm**

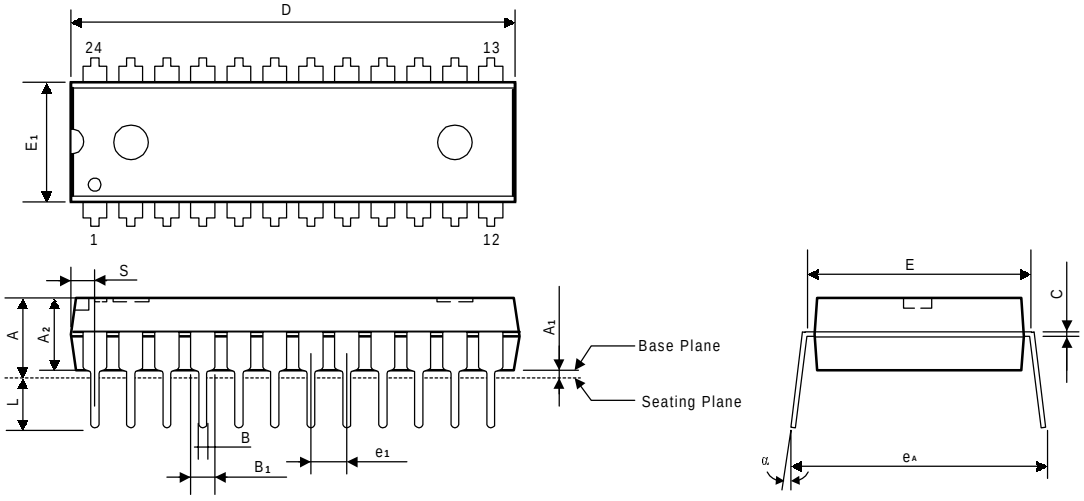


Symbol	Dimension in inch	Dimension in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130±0.010	3.30±0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.750 Typ. (0.770 Max.)	19.05 Typ. (19.56 Max.)
E	0.300±0.010	7.62±0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100±0.010	2.54±0.25
L	0.130±0.010	3.30±0.25
α	0°~ 15°	0°~ 15°
e_A	0.345±0.035	8.76±0.89
S	0.040 Max.	1.02 Max.

Note:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

Package Information

Skinny-DIP 24L Outline Dimensions **unit: inches/mm**



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α	0°~ 15°	0°~ 15°
e_A	0.345±0.035	8.76±0.89
S	0.040 Max.	1.02 Max.

Notes:
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2. Dimension E_1 does not include resin fins.
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