ENHANCED DIFFERENTIAL RECEIVER

FEATURES

- **3.3V and 5V power supply options**
- **250ps propagation delay**
- **Very high voltage gain vs. standard EL16 or EL16V**
- **Ideal for Pulse Amplifier and Limiting Amplifier applications**
- **Data synchronous Enable/Disable ($\overline{EN}$) on Q_{HG} and $\overline{Q}_{HG}$ provides for complete glitchless gating of the outputs**
- **Ideal for gating timing signals**
- **Complete solution for high quality, high frequency crystal oscillator applications**
- **Internal 75K Ohm input pull-down resistors**
- **ESD protection of 2000V**
- **Available in both 8 and 16-pin SOIC; 8 and 10-pin TSSOP and in DIE form**

PIN NAMES

Pin	Function
D	Data Inputs
Q	Data Outputs
Q_{HG}	Data Outputs w/High Gain
V_{BB}	Reference Voltage Output
$\overline{EN}$	Enable Input

TRUTH TABLE

$\overline{EN}$	QHG Output
0	Data
1	Logic Low

DESCRIPTION

The SY10/100EL16VA-VF are differential receivers. The devices are equivalent to SY10/100EL16 or SY10/100EL16V with enhanced capabilities. The $Q_{HG}/\overline{Q}_{HG}$ outputs have a DC gain several times larger than the DC gain of the Q output.

The SY10/100EL16VA have an identical pinout to the SY10/100EL16 or SY10/100EL16V. It provides a V_{BB} output for either single-ended application or as a DC bias for AC coupling to the device.

The SY10/100EL16VB are very similar to the SY10/100EL16VA. The $\overline{Q}$ output is provided for feedback purposes.

The SY10/100EL16VC provides an $\overline{EN}$ input which is synchronized with the data input (D) signal in a way that provides glitchless gating of the Q_{HG} and $\overline{Q}_{HG}$ outputs. When the $\overline{EN}$ signal is LOW, the input is passed to the outputs and the data output equals the data input. When the data input is HIGH and the $\overline{EN}$ goes HIGH, it will force the Q_{HG} LOW and the $\overline{Q}_{HG}$ HIGH on the next negative transition of the data input. If the data input is LOW when the $\overline{EN}$ goes HIGH, the next data transition to a HIGH is ignored and Q_{HG} remains LOW and $\overline{Q}_{HG}$ remains HIGH. The next positive transition of the data input is not passed on to the data outputs under these conditions. The Q_{HG} and $\overline{Q}_{HG}$ outputs remain in their disabled state as long as the $\overline{EN}$ input is held HIGH. The $\overline{EN}$ input has no influence on the $\overline{Q}$ output and the data input is passed on (inverted) to this output whether $\overline{EN}$ is HIGH or LOW. This configuration is ideal for crystal oscillator applications, where the oscillator can be free running and gated on and off synchronously without adding extra counts to the output.

The SY10/100EL16VD provides the flexibility of all the combinations in DIE form, in 16-pin 150mil SOIC package or in 10-pin TSSOP package. The 16-pin SOIC and 10-pin TSSOP packages are ideal for prototyping DIE applications.

The SY10/100EL16VE are similar to the SY10/100EL16VB where the Q, $\overline{Q}$ output is made available differently. In this package option, V_{BB} is no longer provided.

The SY10/100EL16VF are similar to the SY10/100EL16VC, offering the D, $\overline{D}$ inputs rather than the V_{BB} output.

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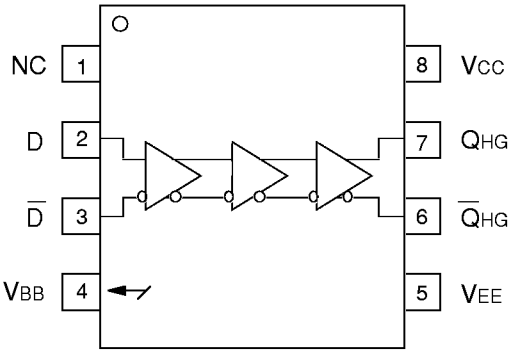
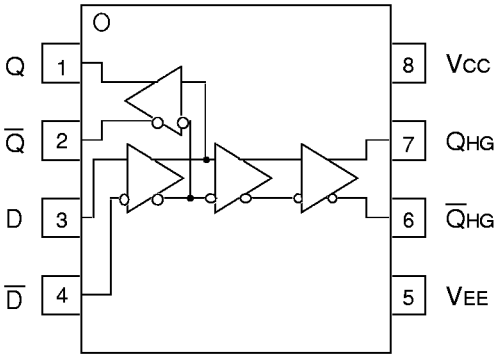
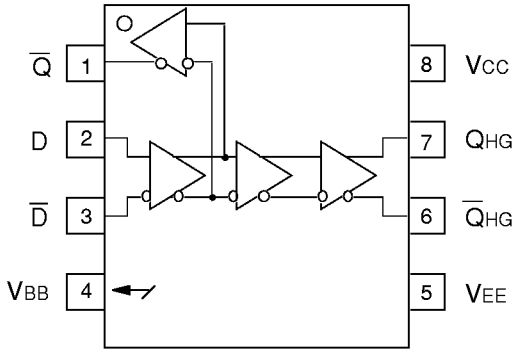
PIN CONFIGURATION/BLOCK DIAGRAM



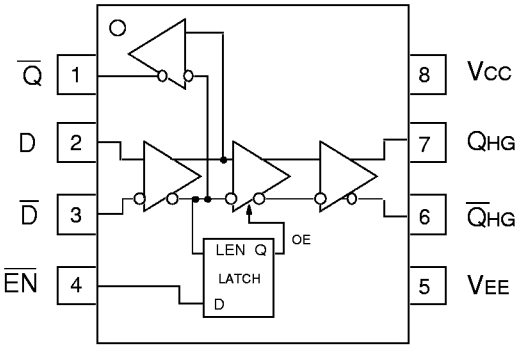
SY10/100EL16VA
5V/3.3V Differential Receiver w/High Gain
(Available in 8-pin SOIC or 8-pin TSSOP)



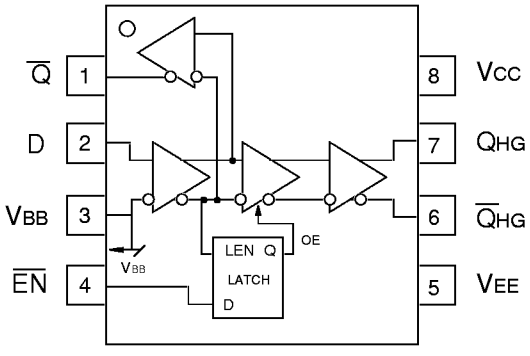
SY10/100EL16VE
EL16VB w/Differential Q, QB output (no VBB)
(Available in 8-pin SOIC or 8-pin TSSOP)



SY10/100EL16VB
EL16VA w/Extra QB output
(Available in 8-pin SOIC or 8-pin TSSOP)

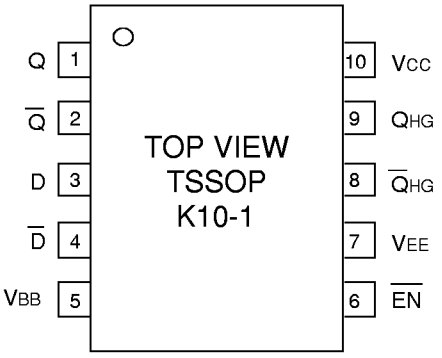


SY10/100EL16VF
EL16VC w/Differential Data Input
(Available in 8-pin SOIC or 8-pin TSSOP)

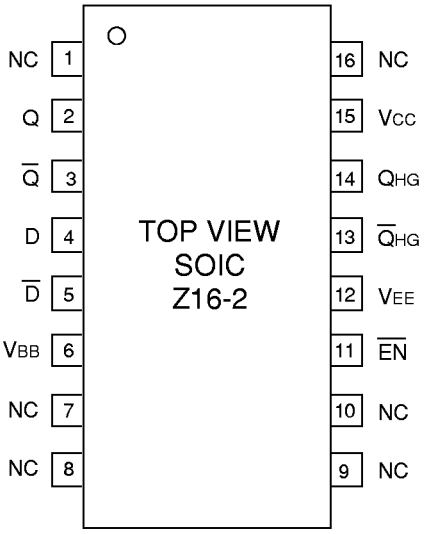


SY10/100EL16VC
EL16VB w/Enable Input
(Available in 8-pin SOIC or 8-pin TSSOP)

PIN CONFIGURATION/BLOCK DIAGRAM (Continued)



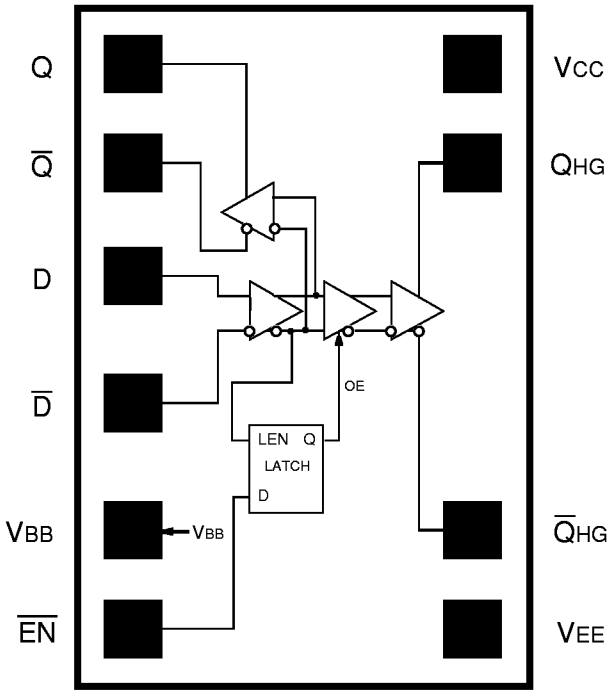
SY10/100EL16VDKC
EL16VDXC packaged in 10-pin TSSOP



SY10/100EL16VDZC
EL16VDXC packaged in 16-pin SOIC

DIE LAYOUT

All options in DIE form w/Extra Q output and VBB output
Die Size (mils) 39. X 52. X 14.5



SY10/100EL16VDXC

DIE
TOP VIEW

DC ELECTRICAL CHARACTERISTICS[1]

V_{EE} = V_{EE} (Min) to V_{EE} (Max), V_{CC} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current 10EL	—	—	40	—	—	40	—	—	40	—	—	40	mA
	100EL	—	—	40	—	—	40	—	—	40	—	—	46	
V_{BB}	Output Reference Voltage 10EL	–1.43	—	–1.30	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19	V
	100EL	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

NOTE:

1. Parametric values specified at: 10/100EL16VA-VE Series: -3.0V to -5.5V.

AC ELECTRICAL CHARACTERISTICS[4]

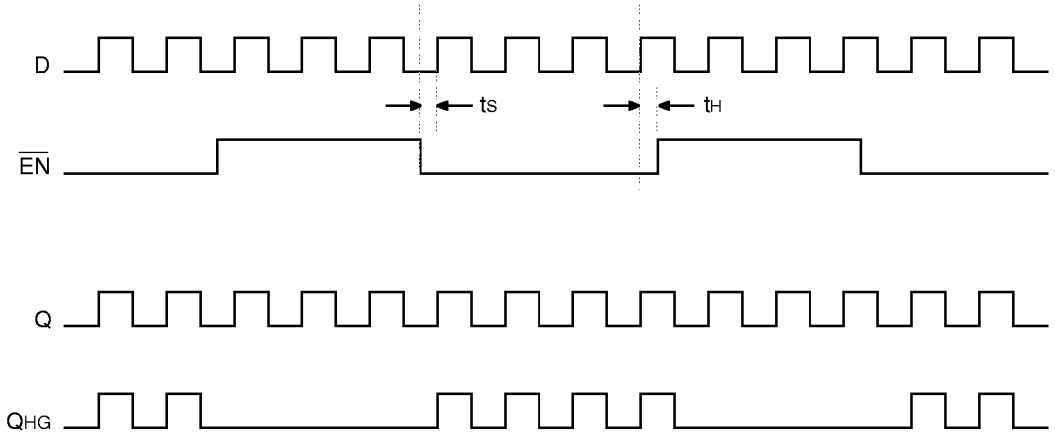
V_{EE} = V_{EE} (Min) to V_{EE} (Max), V_{CC} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Q/$\overline{Q}$ Output D (Diff)	—	—	350	—	—	350	—	—	350	—	—	380	ps
	D (SE)	—	—	400	—	—	400	—	—	400	—	—	430	
	Q_{HG}/$\overline{Q}_{HG}$ Output D (Diff)	—	—	650	—	—	650	—	—	650	—	—	730	
	D (SE)	—	—	700	—	—	700	—	—	700	—	—	780	
t_S	Setup Time $\overline{EN}$	—	150	—	—	150	—	—	150	—	—	150	—	ps
t_H	Hold Time $\overline{EN}$	—	150	—	—	150	—	—	150	—	—	150	—	ps
t_{skew}	Duty Cycle Skew[1] (Diff)	—	5	—	—	5	20	—	5	20	—	5	20	ps
V_{PP}	Minimum Input Swing[2]	150	—	—	150	—	—	150	—	—	150	—	—	mV
V_{CMR}	Common Mode Range[3]	–1.3	—	–0.4	–1.4	—	–0.4	–1.4	—	–0.4	–1.4	—	–0.4	V
tr tf	Output Q Rise/Fall Time (20% TO 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

NOTES:

1. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
2. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 to Q/$\overline{Q}$ outputs and a DC gain of ≈ 200 or higher to Q_{HG}/$\overline{Q}_{HG}$ outputs.
3. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR} (min) will be fixed at 3.3V – |V_{CMR} (min)|.
4. Parametric values specified at: 10/100EL16VA-VE Series: -3.0V to -5.5V.

TIMING DIAGRAM

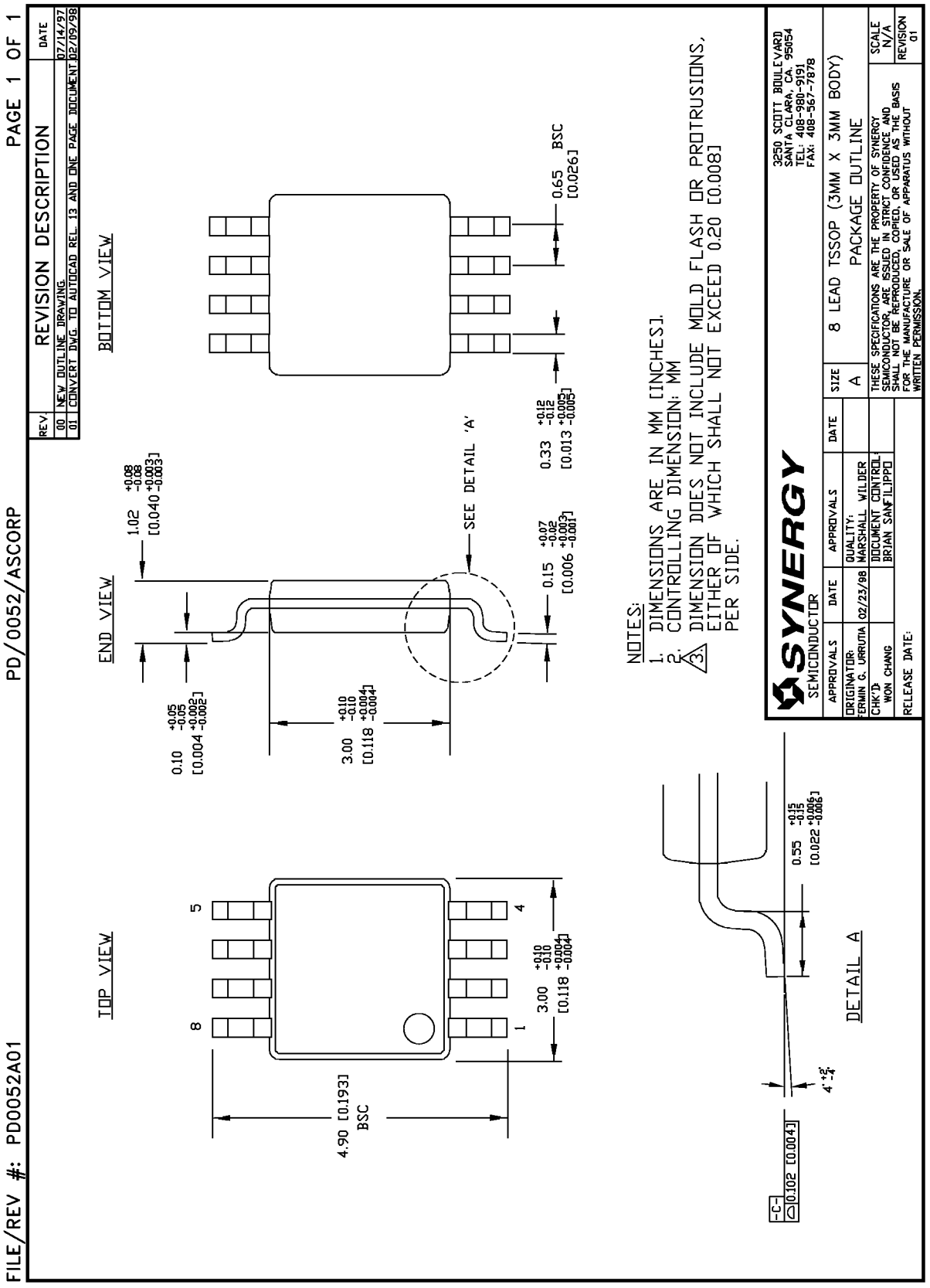


PRODUCT ORDERING CODE

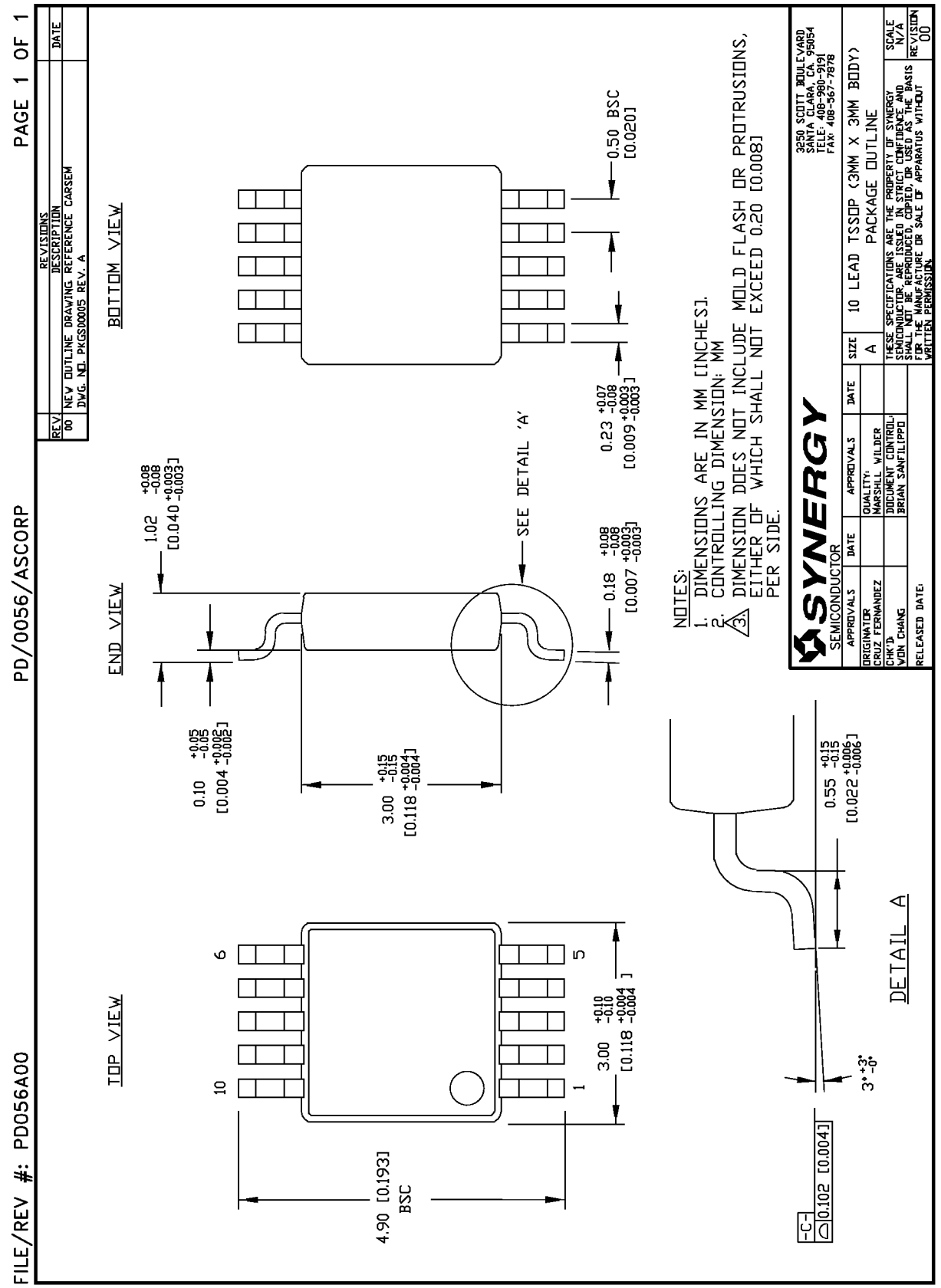
Ordering Code	Package Type	Operating Range	VEE Range (V)
SY10EL16VAZC	Z8-1	Commercial	-3.0 to -5.5
SY10EL16VAZCTR	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VAZC	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VAZCTR	Z8-1	Commercial	-3.0 to -5.5
SY10EL16VBZC	Z8-1	Commercial	-3.0 to -5.5
SY10EL16VBZCTR	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VBZC	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VBZCTR	Z8-1	Commercial	-3.0 to -5.5
SY10EL16VCZC	Z8-1	Commercial	-3.0 to -5.5
SY10EL16VCZCTR	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VCZC	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VCZCTR	Z8-1	Commercial	-3.0 to -5.5
SY10EL16VDZC	Z16-2	Commercial	-3.0 to -5.5
SY10EL16VDZCTR	Z16-2	Commercial	-3.0 to -5.5
SY100EL16VDZC	Z16-2	Commercial	-3.0 to -5.5
SY100EL16VDZCTR	Z16-2	Commercial	-3.0 to -5.5
SY10EL16VEZC	Z8-1	Commercial	-3.0 to -5.5
SY10EL16VEZCTR	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VEZC	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VEZCTR	Z8-1	Commercial	-3.0 to -5.5
SY10EL16VFZC	Z8-1	Commercial	-3.0 to -5.5
SY10EL16VFZCTR	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VFZC	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VFZCTR	Z8-1	Commercial	-3.0 to -5.5

Ordering Code	Package Type	Operating Range	VEE Range (V)
SY10EL16VAKCTR	K8-1	Commercial	-3.0 to -5.5
SY100EL16VAKCTR	K8-1	Commercial	-3.0 to -5.5
SY10EL16VBKCTR	K8-1	Commercial	-3.0 to -5.5
SY100EL16VBKCTR	K8-1	Commercial	-3.0 to -5.5
SY10EL16VCKCTR	K8-1	Commercial	-3.0 to -5.5
SY100EL16VCKCTR	K8-1	Commercial	-3.0 to -5.5
SY10EL16VDKCTR	K10-1	Commercial	-3.0 to -5.5
SY100EL16VDKCTR	K10-1	Commercial	-3.0 to -5.5
SY10EL16VEKCTR	K8-1	Commercial	-3.0 to -5.5
SY100EL16VEKCTR	K8-1	Commercial	-3.0 to -5.5
SY10EL16VFKCTR	K8-1	Commercial	-3.0 to -5.5
SY100EL16VFKCTR	K8-1	Commercial	-3.0 to -5.5
SY10EL16VDXC	DIE	Commercial	-3.0 to -5.5
SY100EL16VDXC	DIE	Commercial	-3.0 to -5.5

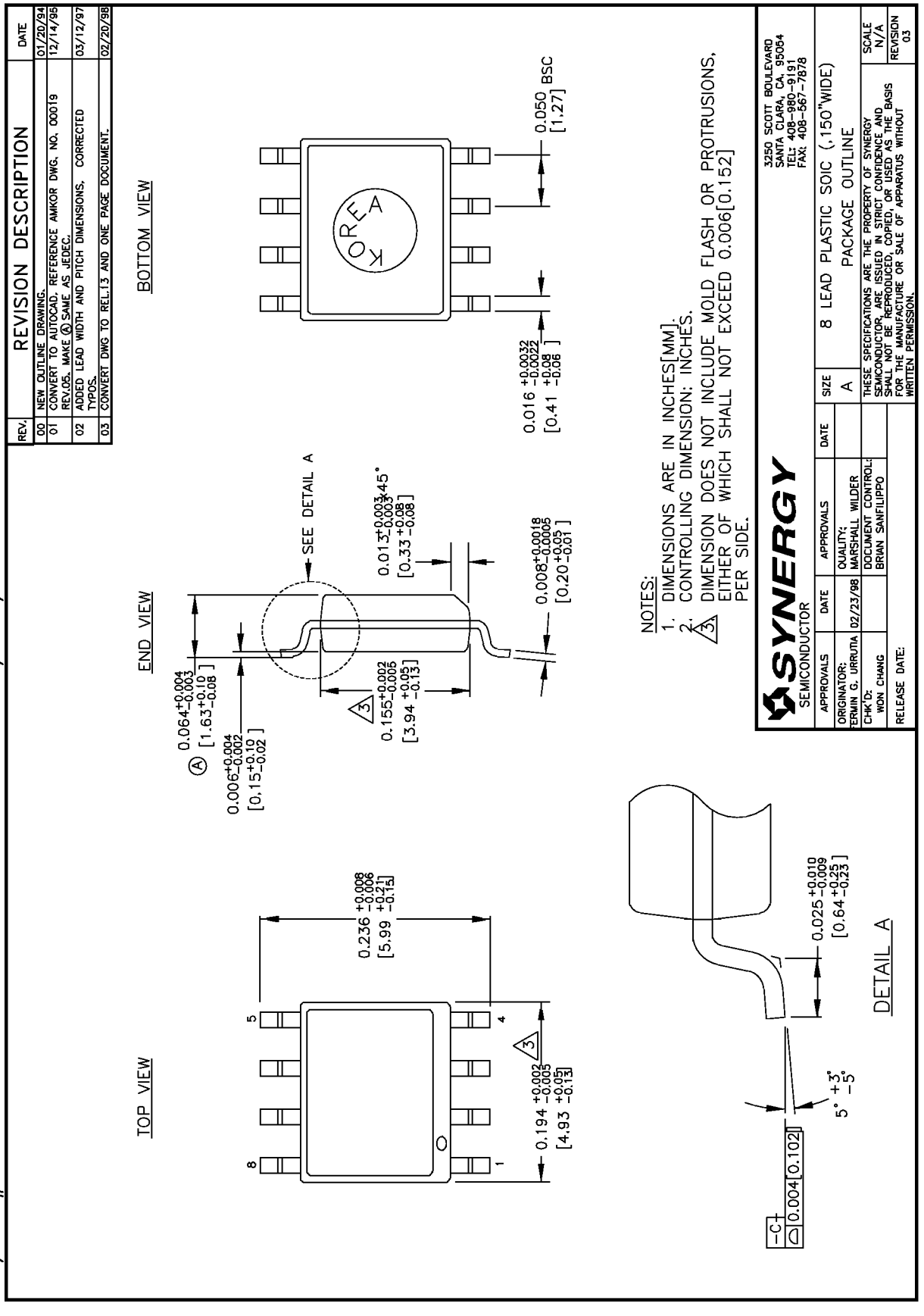
8 LEAD TSSOP (K8-1)



10 LEAD TSSOP (K10-1)



8 LEAD PLASTIC SOIC (Z8-1)



16 LEAD PLASTIC SOIC .150" WIDE (Z16-2)