Multi-Rate to 2.7Gb/s Clock and Data Recovery IC with Integrated Limiting Amp

Preliminary Technical Data — ADN2819

FEATURES

Meets SONET Requirements for Jitter Transfer / Generation / Tolerance
Quantizer Sensitivity: 4 mV typical
Adjustable Slice Level: +/- 100 mV
1.9GHz minimum Bandwidth
Patented Clock Recovery Architecture
Loss of Signal Detect Range: TBD to 15mV
Single Reference Clock Frequency for all rates, including 15/14 (7%) Wrapper Rate
Choice of 19.44, 38.88, 77.76 or 155.52MHz REFCLK. LVPECL / LVDS / LVCMOS / LVTTL compatible inputs (LVPECL / LVDS only at 155.52 MHz)
19.44MHz Oscillator on chip to be used with external crystal
Loss of Lock indicator
Loopback mode for High Speed Test Data
Output Squelch & Bypass features
Single Supply Operation: 3.3 Volts
Low Power: 540mW Typical
7 x 7 mm 48 pin LFCSP

APPLICATIONS

SONET OC-3/12/48, SDH STM-1/4/16, GbE and 15/14 FEC rates
WDM Transponders
Regenerators/Repeaters
Test Equipment
Backplane Applications

PRODUCT DESCRIPTION

The ADN2819 provides the receiver functions of Quantization, Signal Level Detect and Clock and Data Recovery at rates of OC-3, OC-12, OC-48, Gigabit Ethernet and 15/14 FEC rates. All SONET jitter requirements are met, including: Jitter Transfer; Jitter Generation; and Jitter Tolerance. All specifications are quoted for -40 to 85C ambient temperature unless otherwise noted.

The device is intended for WDM system applications and can be used with either an external reference clock or an on-chip oscillator with external crystal. Both native rates and 15/14 rate digital wrappers are supported by the ADN2819, without any change of reference clock.

This device together with a PIN diode and a TIA preamplifier can implement a highly integrated, low cost, low power fiber optic receiver.

The receiver front end Signal Detect circuit indicates when the input signal level has fallen below a user adjustable threshold. The Signal Detect has typically TBD hysteresis to prevent chatter at the output.

The ADN2819 is available in a compact 7x7 mm 48 pin chip scale package.

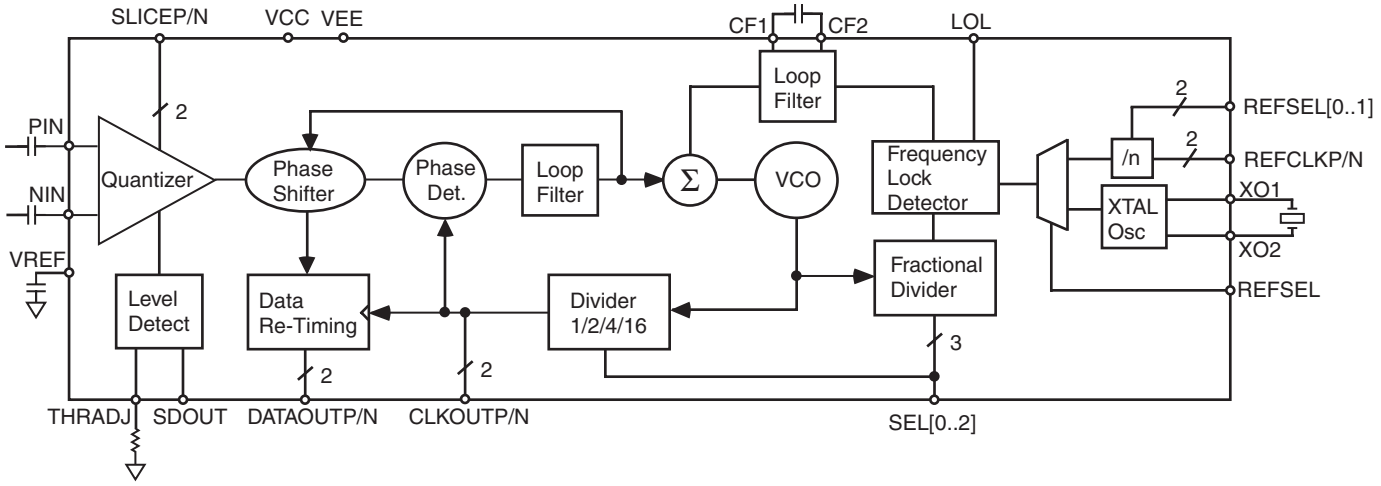

Figure 1. ADN2819 Block Diagram

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

ADN2819–SPECIFICATIONS

($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, V_{EE} = 0V, C_F=4.7uF, SLICEP=SLICEN=VCC, unless otherwise noted.)

PARAMETER	Conditions	Min	Typ	Max	Units
Quantizer - DC Characteristics					
Input Voltage Range	@ PIN or NIN, DC Coupled	0		1.2	V
Peak to Peak Differential Input				2.4	V
Input Common Mode Level	DC Coupled. See Figure 24	0.4			V
Differential Input Sensitivity	PIN-NIN, AC Coupled[1], BER = $1x10^{-10}$	TBD	4		mVpp
Input Overdrive	Figure 5	TBD	2		mVpp
Input Offset			110		uV
Input RMS Noise	BER = $1x10^{-10}$		244		uVrms
Quantizer - AC Characteristics					
Upper -3dB Bandwidth			1.9		GHz
Small Signal Gain	Differential		54		dB
S11	@2.5 GHz		-15		dB
Input Resistance	Differential		100		Ω
Input Capacitance			0.65		pF
Pulse Width Distortion[2]			30		ps
Quantizer Slice Adjustment					
Gain	SliceP-SliceN = +/-0.5V	TBD	.110	TBD	V/V
Control Voltage Range	SliceP-SliceN	-0.8		0.8	V
Control Voltage Range	@SliceP or SliceN	1.3		VCC	V
Slice Threshold Offset			+/-1.0		mV
Level Signal Detect (SDOUT)					
Level Detect Range (Figure 3)	R_{Thresh}= 2kΩ	TBD	TBD	TBD	mV
	R_{Thresh}= 20kΩ	TBD	TBD	TBD	mV
	R_{Thresh}= 90kΩ	TBD	TBD	TBD	mV
Response Time	DC Coupled	0.1		5	µs
Hysteresis (Electrical)	R_{Thresh}= 2kΩ	TBD	TBD	TBD	dB
	R_{Thresh}= 20kΩ	TBD	TBD	TBD	dB
	R_{Thresh}= 90kΩ	TBD	TBD	TBD	dB
Power Supply Voltage		3.0	3.3	3.6	V
Power Supply Current		140	164	233	mA
Phase-Locked Loop Characteristics	**PIN-NIN = 10mVp-p**				
Jitter Transfer BW	OC-48		660	1000	kHz
	GbE		330	500	kHz
	OC-12		167	250	kHz
	OC-3		41	60	kHz
Jitter Tolerance	OC-48 (see Fig 10)				
	600Hz[3]		100	TBD	UIp-p
	6KHz		20	TBD	UIp-p
	100kHz[3]		5.5	TBD	UIp-p
	1MHz[3]		1.0	TBD	UIp-p
Jitter Generation	OC-48, 12kHz-20MHz		0.003	0.01	UIrms
			0.05	0.1	UIp-p
	OC-12, 12kHz-5MHz		0.003	0.01	UIrms
			0.03	0.1	UIp-p
	OC-3, 12kHz-1.3MHz		0.001	0.01	UIrms
			0.01	0.1	UIp-p
Jitter Peaking	OC-48		0.025		dB
	OC-12		0.004		dB
	OC-3		0.002		dB

Notes:
1. PIN and NIN should be differentially driven, AC coupled for optimum sensitivity.
2. PWD measurement made on quantizer outputs in BYPASS mode.
3. Jitter Tolerance measurements are equipment limited.

Specifications subject to change without notice.

PARAMETER	Conditions	Min	Typ	Max	Units
CML Ouputs (CLKOUTP/N, DATAOUTP/N)					
Single-Ended Output Swing	V_{SE}, See Figure 4	300	350	500	mV
Differential Output Swing	V_{DIFF}, See Figure 4	600	700	1000	mV
Output High Voltage	V_{OH}		VCC		V
Output Low Voltage	V_{OL}	VCC-.45		VCC-0.3	V
Rise Time	20%-80%			150	ps
Fall time	80%-20%			150	ps
Setup Time	T_S, See Figure 2				
	OC-48	150			ps
	GbE	350			ps
	OC-12	750			ps
	OC-3	3150			ps
Hold Time	T_H, See Figure 2				
	OC-48	150			ps
	GbE	350			ps
	OC-12	750			ps
	OC-3	3150			ps
REFCLK DC Input Characteristics					
Input Voltage Range	@REFCLKP or REFCLKN	0		VCC	V
Peak to Peak Differential Input		100			mV
Common Mode Level	DC Coupled, Single-ended		VCC/2		V
Test Data DC Input Characteristics[4] (TDINP/N)	CML inputs				
Peak to Peak Differential Input Voltage			0.8		V
LVTTL DC Input Characteristics					
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V
Input High Current	I_{IH}, Vin=2.4V			5	uA
Input Low Current	I_{IL}, Vin=0.4V	-5			uA
LVTTL DC Output Characteristics					
Output High Voltage	V_{OH}, I_{OH}=-2.0mA	2.4			V
Output Low Voltage	V_{OL}, I_{OL}=2.0mA			0.4	V

Notes:
4. TDINP/N are CML inputs. If the drivers to the TDINP/N inputs are anything other than CML, they must be AC coupled.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC).....8V
Minimum Input Voltage (all inputs).....VEE-0.4V
Maximum Input Voltage (all inputs).....VCC+0.4V
Maximum Junction Temperature.....165° C
Storage Temperature.....-65° C to 150° C
Lead Temperature (soldering 10s).....300° C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

MODEL	TEMP RANGE	PACKAGE	OPTION
ADN2819XCP	-40°C to 85°C	48-LFCSP	CP-48
ADN2819XCP-RL	-40°C to 85°C	48-LFCSP tape-reel 2500pcs	CP-48

THERMAL CHARACTERISTICS

Thermal Resistance

48-LFCSP, 4 layer board with exposed paddle soldered to VCC
Θ_{JA}=25° C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 3000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN2819 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

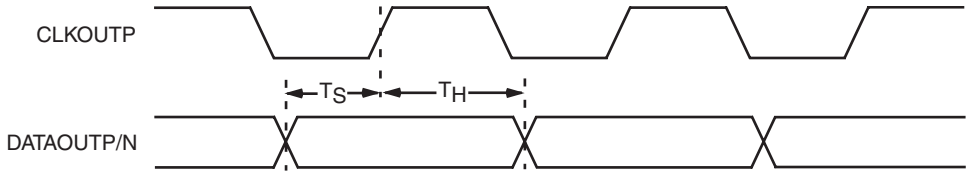


Figure 2. Output Timing

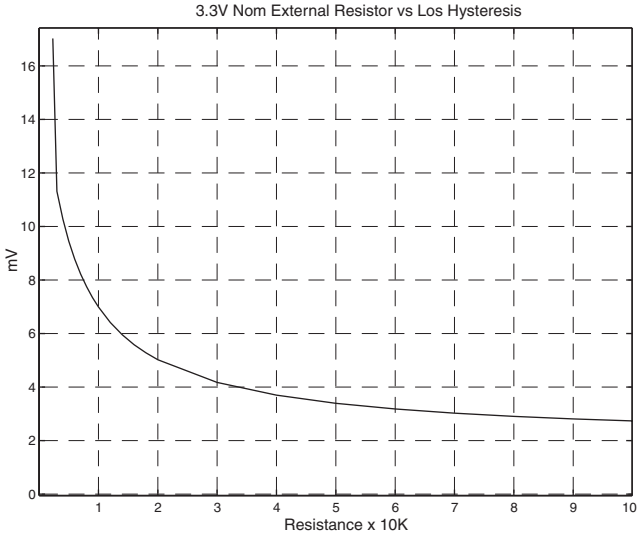


Figure 3. LOS Comparator trip Point Programming

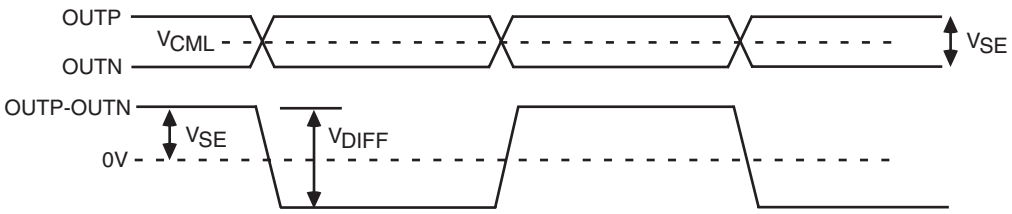


Figure 4. Single-ended -vs- Differential Output Specs

DEFINITION OF TERMS

Maximum, Minimum and Typical Specifications

Specifications for every parameter are derived from statistical analyses of data taken on multiple devices from multiple wafer lots. Typical specifications are the mean of the distribution of the data for that parameter. If a parameter has a maximum (or a minimum), that value is calculated by adding to (or subtracting from) the mean six times the standard deviation of the distribution. This procedure is intended to tolerate production variations: if the mean shifts by 1.5 standard deviations, the remaining 4.5 standard deviations still provide a failure rate of only 3.4 parts per million. For all tested parameters, the test limits are guardbanded to account for tester variation to thus guarantee that no device is shipped outside of data sheet specifications.

INPUT SENSITIVITY AND INPUT OVERDRIVE

Sensitivity and Overdrive specifications for the Quantizer involve offset voltage, gain and noise. The relationship between the logic output of the quantizer and the analog voltage input is shown in Figure 5. For sufficiently large positive input voltage the output is always Logic 1 and similarly, for negative inputs, the output is always Logic 0. However, the transitions between output Logic Levels 1 and 0 are not at precisely defined input voltage levels, but occur over a range of input voltages. Within this Zone of Confusion, the output may be either 1 or 0, or it may even fail to attain a valid logic state. The width of this zone is determined by the input voltage noise of the quantizer. The center of the Zone of Confusion is the quantizer input offset voltage . Input Overdrive is the magnitude of signal required to guarantee correct logic level with $1x10^{-10}$ confidence level.

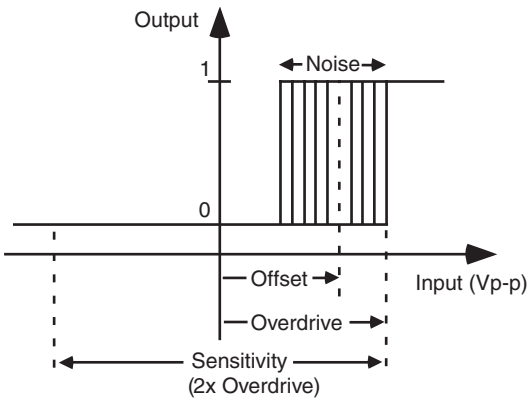


Figure 5. Input Sensitivity and Input Overdrive

SINGLE-ENDED -VS- DIFFERENTIAL

AC coupling is typically used to drive the inputs to the Quantizer. The inputs are internally DC biased to a common-mode potential of ~0.6V. Driving the ADN2819 single-ended and observing the Quantizer input with an oscilloscope probe at the point indicated in Figure 6 shows a binary signal with average value equal to the common-mode potential and instantaneous values both above and below the average value. It is convenient to measure the peak-to-peak amplitude of this signal and call the minimum required value the Quantizer Sensitivity. Referring to Figure 5, since both positive and negative offsets need to be accommodated, the sensitivity is twice the overdrive. The ADN2819 quantizer has TBD mV minimum sensitivity.

Driving the ADN2819 differentially (see Figure 7), sensitivity seems to improve from observing the quantizer input with an oscilloscope probe. This is an illusion caused by the use of a single-ended probe. A 5 mV peak-to-peak signal appears to drive the ADN2819 quantizer. However, the single-ended probe measures only half the signal. The true quantizer input signal is twice this value since the other quantizer input is a complementary signal to the signal being observed.

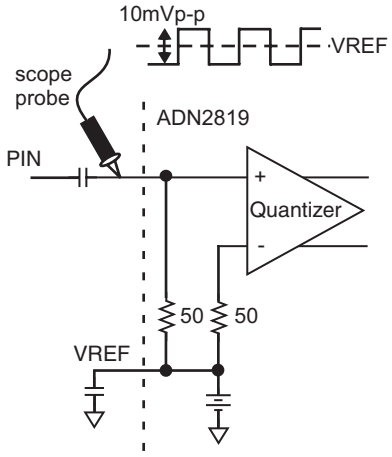


Figure 6. Single-ended sensitivity measurement

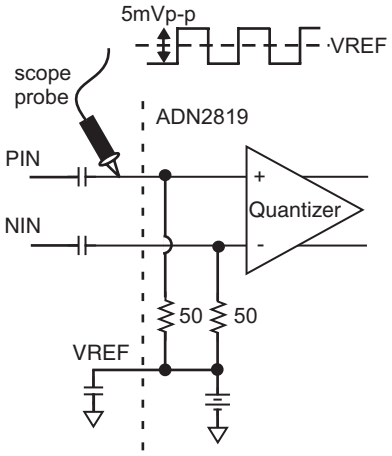


Figure 7. Differential sensitivity measurement

LOS RESPONSE TIME

LOS response time is the delay between removal of the input signal and indication of Loss of Signal (LOS) at SDOUT. The response time of the AD2819 is 300ns typ when the inputs are DC coupled. In practice, the time constant of the ac coupling at the quantizer input determines the LOS response time.

Jitter Specifications

The ADN2819 CDR is designed to achieve the best bit-error-rate (BER) performance and has exceeded the jitter transfer, generation, and tolerance specifications proposed for SONET/SDH equipment defined in the Telcordia Technologies specification.

Jitter is the dynamic displacement of digital signal edges from their long-term average positions, measured in UI (Unit Intervals) where 1 UI = 1 Bit Period. Jitter on the input data can cause dynamic phase errors on the recovered clock sampling edge. Jitter on the recovered clock causes jitter on the re-timed data.

The following section briefly summarizes the specifications of the jitter transfer, tolerance, and generation in accordance with the Telcordia document (GR-253-CORE, Issue 3, September 2000) for the optical interface at the equipment level and the ADN2819 performance with respect to those specifications..

Jitter Generation

The jitter generation specification limits the amount of jitter that can be generated by the device with no jitter and wander applied at the input. For OC-48 devices, the bandpass filter has a 12 kHz high-pass cutoff frequency with a roll-off of 20 dB/decade, and a low-pass cutoff frequency of at least 20 MHz. The jitter generated shall be less than 0.01 UI RMS, and shall also be less than 0.1 UI pp.

Jitter Transfer

The jitter transfer function is the ratio of the jitter on the output signal to the jitter applied on the input signal versus the frequency. This parameter measures the limited amount of the jitter on an input signal that can be transferred to the output signal (See Figure-8).

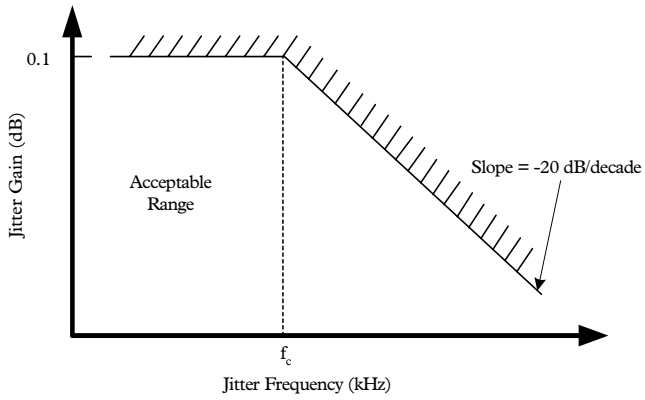


Figure 8. Jitter Transfer Curve

Jitter Tolerance

The jitter tolerance is defined as the peak-to-peak amplitude of the sinusoidal jitter applied on the input signal that causes a 1 dB power penalty. This is a stress test intended to ensure no additional penalty is incurred under the operating conditions. (See Figure-9). Figure 10 shows the typical OC-48 jitter tolerance performance of the ADN2819.

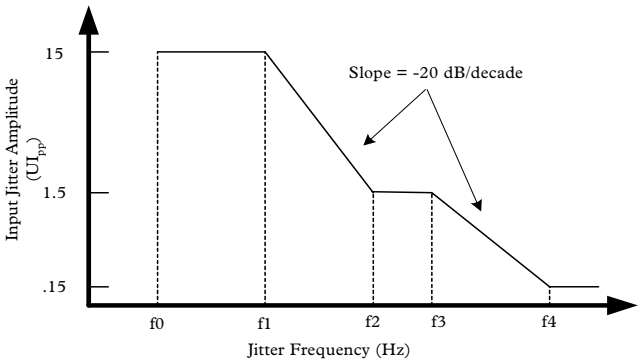


Figure 9. SONET Jitter Tolerance Mask

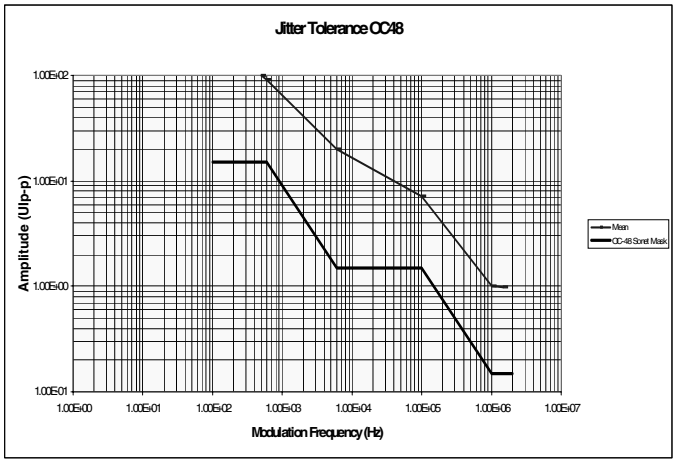


Figure 10. ADN2819 OC-48 Jitter Tolerance Curve

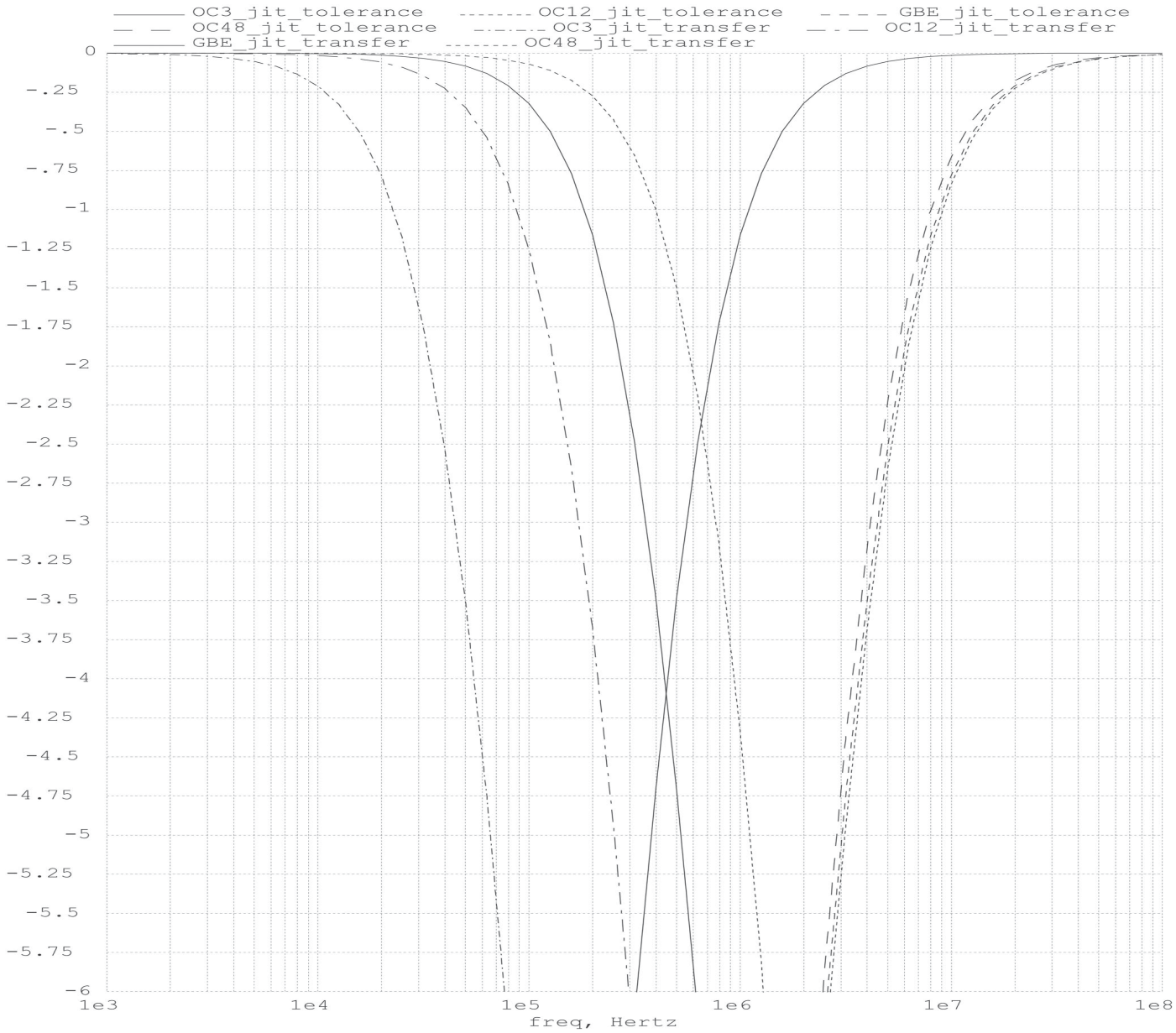


Figure 11. ADN2819 Jitter Transfer and Jitter Tracking BW

	Jitter Transfer			Jitter Tolerance				
Rate	**SONET Spec (f_C)**	**ADN2819**	**Implementation Margin**	**Mask Corner Frequency**	**ADN2819**	**SONET Spec**	**ADN2819**	**Implementation Margin***
OC48	2MHz	660kHz	3.0	1MHz	4.8MHz	0.15UIpp	1.0UIpp	6.67
OC12	500kHz	167kHz	3.0	250kHz	4.8MHz	0.15UIpp	1.0UIpp	6.67
OC3	130kHz	41kHz	3.2	65kHz	600kHz	0.15UIpp	1.0UIpp	6.67

* Jitter Tolerance Measurements Limited by Test Equipment Capabitilities

Table 1. Jitter Transfer and Tolerance: Sonet Spec -v- ADN2819

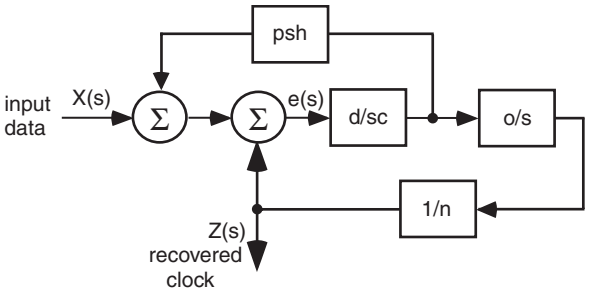
THEORY OF OPERATION

The ADN2819 is a delay- and phase-locked loop circuit for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops which share a common control voltage. A high speed delay- locked loop path uses a voltage controlled phase shifter to track the high frequency components of input jitter. A separate phase control loop, comprised of the vco, tracks the low frequency components of input jitter. The initial frequency of the vco is set by yet a third loop which compares the vco frequency with the reference frequency and sets the coarse tuning voltage. The jitter tracking phase-locked loop controls the vco by the fine tuning control.

The delay- and phase- loops together track the phase of the input data signal. For example, when the clock lags input data, the phase detector drives the vco to higher frequency, and also, increases the delay through the phase shifter: these actions both serve to reduce the phase error between the clock and data. The faster clock picks up phase while the delayed data loses phase. Since the loop filter is an integrator, the static phase error will be driven to zero.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second order phase-locked loop, and this zero is placed in the feedback path and thus, does not appear in the closed-loop transfer function. Jitter peaking in a conventional second order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Since this circuit has no zero in the closed-loop transfer, jitter peaking is minimized.

The delay- and phase- loops together simultaneously provide wide-band jitter accommodation and narrow-band jitter filtering. The linearized block diagram in Figure 12 shows the jitter transfer function , Z(s)/X(s), is a second order low pass providing excellent filtering. Note the jitter transfer has no zero, unlike an ordinary second order phase-locked loop. This means that the main PLL loop has low jitter peaking, see Figure 13. This makes this circuit ideal for signal regenerator applications where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.



d = phase detector gain
o = VCO gain
c = loop integrator
psh = phase shifter gain
n = divide ratio

Jitter Transfer Function

$$\frac{Z(s)}{X(s)} = \frac{1}{s^2\frac{cn}{do} + s\frac{n\,psh}{o} + 1}$$

Tracking Error Transfer Function

$$\frac{e(s)}{X(s)} = \frac{s^2}{s^2 + s\frac{d\,psh}{c} + \frac{do}{cn}}$$

Figure 12. ADN2819 PLL/DLL Architecture

The error transfer, e(s)/X(s), has the same high pass form as an ordinary phase-locked loop. This transfer function is free to be optimized to give excellent wide-band jitter accommodation since the jitter transfer function, Z(s)/X(s), provides the narrow-band jitter filtering. See Table 1 for a table of error transfer bandwidths and jitter transfer bandwidths at the various data rates.

The delay- and phase- loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case the vco is frequency modulated and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the vco tuning range. A wider tuning range gives larger accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors, so the phase shifter remains close to the center of its range and thus contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the vco are not large enough to track input jitter. In this case the vco control voltage becomes large and saturates and the vco frequency dwells at one or the other extreme of its tuning range. The size of the vco tuning range, therefore has only a small effect on the jitter accommodation. The delay-locked loop control voltage is now larger, and so the phase shifter takes on the burden of tracking the input jitter. The phase shifter range, in UI, can be seen as a broad plateau on the jitter tolerance curve. The phase shifter has a minimum range of 2UI at all data rates.

The gain of the loop integrator is small for high jitter frequencies, so that larger phase differences are needed to make the loop control voltage big enough to tune the range of the phase shifter. Large phase errors at high jitter frequencies cannot be tolerated. In this region the gain of the integrator determines the jitter accommodation. Since the gain of the loop integrator declines linearly with frequency, jitter accommodation is lower with higher jitter frequency. At the highest frequencies, the loop gain is very small, and little tuning of the phase shifter can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error, and the residual loop jitter generation. The jitter accommodation is roughly 0.5UI in this region. The corner frequency between the declining slope and the flat region is the closed loop bandwidth of the delay-locked loop, which is roughly 5MHz for OC-12, OC48 and GbE data rates and 600kHz for OC-3 data rates.

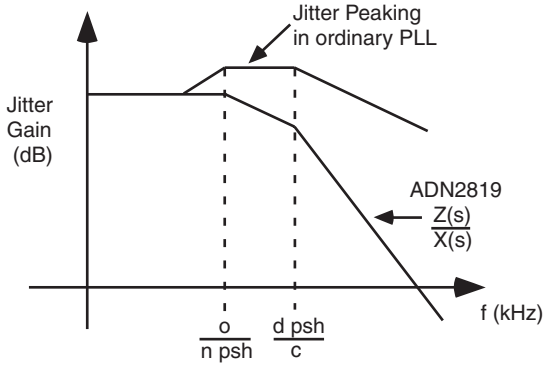


Figure 13. ADN2819 Jitter Response -vs- Conventional PLL

FUNCTIONAL DESCRIPTION

Multi-Rate Clock and Data Recovery

The ADN2819 will recover clock and data from serial bit streams at OC-3, OC-12, OC48, GbE data rates as well as the 15/14 FEC rates. The output of the 2.5GHz VCO is divided down in order to support the lower data rates. The data rate is selected by the SEL[2..0] inputs, see Table 2.

SEL[2..0]	Rate	Frequency (MHz)
000	OC-48	2488.32
001	GbE	1250.00
010	OC-12	622.08
011	OC-3	155.52
100	OC-48 FEC	2666.06
101	GbE FEC	1339.29
110	OC-12 FEC	666.51
111	OC-3 FEC	166.63

Table 2. Data Rate Selection

Limiting Amplifier

The limiting amplifier has differential inputs (PIN/NIN), which are internally terminated with 50 ohms to an on chip voltage reference (VREF = 0.6V typically). These inputs are normally AC coupled, although DC coupling is possible , as long as the input common mode voltage remains above 0.4V (see Figures 22-24 in the Applications section). Input offset is factory trimmed to achieve better than 4mV typical sensitivity with minimal drift. The limiting amplifier can be driven differentially or single-ended.

Slice Adjust

The Quantizer Slicing level can be offset by +/- 100mV to mitigate the effect of ASE (amplified spontaneous emission) noise by applying a differential voltage input of +/-0.8V to 'SLICEP/N' inputs. If no adjustment of the slice level is needed, SLICEP/N should be tied to VCC.

Loss of Signal (LOS) Detector

The receiver front end Level Signal Detect circuit indicates when the input signal level has fallen below a user adjustable threshold. The threshold is set with a single external resistor from pin1, THRADJ, to VEE. The LOS comparator trip point -vs- resistor value is illustrated in figure 3, (this is only valid for SLICEP=SLICEN=VCC). If the input level to the ADN2819 drops below the programmed LOS threshold, SDOUT (pin45) will indicate the loss of signal condition with a logic “1”. The LOS response time is ~300ns by design but will be dominated by the RC time constant in AC coupled applications.

If the LOS detector is used, the Quantizer Slice Adjust pins must both be tied to VCC. This is to avoid interaction with the LOS threshold level.

Note that it is not expected to use both LOS and Slice Adjust at the same time: systems with optical amplifiers need the slice adjust to evade ASE. However, a loss of signal in an optical link that uses optical amplifiers causes the optical amplifier output to be full scale noise. Under this condition the LOS would not detect the failure. In this case the Loss of Lock signal will indicate the failure because the CDR circuitry will not be able to lock onto a signal that is full scale noise.

Reference Clock

There are three options for providing the reference frequency to the ADN2819; differential clock, single-ended clock, or crystal oscillator. See Figures14-16 for example configurations.

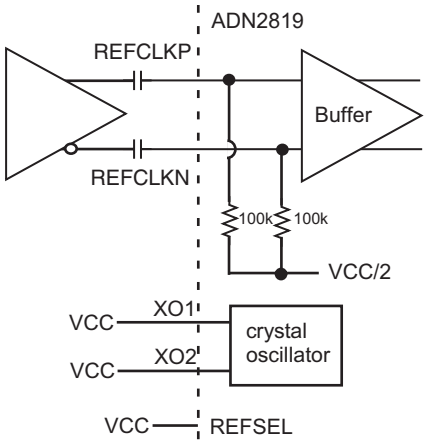


Figure 14. Differential REFCLK Configuration

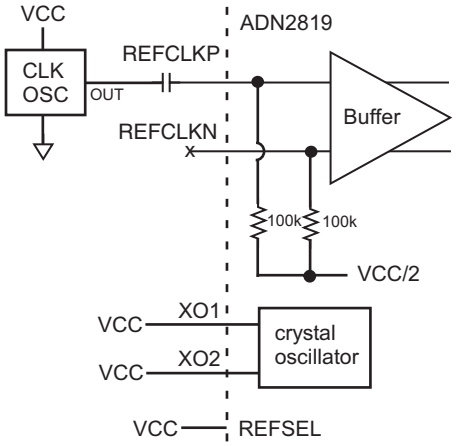


Figure 15. Single-ended REFCLK Configuration

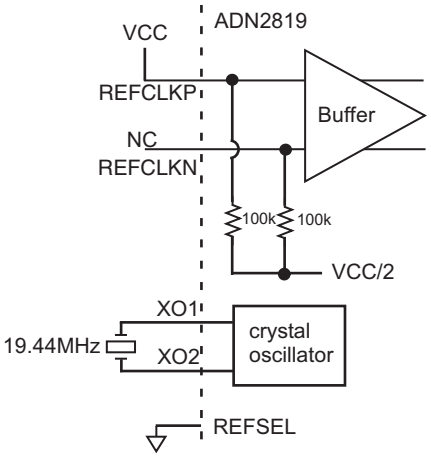


Figure 16. Crystal Oscillator Configuration

The ADN2819 can accept any of the following reference clock frequencies: 19.44 MHz, 38.88MHz, 77.76MHz at LVTTL/ LVCMOS/LVPECL/LVDS levels or 155.52MHz at LVPECL/ LVDS levels via the REFCLKN/P inputs, independent of data rate (including gigabit Ethernet and wrapper rates). The input buffer accepts any differential signal with a peak to peak differential amplitude of greater than 100mV (e.g. LVPECL or LVDS) or a standard single ended low voltage TTL input, providing maximum system flexibility. The appropriate division ratio can be selected using the REFSEL0/1 pins, according to Table 3. Phase noise and duty cycle of the Reference Clock are not critical and 100ppm accuracy is sufficient.

An on-chip oscillator to be used with an external crystal is also provided, as an alternative to using the REFCLKN/P input. Details of the recommended crystal are given in Table 4.

REFSEL	REFSEL[1..0]	Applied Reference Frequency(MHz)
1	00	19.44
1	01	38.88
1	10	77.76
1	11	155.52
0	XX	REFCLKP/N inactive, use 19.44MHz XTAL oscillator on pins XO1, XO2 (pull REFCLKP to VCC)

Table 3. Reference Frequency Selection

Parameter	Value
Mode	Series Resonant
Frequency/Overall Stability	19.44MHz ± 50ppm
Frequency Accuracy	± 50ppm
Temperature Stability	
Aging	
ESR	20 Ω max

Recommended manufacturer:
Raltron (305) 593-6033
Part Number: H10S-19.440-S-EXT-AD1

Table 4. Required Crystal Specifications

REFSEL must be tied to VCC when the REFCLKN/P inputs are active, or tied to VEE when the crystal oscillator is used. No connection between the XO pin and REFCLK input is necessary (see figures 14-16). Please note that the crystal should operate in series resonant mode, which renders it insensitive to external parasitics. No trimming capacitors are required.

Lock Detector Operation

The lock detector monitors the frequency difference between the VCO and the reference clock, and de-asserts the 'Loss of Lock' signal when the VCO is within 500ppm of center frequency (see figure 17). This enables the phase loop which pulls the VCO frequency in the remaining amount and also acquires phase lock. Once locked, if the input frequency error exceeds 1000ppm (0.1%), the 'Loss of Lock' signal is re-asserted and control returns to the frequency loop which will re-acquire, and maintain a stable clock signal at the output.

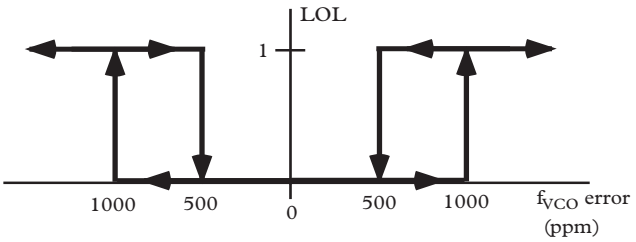


Figure 17. Transfer Function of LOL

The frequency loop requires a single external capacitor between CF1 and CF2. The capacitor specification is given in Table 5.

Parameter	Value
Temp Range	-40°C to 85°C
Capacitance	>3.0µF
Leakage	<80nA
Rating	>6.3V

Recommended manufacturer:
Murata Electronics (770) 436-1300
Part Number: GRM32RR71C475LC01

Table 5. Recommended Cf Capacitor Specification

Squelch Mode

When the 'Squelch' input is driven to a TTL high state, both the clock and data outputs are set to the zero state, to suppress downstream processing. If desired, this pin can be directly driven by the LOS (Loss-Of-Signal) detector output (SDOUT). If the Squelch function is not required, the pin should be tied to VEE.

Test Modes: Bypass & Loopback

When the 'Bypass' input is driven to a TTL high state, the Quantizer output is connected directly to the buffers driving the Data Out pins, thus bypassing the clock recovery circuit (Figure 18). This feature can help the system to deal with non standard bit rates.

The loopback mode can be invoked by driving the 'LOOPEN' pin to a TTL high state, which facilitates system diagnostic testing. This will connect the Test inputs (TDINP/N) to the clock and data recovery circuit (per Figure 18). The Test inputs have internal 50Ω terminations and can be left floating when not in use. TDINP/N are CML inputs and can only be DC coupled when being driven by CML outputs. The TDINP/N inputs must be AC coupled if being driven by anything other than CML outputs.

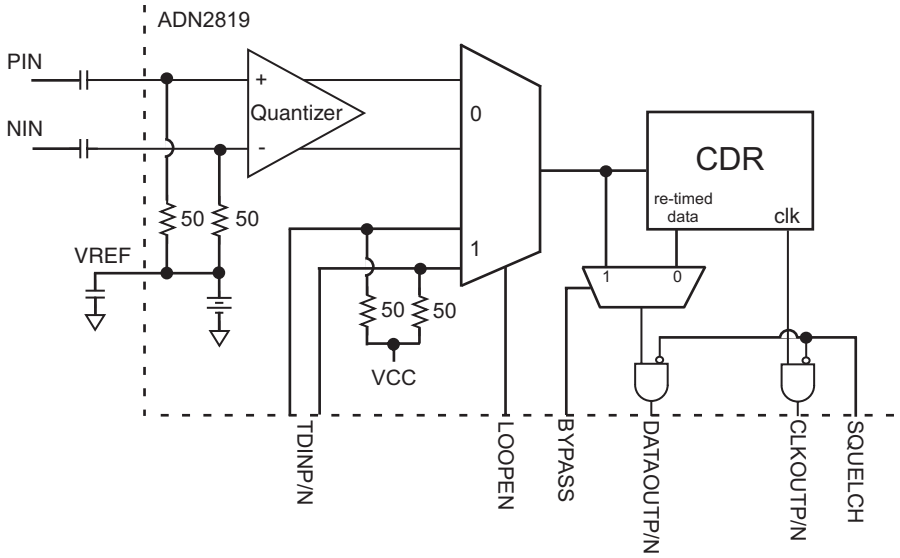


Figure 18. ADN2819 Test Modes

APPLICATIONS INFORMATION

PCB Design Guidelines

Proper RF PCB design techniques must be used for optimal performance.

Power Supply Connections and Ground Planes

Use of one low impedance ground plane to both analog and digital grounds is recommended. The VEE pins should be soldered directly to the ground plane to reduce series inductance. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias may be used in parallel to reduce the series inductance, especially on pins 33 and 34 which is the ground return for the output buffers.

Use of a 10µF electrolytic capacitor between VCC and GND is recommended at the location where the 3.3V supply enters the PCB. Use of 0.1µF and 1nF ceramic chip capacitors should be placed between IC power supply VCC and GND as close as possible to the ADN2819 VCC pins. Again, if connections to the supply and ground is made through vias, the use of multiple vias in parallel will help to reduce series inductance. Especially on pins 35 and 36 which supply power to the high speed CLKOUTP/N and DATAOUTP/N output buffers. Refer to the schematic in Figure 19 for recommended connections.

Transmission Lines

Use of 50Ω transmission lines are required for all high frequency input and output signals to minimize reflections; PIN, NIN, CLKOUTP, CLKOUTN, DATAOUTP, DATAOUTN (also REFCLKP, REFCLKN for a 155.52MHz refclk). It is also recommended that the PIN/NIN input traces are matched in length and that the CLKOUTP/N and DATAOUTP/N output traces are matched in length. All high speed CML outputs, CLKOUTP/N and DATAOUTP/N, also require 100Ω back termination chip resistors connected between the output pin and VCC. These resistors should be placed as close as possible to the output pins. These 100Ω resistors are in parallel with on-chip 100Ω termination resistors to create a 50Ω back termination (See Figure 20).

The high speed inputs, PIN and NIN, are internally terminated with 50Ω to an internal reference voltage (see Figure 21). A 0.1µF is recommended between VREF, pin 4, and GND to provide an AC ground for the inputs.

As with any high speed mixed-signal design, take care to keep all high speed digital traces away from sensitive analog nodes.

Soldering Guidleines for Chip-Scale Package

The lands on the 48 LFCSP are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This will ensure that the solder joint size is maximized. The bottom of the chip scale package has a central exposed pad. The pad on the printed circuit board should be at least as large as this exposed pad. The user must connect the exposed pad to analog VCC. If vias are used, they should be incorporated in the pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz. copper to plug the via.

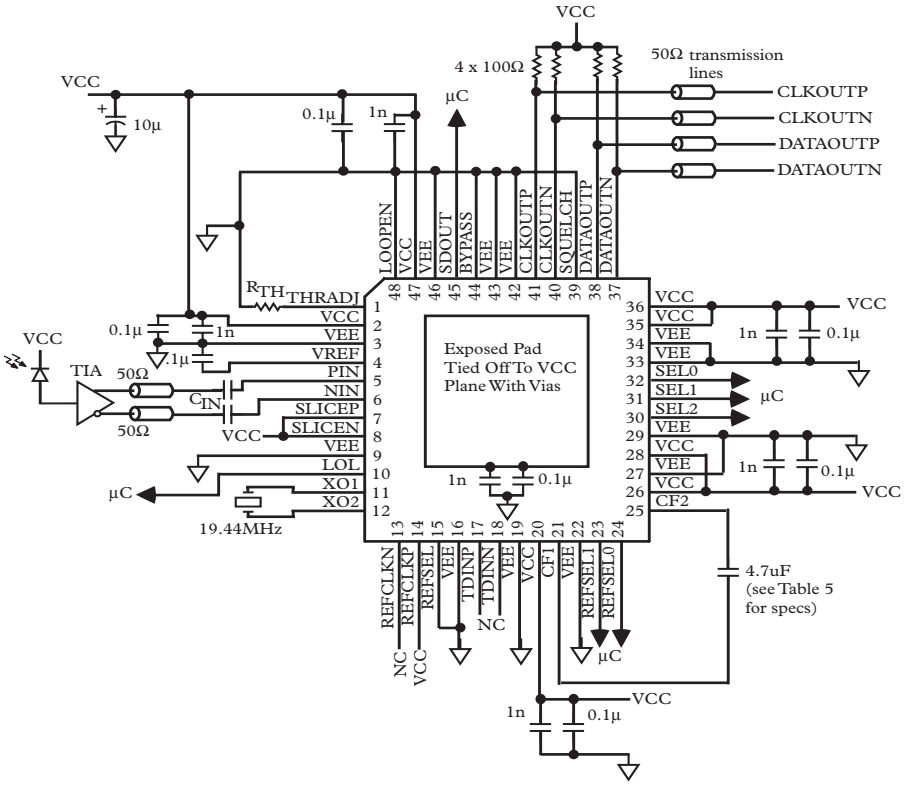


Figure 19. ADN2819 Typical Application Circuit

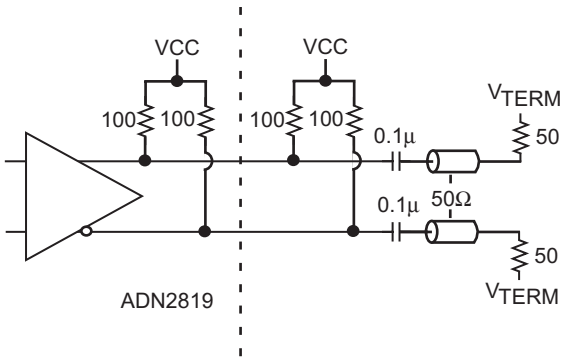


Figure 20. ADN2819 AC-Coupled Output Configuration

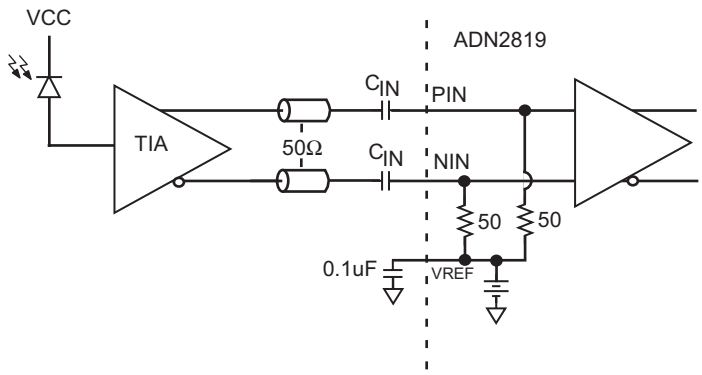
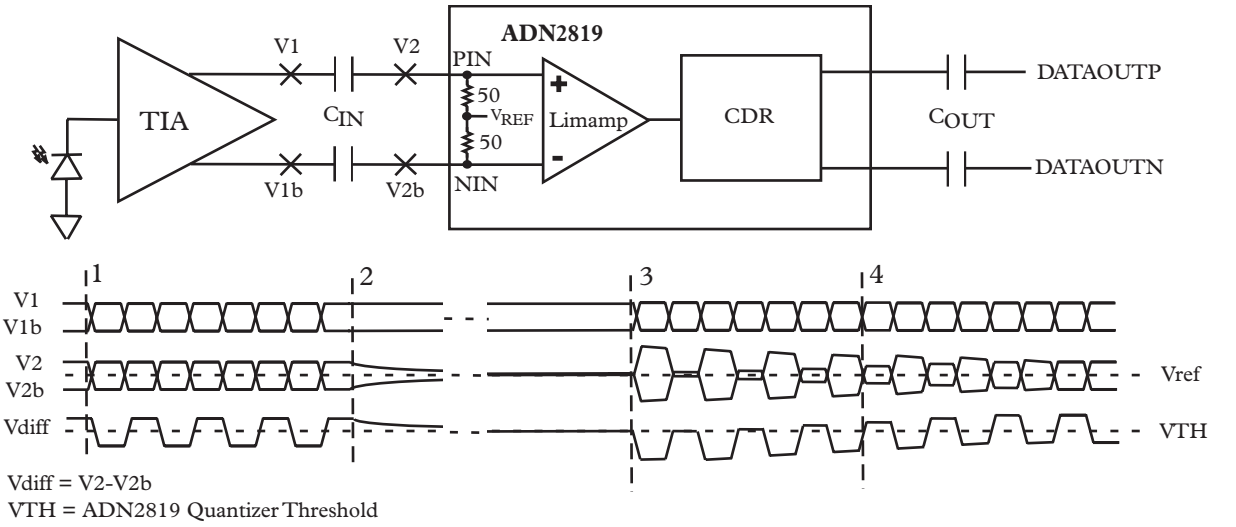


Figure 21. ADN2819 AC-Coupled Input Configuration

Choosing AC Coupling Capacitors

The choice of AC coupling capacitors at the input (PIN, NIN) and output (DATAOUTP, DATAOUTN) of the ADN2819 must be chosen such that the device works properly at the lower OC3 and higher OC48 data rates. When choosing the capacitors, the time constant formed with the two 50 Ohm resistors in the signal path must be considered. When a large number of consecutive identical digits (CIDs) are applied, the capacitor voltage can droop due to baseline wander (See Figure 22), causing pattern dependent jitter (PDJ).

For the ADN2819 to work robustly at OC3 *and* OC48 a minimum capacitor of 1.6uF to PIN/NIN, and 0.1uF on DATAOUTP/DATAOUTN should be used. This is based on the assumption that 1000 CIDs must be tolerated, and that the PDJ should be limited to 0.01UIpp.



NOTES:
1. During data patterns with high transition density, differential DC voltage at V1 and V2 is zero.
2. When the output of the TIA goes to CID, V1 and V1b are driven to different DC levels. V2 and V2b discharge to the Vref level which effectively introduces a differential DC offset across the AC coupling capacitors.
3. When the burst of data starts again, the differential DC offset across the AC coupling capacitors is applied to the input levels causing a DC shift in the differential input. This shift is large enough such that one of the states, either HI or LO depending on the levels of V1 and V1b when the TIA went to CID, is cancelled out. The quantizer will not recognize this as a valid state.
4. The DC offset slowly discharges until the differential input voltage exceeds the sensitivity of the ADN2819. The quantizer will be able to recognize both HI and LO states at this point.

Figure 22. Example of Baseline Wander

DC Coupled Application

The inputs to the ADN2819 can also be DC coupled. This may be necessary in burst mode applications where there are long periods of CIDs and baseline wander can not be tolerated. If the inputs to the ADN2819 are DC coupled, care must be taken not to violate the input range and common mode level requirements of the ADN2819 (see Figures 23-25). If DC coupling is required, and the output levels of the TIA do not adhere to the levels shown in figure 24 and 25, then there will need to be level shifting and/or an attenuator between the TIA outputs and the ADN2819 inputs.

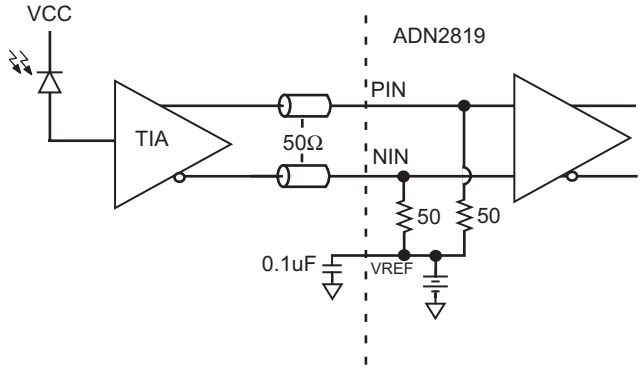


Figure 23. ADN2819 with DC Coupled Inputs

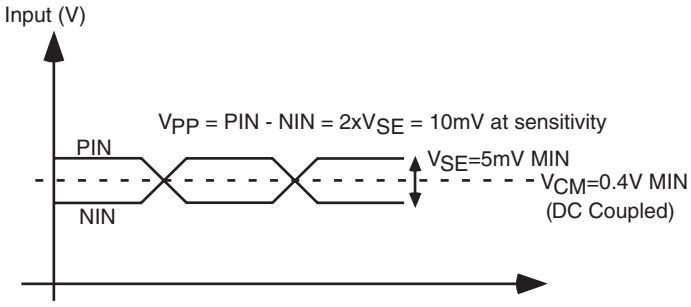


Figure 24. Minimum Allowed DC Coupled Input Levels

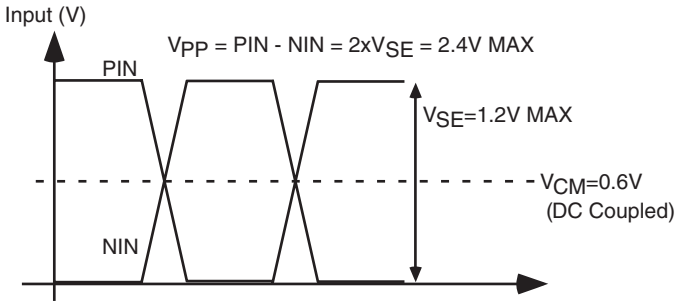
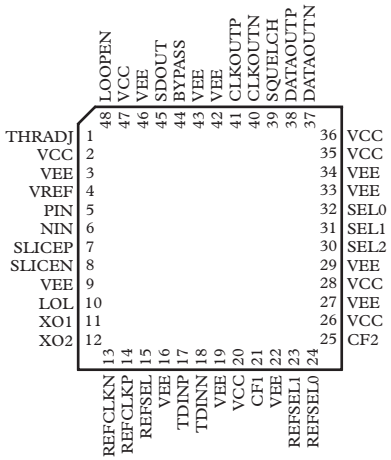


Figure 25. Maximum Allowed DC Coupled Input Levels

LOL Toggling during loss of input data

If the input data stream is lost due to a break in the optical link (or for any reason), the clock output from the 2819 will stay within 1000ppm of the VCO center frequency as long as there is a valid reference clock. The LOL pin will toggle at a rate of several kHz. This is because the LOL pin will toggle between a logic "1" and a logic "0" while the frequency loop and phase loop swap control of the VCO. The chain of events are as follows:

- The ADN2819 is locked to the input data stream; LOL=0
- The input data stream is lost due to a break in the link. The VCO frequency drifts until the frequency error is greater than 1000ppm. LOL is asserted to a logic 1 as control of the VCO is passed back to the frequency loop.
- The frequency loop pulls the VCO to within 500ppm of its center frequency. Control of the VCO is passed back to the phase loop and LOL is de-asserted to a logic 0.
- The phase loop tries to acquire, however, there is no input data present so the VCO frequency drifts.
- The VCO frequency drifts until the frequency error is greater than 1000ppm. LOL is asserted to a logic 1 as control of the VCO is passed back to the frequency loop.This process is repeated until a valid input data stream is re-established.



Pin Number	Name	Type	Description
2, 26, 28, Pad	VCC	P	Analog Supply
20, 47	VCC	P	Digital Supply
35, 36	VCC	P	Output Driver Supply
3, 9, 16, 19, 22, 27, 29, 33, 34, 42, 43, 46	VEE	P	Ground
1	THRADJ	AI	LOS threshold setting resistor
4	VREF	AO	Internal Vref voltage. Decouple to GND with 0.1uF cap
5	PIN	AI	Differential data input. CML
6	NIN	AI	Differential data input. CML
7	SLICEP	AI	Differential slice level adjust input
8	SLICEN	AI	Differential slice level adjust input
10	LOL	DO	Loss of lock indicator. LVTTL Active High
11	XO1	AO	Crystal oscillator
12	XO2	AO	Crystal oscillator
13	REFCLKN	DI	Differential refclk input. LVTTL, LVCMOS, LVPECL, LVDS (LVPECL, LVDS only at 155.52MHz)
14	REFCLKP	DI	Differential refclk input. LVTTL, LVCMOS, LVPECL, LVDS (LVPECL, LVDS only at 155.52MHz)
15	REFSEL	DI	Reference source select. "0" = on-chip oscillator with external crystal; "1" = external clock source, LVTTL
17	TDINP	AI	Differential test data input
18	TDINN	AI	Differential test data input
21	CF1	AO	Frequency loop capacitor
23	REFSEL1	DI	Reference frequency select, See Table XX. LVTTL
24	REFSEL0	DI	Reference frequency select, See Table XX. LVTTL
25	CF2	AO	Frequency loop capacitor
30	SEL2	DI	Data rate select, See Table XX. LVTTL
31	SEL1	DI	Data rate select, See Table XX. LVTTL
32	SEL0	DI	Data rate select, See Table XX. LVTTL
37	DATAOUTN	DO	Differential recovered data output. CML
38	DATAOUTP	DO	Differential recovered data output. CML
39	SQUELCH	DI	Disable clock and data outputs. Actice high. LVTTL
40	CLKOUTN	DO	Differential recovered clock output. CML
41	CLKOUTP	DO	Differential recovered clock output. CML
44	BYPASS	DI	Bypass CDR mode. Active high. LVTTL
45	SDOUT	DO	Loss of signal detect output. Active high. LVTTL
48	LOOPEN	DI	Enable test data inputs. Active high. LVTTL

Type: P = Power, AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output

MECHANICAL OUTLINE DIMENSIONS

Dimensions shown in inches and (millimeteres)