GoldStar
GOLDSTAR ELECTRON CO., LTD.

GMCD32100/L-60/70/80

1,048,576 WORDS × 32 BIT
CMOS DYNAMIC RAM CARD

Description

The GMCD32100 is a 4 megabyte, DRAM card organized as a 1M × 32 bit memory array. It may also be configured as a 2M × 16 bit memory array, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented.

For the × 16 application, the corresponding DQs and the corresponding $\overline{CAS}$ pins must be connected together (DQ0 to DQ16, DQ1 to DQ17, and DQ2 to DQ18 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). This card has CMOS buffers added to the all inputs to minimize loading caused by the card and ensure compatibility in a wide range of systems. $\overline{RAS}$ and data input/output remain compatible with TTL. Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the × 32 organization, the memory is a single array that may be divided into four separate bytes. In the × 16 organization, up to two banks, each with two separate bytes, may be independently selected, the others not selected remain in standby mode, drawing minimum power.

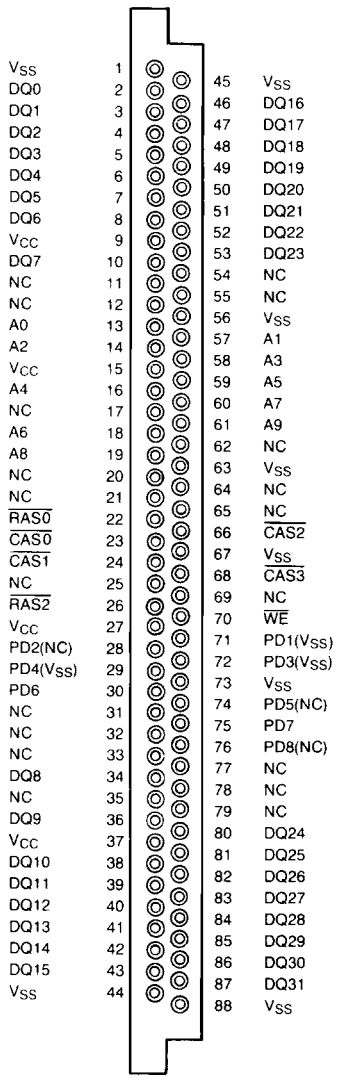
Features

- JEIDA, JEDEC and PCMCIA standard 88-pin DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- All outputs are fully TTL compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for × 16 or × 32 selectability
- FAST PAGE MODE operation
- Fast access time and cycle time (Unit: ns)

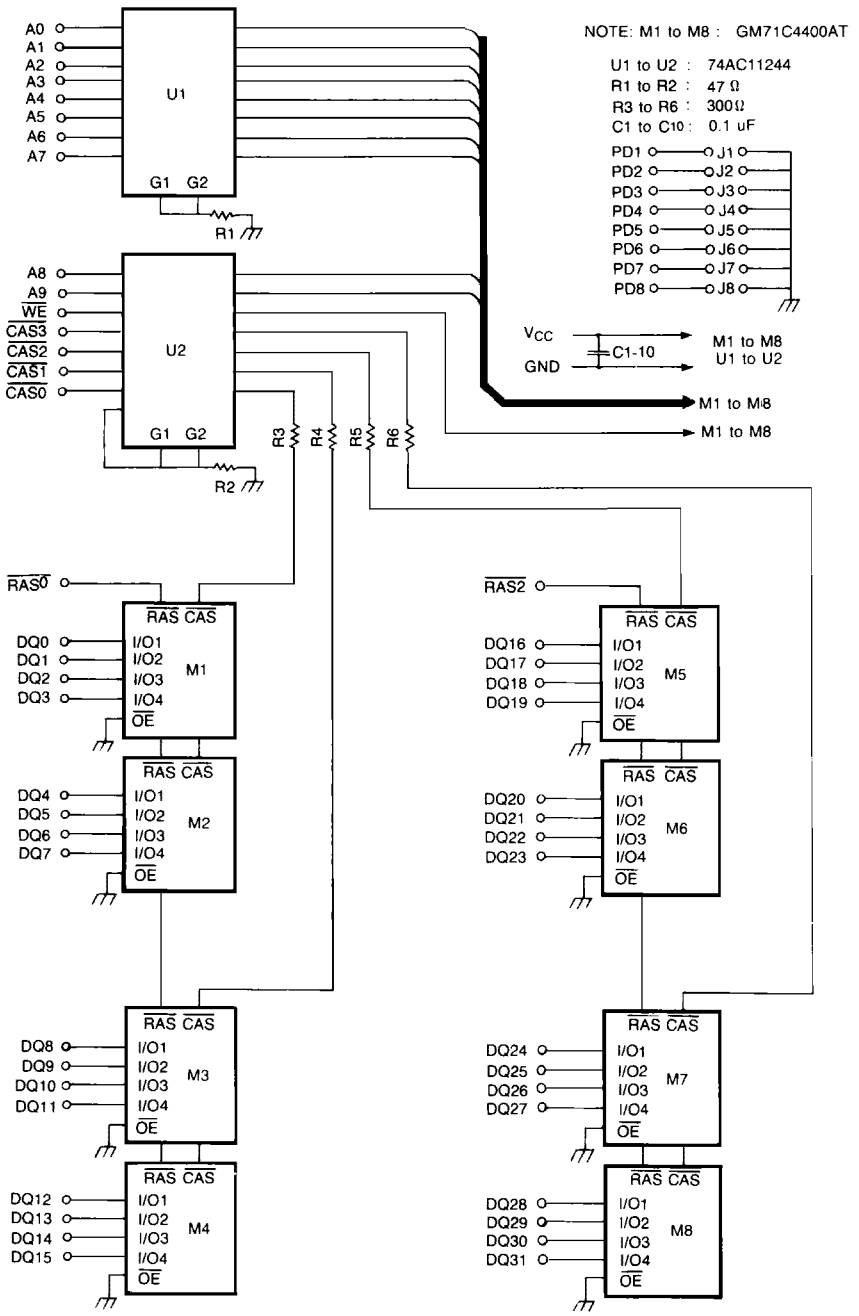
	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMCD32100-60	60	22	110	47
GMCD32100-70	70	27	130	52
GMCD32100-80	80	27	150	57

- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$ and HIDDEN
- Single +5V ± 5% power supply
- 1M × 32, 2 $\overline{RAS}$, 4 $\overline{CAS}$ organization Low power;
  Active: 5.1/4.7/4.3W (MAX)
  Standby: 47.25mW (CMOS level; MAX)
- Refresh cycle: 1024 cycles/16ms
  1024 cycles/128ms (L-series)

Pin Configuration



Block Diagram



Pin Description

Pin	Function	Pin	Function
A0 ~ A9	Address Input	PD1 ~ PD5	Presence Detect
DQ0 ~ DQ31	Data Inputs/Outputs	V_{CC}	Power Supply: +5V ± 5%
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS0}$ ~ $\overline{CAS3}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Read/Write Enable	$\overline{OE}$	Output Enable

Presence Detect Pins

Device	Configuration*					Speed		Refresh Control	
	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	
GMCD32100-60	V_{SS}	NC	V_{SS}	V_{SS}	NC	NC	NC	STANDARD	NC
GMCD32100-70	V_{SS}	NC	V_{SS}	V_{SS}	NC	V_{SS}	NC		
GMCD32100-80	V_{SS}	NC	V_{SS}	V_{SS}	NC	NC	V_{SS}	AUTO	V_{SS}

*Note: It means that the number of card address is 20, number of $\overline{RAS}$ and $\overline{CAS}$ address is each 10, and page depth is 1024.

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature Under Bios	0 ~ 55	°C
T_{STG}	Storage Temperature	-40 ~ 55	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-0.5 ~ 6.5	V
V_{CC}	Power Supply Voltage	-0.5 ~ 6.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	10	W

*Note: Stress greater than above "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended DC Operating Condition (T_A = 0 ~ 55°C)

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_{IH}	Input High Voltage	$\overline{CAS}$, $\overline{WE}$, Address	0.7*V_{CC}			V
		$\overline{RAS}$, DQ	2.4		6.5	V
V_{IL}	Input Low Voltage	$\overline{CAS}$, $\overline{WE}$, Address			0.3*V_{CC}	V
		$\overline{RAS}$, DQ	-1.0		0.8	V

Symbol	Parameter		Min	Typ	Max	Unit
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	900	mA	1,2
		70ns	—	820		
		80ns	—	740		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	17	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	900	mA	2
		70ns	—	820		
		80ns	—	740		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	60ns	—	900	mA	1,3
		70ns	—	820		
		80ns	—	740		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC}-0.2V)		—	9	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	900	mA	
		70ns	—	820		
		80ns	—	740		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	40	mA	1
$I_{I(L)}$	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 7V$) All Other Pins Not Under Test = 0V		−10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 7V$)		−10	10	μA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

Capacitance (V_{CC} = 5V ± 5%, T_A = 25°C, f = 1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (A0 ~ A9)	—	15	pF	1
C_{I2}	Input Capacitance ($\overline{WE}$)	—	15	pF	1
C_{I3}	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	—	37	pf	1
C_{I4}	Input Capacitance ($\overline{CAS0}$ ~ $\overline{CAS3}$)	—	15	pF	1,2
C_{DQ}	I/O Capacitance (DQn)	—	15	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Electrical Characteristics (V_{CC} = 5V ± 5%, T_A = 0 ~ 55°C, Notes 1,14)

The GMCD32100 writes data only in early write cycle (twcs ≥ twcs(min)).
Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMCD32100-60		GMCD32100-70		GMCD32100-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	150	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	60	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	22	10,000	27	10,000	27	10,000	ns	
t_{ASR}	Row Address Set-up Time	7	—	7	—	7	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	ns	
t_{ASC}	Column Address Set-up Time	7	—	7	—	7	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	38	20	43	20	53	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	23	15	28	17	33	ns	9
t_{RAH}	$\overline{RAS}$ Hold Time	22	—	27	—	27	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	17	—	17	—	17	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	16	—	16	—	16	ms	

Read Cycle

Symbol	Parameter	GMCD32100-60		GMCD32100-70		GMCD32100-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	–	22	–	27	–	27	ns	3,4
t_{AA}	Access Time from Column Address	–	37	–	42	–	47	ns	3,5
t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	–	0	–	0	–	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	10	–	10	–	10	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	37	–	42	–	47	–	ns	
t_{OFF}	Output Buffer Turn-off Time	–	20	–	20	–	20	ns	6

Write Cycle

Symbol	Parameter	GMCD32100-60		GMCD32100-70		GMCD32100-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
t_{WP}	Write Command Pulse Width	17	–	17	–	17	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	22	–	27	–	27	–	ns	
t_{DS}	Data-in Set-up Time	0	–	0	–	0	–	ns	11
t_{DH}	Data-in Hold Time	15	–	15	–	15	–	ns	11

Refresh Cycle

Symbol	Parameter	GMCD32100-60		GMCD32100-70		GMCD32100-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Time from $\overline{RAS}$ Refresh Cycle	17	–	17	–	17	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	–	10	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	–	10	–	10	–	ns	

Fast Page Mode Cycle

Symbol	Parameter	GMCD32100-60		GMCD32100-70		GMCD32100-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast-Page Mode Cycle Time	47	—	52	—	57	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Recharge Time	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	42	—	47	—	52	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	42	—	47	—	52	—	ns	

Notes:
1. AC measurements assume $t_T = 5ns$.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS} is not restrictive operating parameters. If is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
12. t_{RASC} is defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

TIMING WAVEFORMS

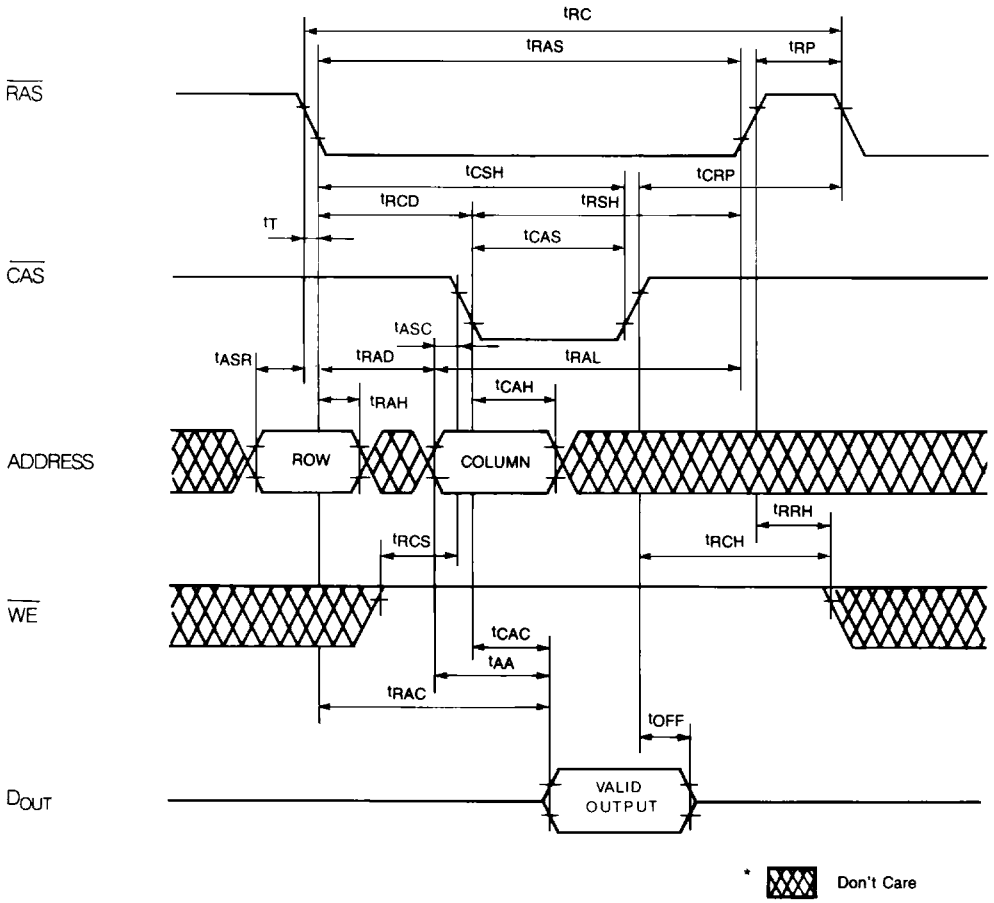


FIGURE 1. READ CYCLE

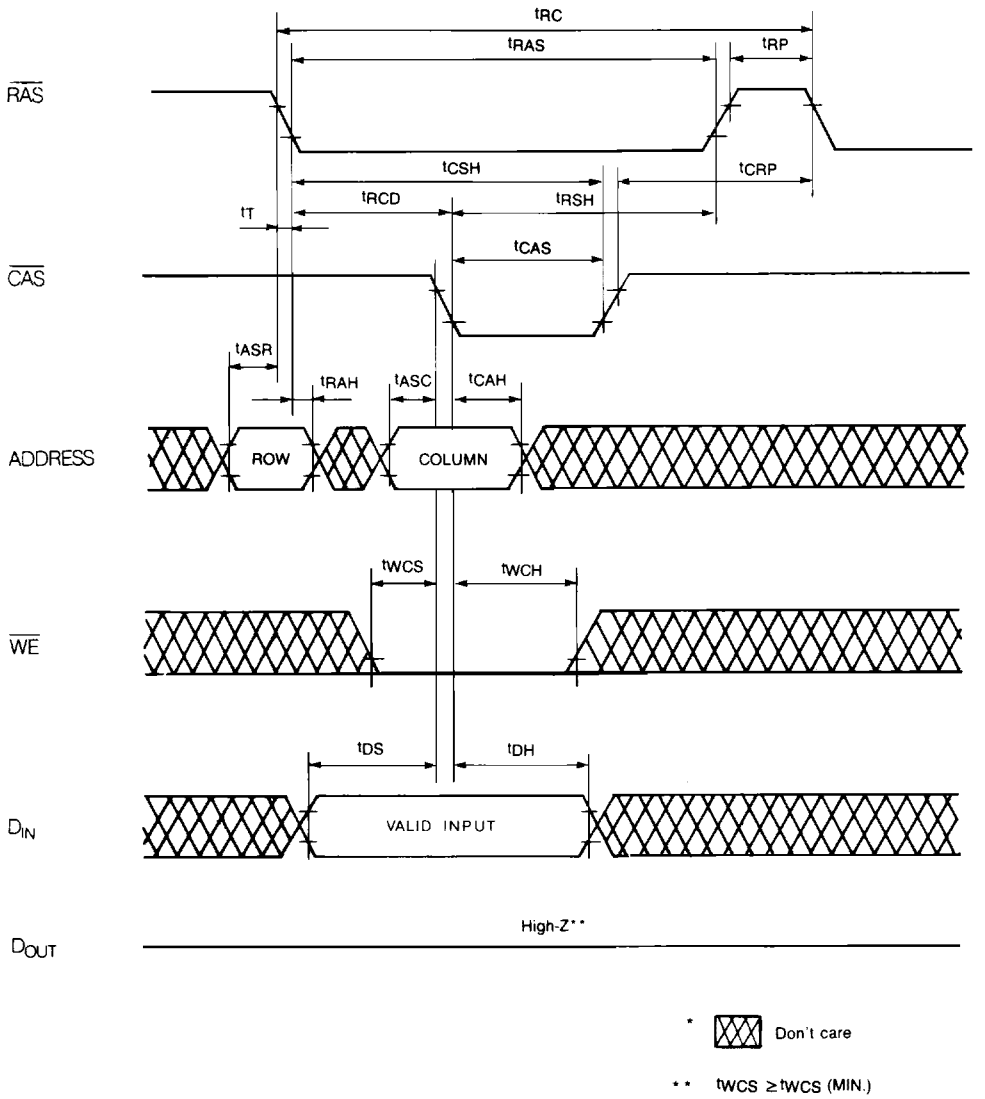


FIGURE 2. EARLY WRITE CYCLE

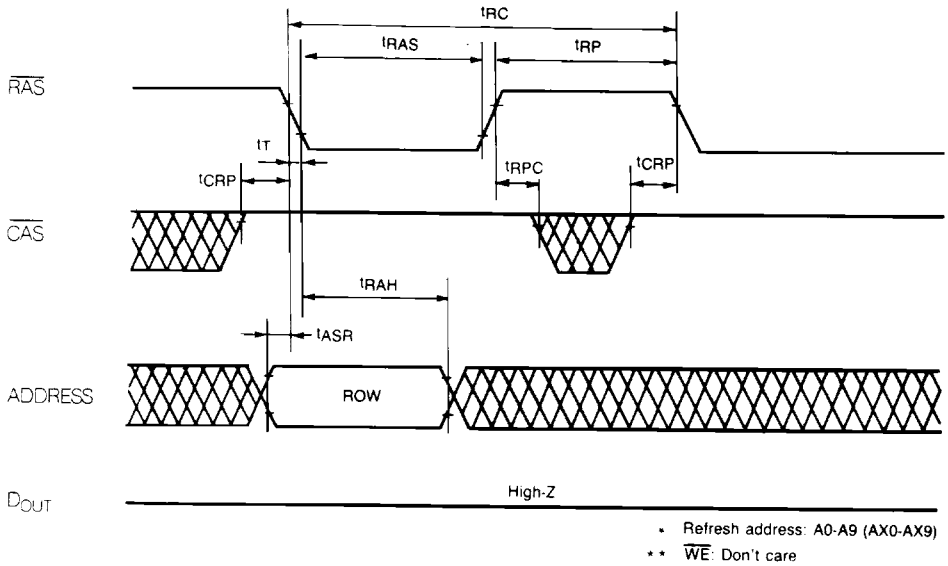


FIGURE 3. RAS-ONLY-REFRESH CYCLE

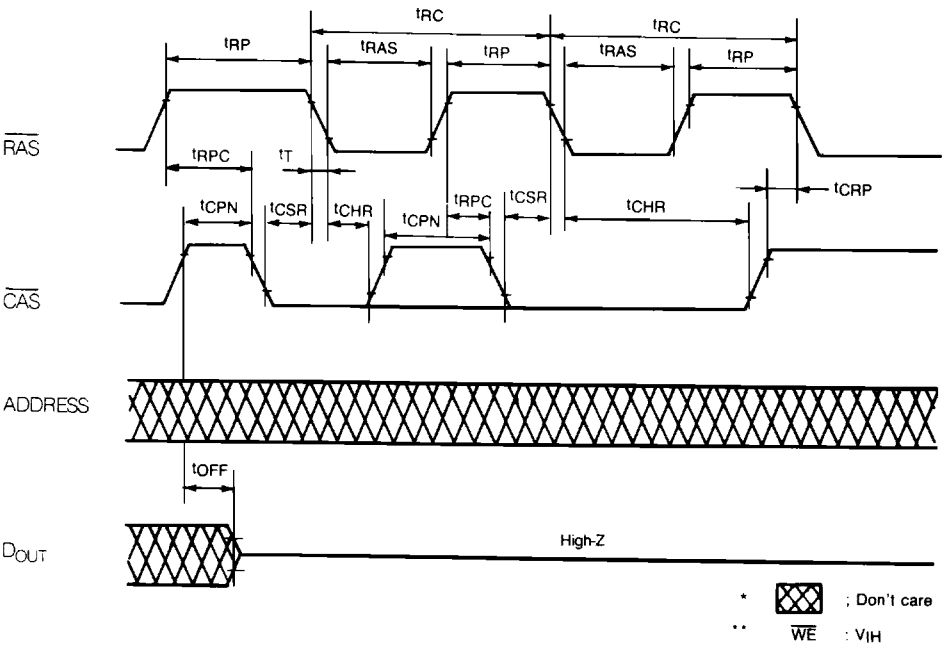


FIGURE 4. CAS-BEFORE-RAS REFRESH CYCLE

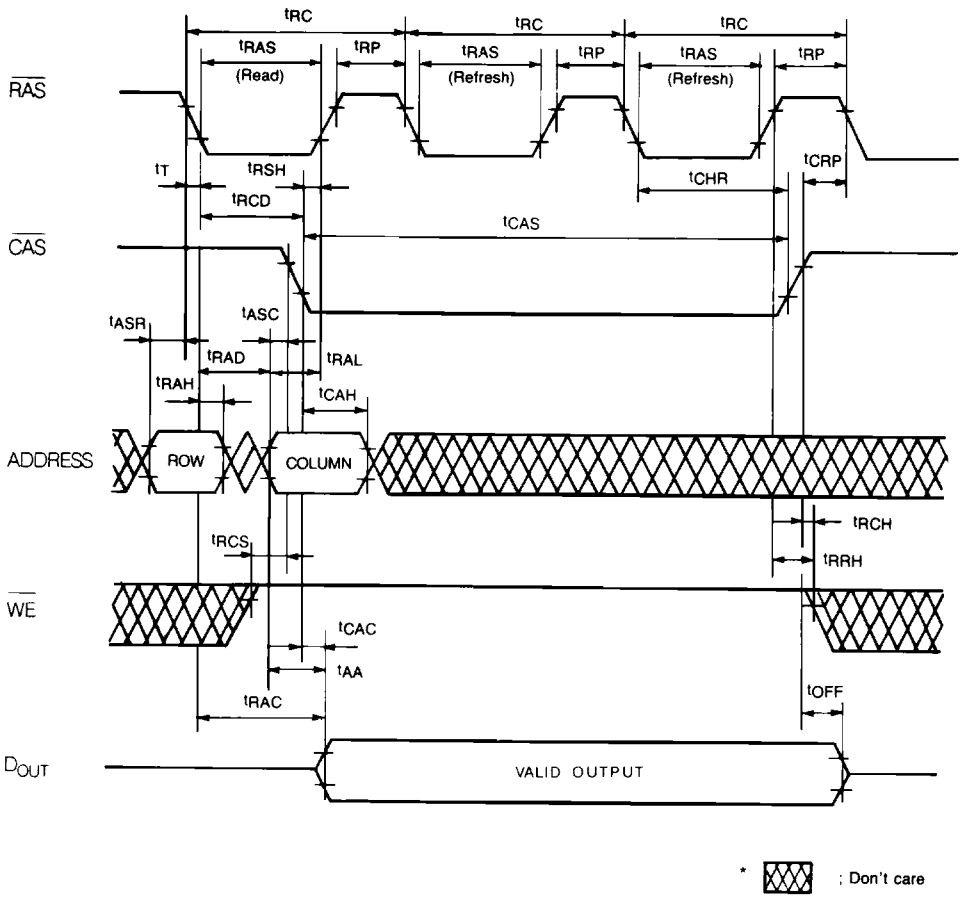


FIGURE 5. HIDDEN REFRESH CYCLE

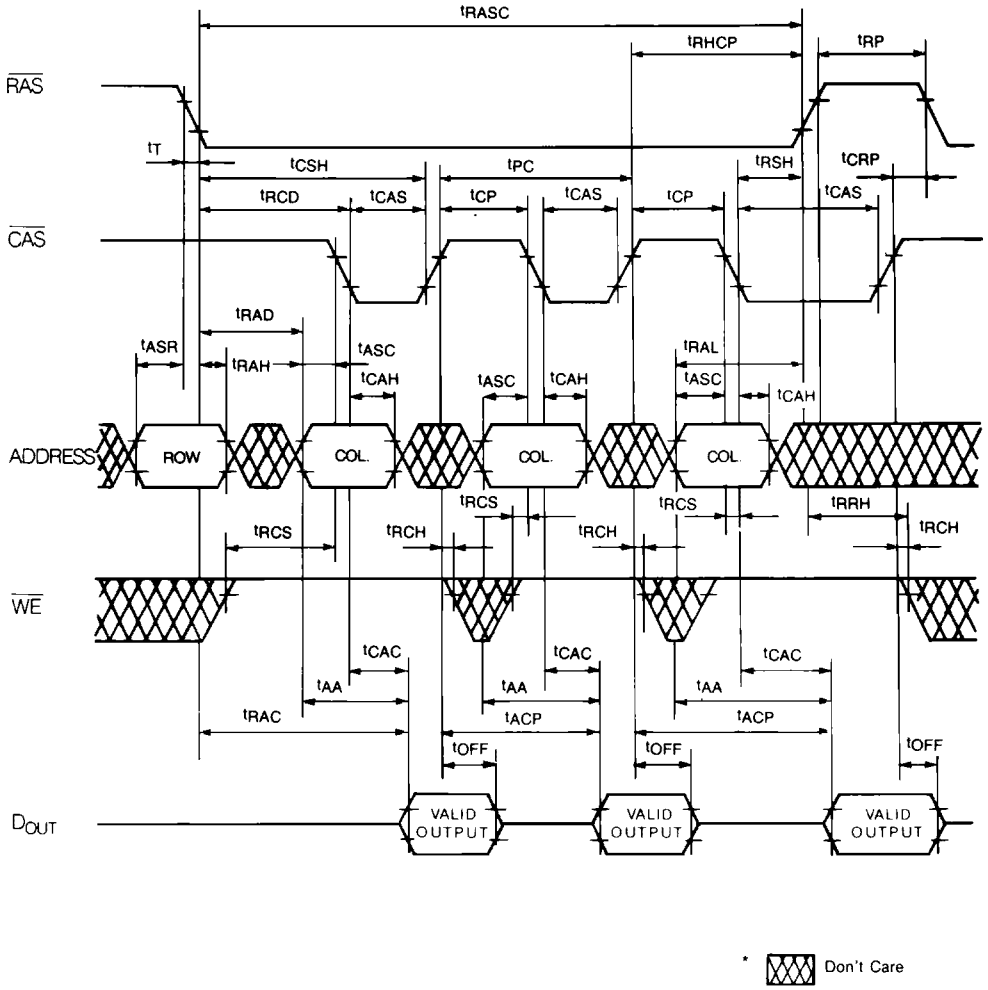


FIGURE 6. FAST PAGE MODE READ CYCLE

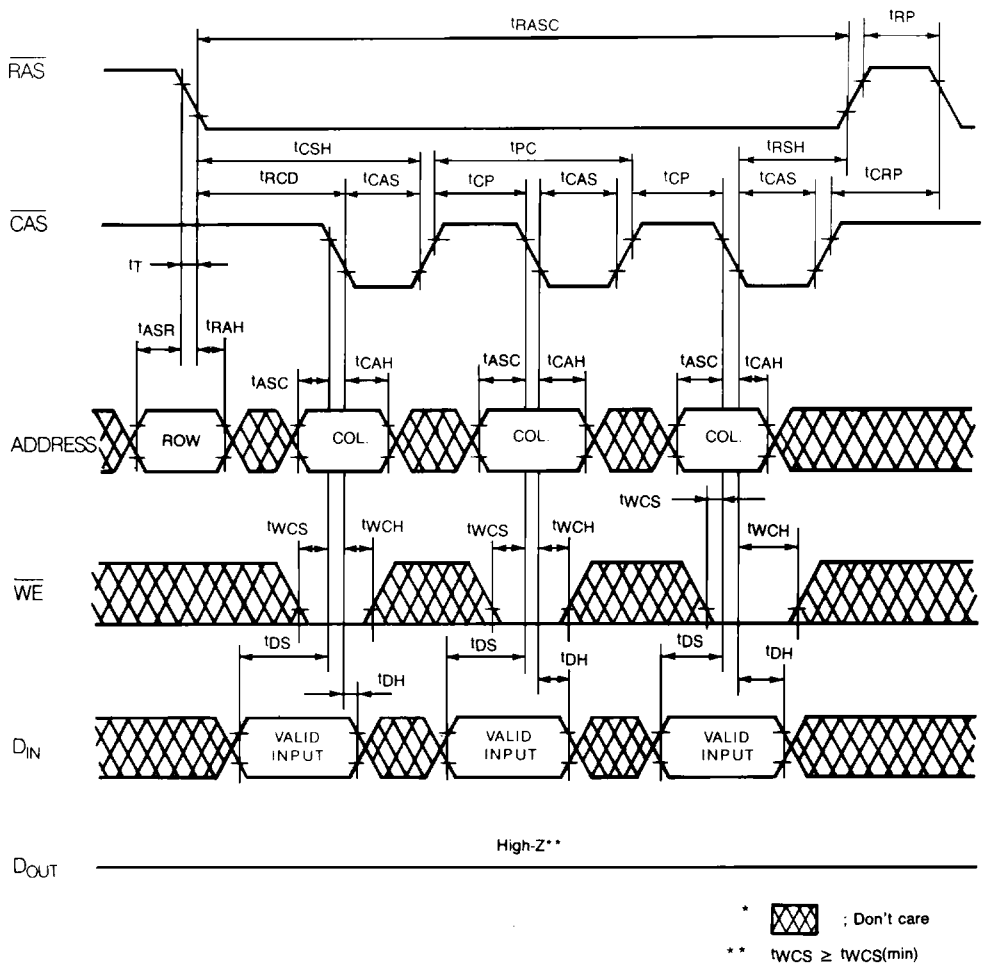


FIGURE 7. FAST PAGE MODE EARLY WRITE CYCLE

Dimension

Unit: mm (inches)