AN5520

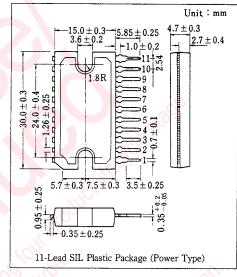
TV Vertical Deflection Output Circuit

Outline

The AN5520 is an integrated circuit designed for color TV vertical deflection output circuit. Combining with the deflection signal processing circuit AN5410 can facilitate the vertical output circuit design.

Features

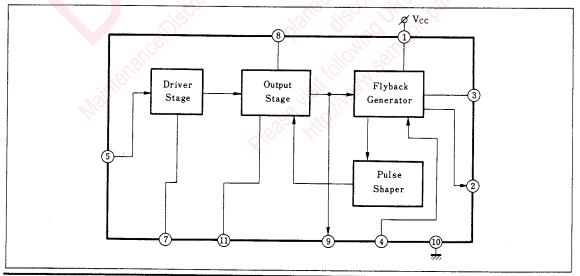
- Low power consumption, direct deflection coil driving capability (Flyback voltage two times as high as supply voltage is supplied during flyback period only)
- High breakdown voltage: 60 V



Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{cc}	7	Drive Tr. Collector
2	BLK Pulse Output	8	Supply Voltage for Output
3	Pulse Amp. Output	9	Output
4	Trigger Pulse Input	10	GND
5	Input	110	Output Tr. Base
6	NC		(2), "(b, "O), = "(l),

Block Diagram



■ Absolute Maximum Rating (Ta=25°C)

	Item	Symbol	Rat	ing	Unit
<u> </u>	Supply Voltage	V ₁₋₁₀	27	27.6	
17-ltomo	Circuit Voltage	V ₄₋₁₀	0	1.5	V
Voltage		V ₅₋₁₀	0	2.5	v
		V ₈₋₁₀	0	60	v
	Total Current Consumption	Itot	3	50	mA
Current	Circuit Current	I ₂	-1.0	1.0	mA
Current		I ₃	-900	900	mA _{p-p}
		I ₉	-900	900	_O mA
Power Dissi	pation	P_{D}	5	. 5	W
Temperatur	Operating Ambient Temperature	Topr	-20~	+70	°C
I emberatur	Storage Temperature	Tstg	-55~	+150	°C

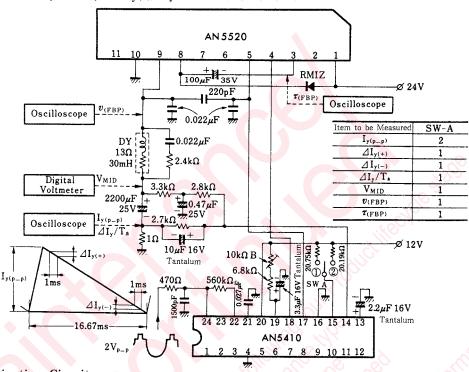
Note: ① and ② are flow-in and flow-out currents to/from the circuit, respectively.

■ Electrical Characteristics (Ta=25°C)

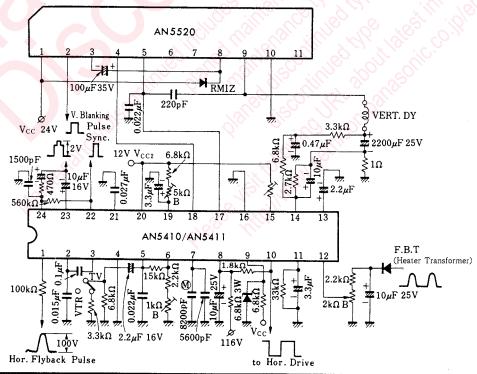
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Operating Ambient Temperature	Iy(p-p)	1	Ta=70 °C	1.31	1.45	1.59	A_{p-p}
Deflection Current Linearity	⊿ Iy(+)	1		60		110	mA _{p-p}
Deflection Current Linearity	⊿ Iy(-)	1		60		110	mA _{p-p}
Deflection Current Change with Ambient Temperature*	△ Iy/ Ta	1	$Ta = -20 \sim +70^{\circ}C$	-1.5		1.5	%
Center Voltage	VMID	1	60, 31, 70, 10,	11.9	12.4	12.9	v
Flyback Pulse Amplitude	V(FBP)	1	762 761 677 771	47		(0)	v
Flyback Pulse Width	T (BLP)	1	all all is a	0.9	1.02	1.08	ms
Static Circuit Current	Icq		$\begin{array}{c} V_{8-10} = 24V & & & & & & & & & & \\ V_{1-10} = 24V & & & & & & & & \\ V_{4-10} = 0V & & & & & & & \\ \end{array}$	7	15	30	mA
Output Tr Saturation	V ₈₋₉		$V_{8-10} = V_{1-10} = 24V, V_{4-10} = 0V$ 33\Omega between Pins@and\text{0}, $V_{5-10} = 0.3V$	7,0	3.0	4.0	v
Voltage	V ₉₋₁₀	-	$V_{8-10} = V_{1-10} = 24V, \ V_{4-10} = 0V$ 33\Omega between Pins(9) and (8), $V_{5-10} = 1.3V$		1.3	2.0	v
Q ₂₁ Saturation Voltage	V ₃₋₁₀		$V_{1-10} = 24V$, $1.2k\Omega$ between Pins①and③ $V_{4-10} = 0V$			0.5	V
Thermal Resistance	Rth(j-c)		ill man			8	°C/W

^{*} Design reference value

Test Circuit 1 $(I_{y(p-p)}, \Delta I_{y(+)}, \Delta I_{y(-)}, \Delta I_{y}/Ta, V_{MID}, \upsilon_{(FBP)}, \tau_{(BLP)})$



Application Circuit



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