HD74AC524 ● 8-Bit Registered Comparator

Preliminary

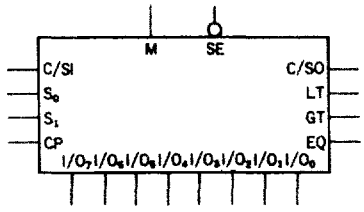
Description

The 'AC524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. The device functions are controlled by two control lines (S_0, S_1) to execute shift, load, hold, and read out.

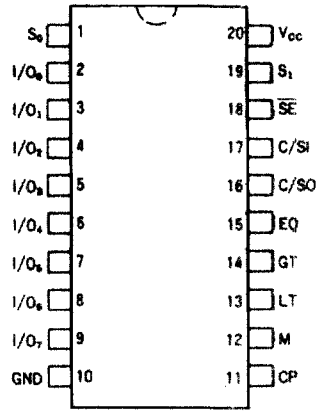
An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-HIGH, open drain outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow twos complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

- 8-Bit Bidirectional Register with Bus-Oriented Input-Output
- Independent Serial Input-Output to Register
- Register Bus Comparator with 'Equal to', 'Greater than' and 'Less than' Outputs.
- Cascadable in Groups of Eight Bits
- Open-Drain Comparator Outputs for AND-Wired Expansion
- Twos Complement or Magnitude Compare
- Outputs Source/Sink 24 mA

Logic Symbol



Pin Assignment



(Top View)

Pin Names

S_0, S_1	Mode Select Inputs
C/SI	Status Priority or Serial Data Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{SE}$	Status Enable Input (Active LOW)
M	Compare Mode Select Input
I/O_0-I/O_7	Parallel Data Inputs or 3-State Parallel Data Outputs
C/SO	Status Priority or Serial Data Output
LT	Register Less Than Bus Output
EQ	Register Equal Bus Output
GT	Register Greater Than Bus Output

Status Truth Table (Hold Mode)

Inputs			Outputs			
$\overline{SE}$	C/SI	Data Comparison	EQ	GT	LT	C/SO
H	X	X	H	H	H	I
L	L	O_A-O_H > I/O_0-I/O_7	L	H	H	L
L	L	O_A-O_H = I/O_0-I/O_7	H	H	H	L
L	L	O_A-O_H < I/O_0-I/O_7	L	H	H	L
L	H	O_A-O_H > I/O_0-I/O_7	L	H	L	L
L	H	O_A-O_H = I/O_0-I/O_7	H	L	L	H
L	H	O_A-O_H < I/O_0-I/O_7	L	L	H	L

I = HIGH if data are equal, otherwise LOW
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Fusctional Description

The AC524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus I/O_0-I/O_7, Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occur on the rising edge of the input clock (CP). The operation of the shift register is controlled by two signals S_0 and S_1 according to the Select Truth Table. The 3-state parallel output buffers are enabled only in the Read mode.

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF, opencollector outputs indicate whether the contents held in the shift register are 'greater than', (GT), 'less than' (LT), or 'equal to' (EQ) the data on the input bus. A HIGH signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A mode control input (M) allows selection between a straightforward magnitude compare or a comparison between twos complement numbers.

For 'greater than' or 'less than' detection, the C/SI input must be held HIGH, as indicated in the Status Truth Table The internal logic is arranged such that a LOW signal on the C/SI input disables the 'greater than' and 'less than' outputs. The C/SO output will be forced HIGH if the 'equal to' status condition exists. otherwise C/SO will be held LOW. These facilities enable the AC524 to be cascaded for word length greater than eight bits.

Select Truth Table

S_0	S_1	Operation
L	L	Hold – Retains data in shift register
L	H	Read – Read contents in register onto data bus
H	L	Shift – Allows serial shifting on next rising clock edge
H	H	Load – Load data on bus into register

Word length expansion (in groups of eight bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see Figure a). The C/SI input of the most significant device is held HIGH while the $\overline{SE}$ input of the least significant device is held LOW. The corresponding status outputs are AND-wired together. In the case of twos complement number compare, only the Mode input to the most significant device should be HIGH. The Mode inputs to all other cascaded devices are held LOW.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, the EQ and LT outputs will be pulled LOW and the GT output will float HIGH . Also the C/SO output of the most significant device will be forced LOW, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go LOW and LT output floats HIGH.

If an equality condition is detected in the most significant device, its C/SO output is forced HIGH. This enables the next less significant device and also disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving 'n' cascaded AC524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take $35+6(n-2)$ ns.

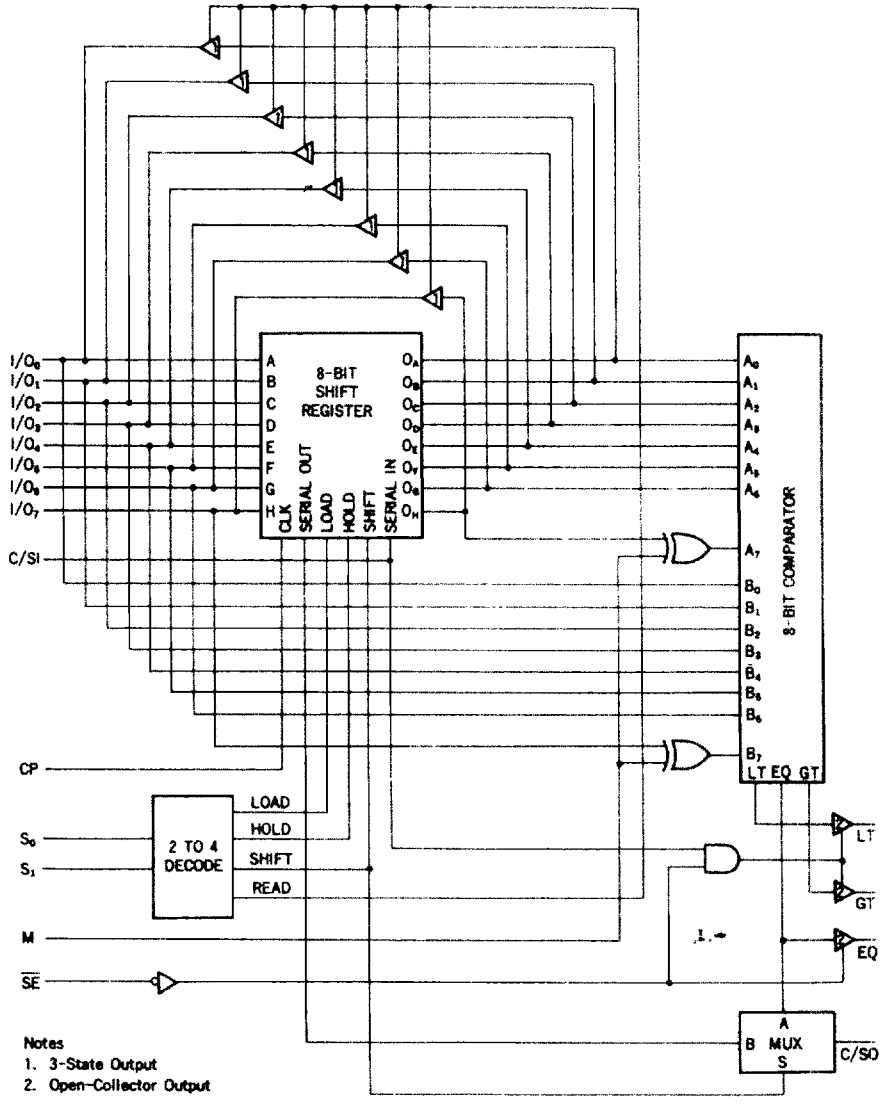
Number Representation Select Table

M	Operation
L	Magnitude compare
H	Twos complement compare

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5V$, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5V$, Ta = 25℃

Block Diagram



AC Characteristics : HD74AC524

Symbol	Parameter	Vcc* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay IO_n to EQ	3.3	1.0		24.5	1.0	28.0	ns
		5.0	1.0		17.5	1.0	20.0	
t_{PHL}	Propagation Delay IO_n to EQ	3.3	1.0		24.5	1.0	28.0	ns
		5.0	1.0		17.5	1.0	20.0	
t_{PLH}	Propagation Delay IO_n to GT or LT	3.3	1.0		28.0	1.0	32.0	ns
		5.0	1.0		20.0	1.0	23.0	
t_{PHL}	Propagation Delay IO_n to GT LT	3.3	1.0		28.0	1.0	32.0	ns
		5.0	1.0		20.0	1.0	23.0	
t_{PLH}	Propagation Delay IO_n to C/SO	3.3	1.0		26.5	1.0	31.0	ns
		5.0	1.0		19.0	1.0	22.0	
t_{PHL}	Propagation Delay IO_n to C/SO	3.3	1.0		26.5	1.0	31.0	ns
		5.0	1.0		19.0	1.0	22.0	
t_{PLH}	Propagation Delay SP to EQ	3.3	1.0		31.5	1.0	36.5	ns
		5.0	1.0		22.5	1.0	26.0	
t_{PHL}	Propagation Delay CP to EQ	3.3	1.0		31.5	1.0	36.5	ns
		5.0	1.0		22.5	1.0	26.0	
t_{PLH}	Propagation Delay CP to ET or GT	3.3	1.0		35.0	1.0	40.5	ns
		5.0	1.0		25.0	1.0	29.0	
t_{PHL}	Propagation Delay CP to LT or CF	3.3	1.0		35.0	1.0	40.5	ns
		5.0	1.0		25.0	1.0	29.0	
t_{PLH}	Propagation Delay CP to C/SO (Compare)	3.3	1.0		35.0	1.0	40.5	ns
		5.0	1.0		25.0	1.0	29.0	
t_{PHL}	Propagation Delay CP to C/SO (shift)	3.3	1.0		35.0	1.0	40.5	ns
		5.0	1.0		25.0	1.0	29.0	
t_{PLH}	Propagation Delay CP to C/SO (shift)	3.3	1.0		19.0	1.0	21.5	ns
		5.0	1.0		13.5	1.0	15.5	
t_{PHL}	Propagation Delay CP to C/SO (shift)	3.3	1.0		19.0	1.0	21.5	ns
		5.0	1.0		13.5	1.0	15.5	
t_{PLH}	Propagation Delay C/S to GT or LT	3.3	1.0		15.5	1.0	17.5	ns
		5.0	1.0		11.0	1.0	12.5	
t_{PHL}	Propagation Delay C/S to GT or LT	3.3	1.0		15.5	1.0	17.5	ns
		5.0	1.0		11.0	1.0	12.5	
t_{PLH}	Propagation Delay Sn to EQ	3.3	1.0		36.5	1.0	42.0	ns
		5.0	1.0		26.0	1.0	30.0	
t_{PHL}	Propagation Delay Sn to EQ	3.3	1.0		36.5	1.0	42.0	ns
		5.0	1.0		26.0	1.0	30.0	
t_{PLH}	Propagation Delay Sn to GT or LT	3.3	1.0		41.5	1.0	47.5	ns
		5.0	1.0		29.5	1.0	34.0	
t_{PHL}	Propagation Delay Ss to GT or LT	3.3	1.0		41.5	1.0	47.5	ns
		5.0	1.0		29.5	1.0	34.0	
t_{PLH}	Propagation Delay Sn to C/SO	3.3	1.0		14.5	1.0	17.0	ns
		5.0	1.0		10.5	1.0	12.0	
t_{PHL}	Propagation Delay Sn to C/SO	3.3	1.0		14.5	1.0	17.0	ns
		5.0	1.0		10.5	1.0	12.0	
t_{PLH}	Propagation Delay SE to EQ	3.3	1.0		12.5	1.0	14.5	ns
		5.0	1.0		9.0	1.0	10.5	
t_{PHL}	Propagation Delay SE to EQ	3.3	1.0		12.5	1.0	14.5	ns
		5.0	1.0		9.0	1.0	10.5	

AC Characteristics: HD74AC524(Cont.)

Symbol	Parameter	Vcc* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay SE to GT or LT	3.3 5.0	1.0 1.0		17.0 12.0	1.0 1.0	19.5 14.0	ns
t_{PHL}	Propagation Delay SE to GT or LT	3.3 5.0	1.0 1.0		17.0 12.0	1.0 1.0	19.5 14.0	ns
t_{PLH}	Propagation Delay C/Si to C/So	3.3 5.0	1.0 1.0		22.5 16.0	1.0 1.0	26.0 18.5	ns
t_{PHL}	Propagation Delay C/Si to C/So	3.3 5.0	1.0 1.0		22.5 16.0	1.0 1.0	26.0 18.5	ns
t_{PLH}	Propagation Delay M to GT or LT	3.3 5.0	1.0 1.0		31.0 22.0	1.0 1.0	35.5 25.5	ns
t_{ZH}	Enable Time M to GT or LT	3.3 5.0	1.0 1.0		31.0 22.0	1.0 1.0	35.5 25.5	ns
t_{ZH}	Enable Time Sn to On	3.3 5.0	1.0 1.0		18.0 13.0	1.0 1.0	21.0 15.0	ns
t_{ZL}	Enable Time Sn to On	3.3 5.0	1.0 1.0		15.5 11.0	1.0 1.0	17.5 12.5	ns
t_{HZ}	Enable Time Sn to On	3.3 5.0	1.0 1.0		21.0 15.0	1.0 1.0	24.0 17.0	ns
t_{LZ}	Enable Time Sn to On	3.3 5.0	1.0 1.0		15.5 11.0	1.0 1.0	17.5 12.5	ns

*Voltage Range 3.3 is 3.3V±0.3V
Voltage Range 5.0 is 5.0V±5.0V

AC Operating Requirements : HD74AC524

Symbol	Parameter	Vcc* (V)	Ta = +25°C, C_L = 50pF		Ta = −40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Setup Time, HIGH or LOW I/On to CP	3.3 5.0		5.0 4.0	6.0 4.5	ns
t_h	Hold Time, HIGH or LOW I/On to CP	3.3 5.0		2.5 2.0	3.0 2.0	ns
t_{su}	Setup Time, HIGH or LOW Sn to CP	3.3 5.0		5.0 4.0	6.0 4.5	ns
t_h	Hold Time, HIGH or LOW Sn to CP	3.3 5.0		0.0 0.0	0.0 0.0	ns
t_{su}	Setup time, HIGH or LOW C/Si to CP	3.3 5.0		5.0 4.0	6.0 4.5	ns
t_h	Hold Time, HIGH or LOW C/Si to CP	3.3 5.0		0.0 0.0	0.0 0.0	ns
t_w	Pulse width	3.3 5.0		5.5 4.5	7.0 5.0	ns

*Voltage Range 3.3 is 3.3V±0.3V
Voltage Range 5.0 is 5.0V±0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC}=5.5V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	V_{CC}=5.0V
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC}=5.0V