élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL5181C, EL5281C, EL5283C, EL5481C, EL5482C Preliminary

8nS High-Speed Comparator Fafmily

Features

- 8ns Typ. Propagation delay
- Low Power Consumption of <25mW/ comparator (at +5V)
- 5V to 12V input supply
- +2.7V to +5V output supply
- True To Ground Input
- Rail to rail outputs
- Active low latch
- Pin compatible 4nS family available (EL5185 family)

Applications

- Threshold Detection
- High Speed Sampling Circuits
- High speed Triggers
- Line Receivers
- PWM Circuits
- High SpeedV/F Converters

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL5181CN	-40°C to +85°C	8-Pin DIP	MDP0031
EL5181CS	-40°C to +85°C	8-Pin SOIC	MDP0027
EL5283CY	-40°C to +85°C	10-Pin MSOP	MDP0043
EL5281CS	-40°C to +85°C	14-Pin SOIC	MDP0027
EL5481CS	-40°C to +85°C	16-Pin SOIC	MDP0027
EL5482CM	-40°C to +85°C	20-Pin SOL	MDP0027
EL5482CU	-40°C to +85°C	24-Pin QSOP	MDP0040

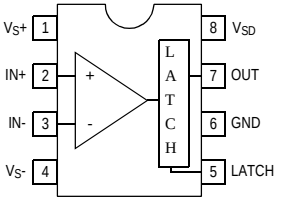
General Description

The EL5181C family of comparators are designed for operation in single supply and dual supply applications with 5V to 12V between V_S+ and V_S-. For single supplies, the inputs can operate from 0.1V below ground for use in ground sensing applications.

The output side of the comparator can be supplied from a single supply of 2.7V to 5V. The outputs swing is to each rail to allow direct connection to CMOS and TTL logic circuits.

These comparators exhibit very short delay times of typically 8ns with power a dissipation of less than 25mW per comparator.

The EL5181C, EL5283C, EL5281C and EL5481C also have latch inputs, holding the comparator output value when a low logic level is applied to the pin. The EL5482C has no latches. The EL5283C is a window comparator, with a single input pin and two range inputs. When the input is beyond the range, the output flags an out of bounds condition.



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Absolute Maximum Ratings (T_A = 25 °C)

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Analog Supply Voltage (V_S+ to V_S-)	+12V
Digital Supply Voltage (V_{SD} to GND)	+7V
Differential Input Voltage	[(V_S-) -0.2V] to [(V_S+) +0.2V]
Common-Mode Input Voltage	[(V_S-) -0.2V] to [(V_S+) +0.2V]
Latch Input Voltage	-0.2V to [V_{SD}+0.2V]
Storage Temperature Range	-65°C to +150°C
Ambient operating Temperature	-40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	TBDmW
ESD Voltage	2kV

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Electrical Characteristics

V_S = ±5V, V_{SD} = 5V, R_L = 2.3kΩ, C_L = 15pF, T_A = 25°C, unless otherwise specified.

Parameter	Description	Condition	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	V_{CM}=0V, V_O=2.5V		0.5	2.0	mV
I_B	Input Bias Current			5	10	µA
C_{IN}	Input Capacitance			5		pF
I_{OS}	Input Offset Current	V_{CM}=0V, V_O=2.5V		50	250	nA
V_{CM}	Input Voltage Range		(V_S-) - 0.1		(V_S+) -2V	V
A_{VO}	Large Signal Voltage Gain			5000		V/V
CMRR	Common-Mode Rejection Ratio	-5V<V_{CM}<+2.75V, V_O=1.4V	.	80		dB
PSRR	Power Supply Rejection Ratio			80		dB
V_{OH}	Output High Voltage	V_{IN}>250mV	V_{SD} - 0.5V	V_{SD} - 0.4V		V
V_{OL}	Output Low Voltage	V_{IN}>250mV		GND + 0.4V	GND + 0.5V	V
V_{LH}	Latch Input Voltage High				2.0	V
V_{LL}	Latch Input Voltage Low		0.8			V
I_{LH}	Latch Input Current High	V_{LH}=3.0V		1	20	µA
I_{LL}	Latch Input Current Low	V_{LL}=0.3V		5	20	µA
I_S+	Positive Analog Supply Current	(per comparator)		3		mA
I_S-	Negative Analog Supply Current	(per comparator)		2.5		mA
I_{DD}	Digital Supply Current	(per comparator)		2		mA
t_{pd}+	Positive Going Delay Time	V_{OD}=5mV, C_L=15pF, I_O=2mA		8	10	nS
t_{pd}-	Negative Going Delay Time	V_{OD}=5mV, C_L=15pF, I_O=2mA		8	10	nS
t_d+	Latch Disable to High Delay			10		nS
t_d-	Latch Disable to Low Delay			12		nS
t_s	Minimum setup time			2		nS
t_h	Minimum hold time			1		nS
t_{pw}(D)	Minimum Latch Disable Pulse Width			10		nS