AMCC®

SONET/SDH/ATM OC-12 TRANSCEIVER W/CDR S3032

FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLLs for clock generation and clock recovery
- Supports 155.52 MHz (OC-3) and 622.08 Mbit/s (OC-12)
- Selectable reference frequencies of 19.44, 38.88, 51.84 or 77.76 MHz
- Interface to both LVPECL and TTL logic
- 8-bit TTL datapath
- Compact 10mm 64 PQFP package
- Diagnostic loopback mode
- Lock detect
- Low jitter LVPECL interface
- Single 3.3V supply

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add drop multiplexors
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3032 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET OC-12 (622.08 Mbit/s) and OC-3 (155.52 Mbit/s) interface device. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3032 transceiver chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the device by synchronizing its on-chip VCO directly to the incoming data stream. The S3032 also performs SONET/SDH frame detection. The chip can be used with a 19.44, 38.88, 51.84 or 77.76 MHz reference clocks, in support of existing system clocking schemes.

The low jitter LVPECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3032 is packaged in a 10mm 64 PQFP, offering designers a small package outline.

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Figure 1. System Block Diagram

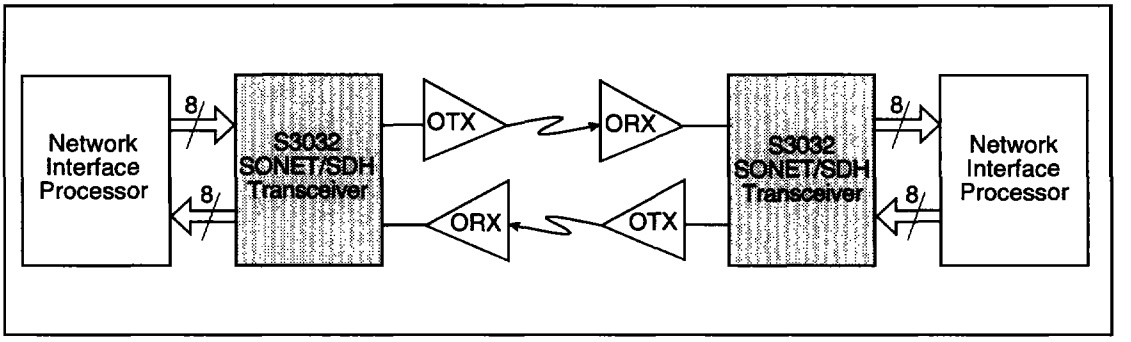
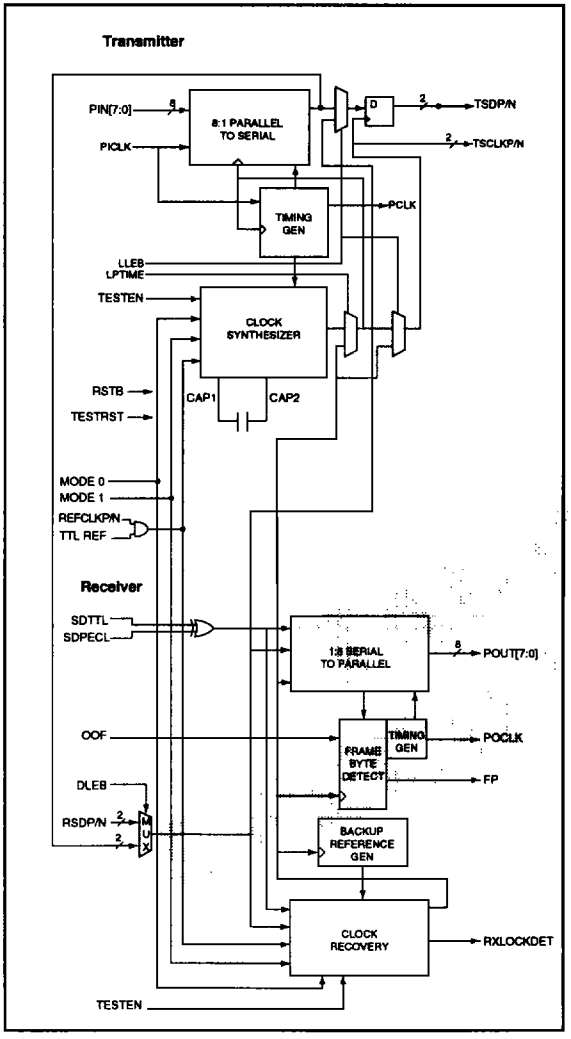


Figure 2. S3032 Transceiver Functional Block Diagram



S3032 OVERVIEW

The S3032 transceiver implements SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. The block diagram in Figure 2 shows basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing. The system timing circuitry consists of management of the datastream, framing, and clock distribution throughout the front end.

The S3032 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

1. Clock and data recovery from serial input
2. Frame detection
3. Serial-to-parallel conversion
4. 8-bit parallel output

Internal clocking and control functions are transparent to the user.

A lock detect feature is provided on the S3032, which indicates that the PLL is locked (synchronized) to the incoming data stream, and facilitates continuous down-stream clocking in the absence of data.

Suggested Interface Devices

PMC PM5312	STTX	SONET/SDH Tranport Term. Transceiver
PMC PM5355	SUNI-622	Satum User Network Interface

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