NEW PRODUCT

HB56G136CC Series

1,048,576-Word × 36-Bit High Density Dynamic RAM Card

HITACHI

Rev.0
Jul. 03, 1992

Description

The HB56G136CC is a 1M × 36 dynamic RAM Card, mounted 8 pieces of 4Mbit DRAM (HM514900LTT) sealed in TSOP package.

An outline of the HB56G136CC is 88-pin two piece connector package.

Therefore, the HB56G136CC makes high density and it is possible to expand easily for memory system.

The HB56G136CC provides common data inputs and outputs.

Decoupling capacitors are mounted each memory.

■ Feature

- 88-pin two piece connector package
  - Lead pitch 1.0mm
- Single 5V (± 5%) supply
- High speed
  - t_{RAC} .... 70ns/80ns (max.)
  - t_{CAC} .... 27ns (max.)
- Low power dissipation
  - Active mode .... 2.47W/2.26W (max.)
  - Standby mode .... 90.0mW (max.)
- Fast page mode capability
- 1,024refresh cycle / 128ms (Distributed Refresh)
- 2 variations of refresh
  - /RAS only refresh
  - /CAS before /RAS refresh
- CMOS interface

■ Ordering information

Part No.	Access time	Package
HB56G136CC-7L	70ns	88-pin 2 piece connector type
HB56G136CC-8L	80ns	

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice

■ Pin Assignment

Pin Name	Pin No.	Pin No	Pin Name
GND	1	45	GND
DQ0	2	46	DQ18
DQ1	3	47	DQ19
DQ2	4	48	DQ20
DQ3	5	49	DQ21
DQ4	6	50	DQ22
DQ5	7	51	DQ23
DQ6	8	52	DQ24
Vcc(5V)	9	53	DQ25
DQ7	10	54	DQ26
NC	11	55	NC
DQ8	12	56	GND
A0	13	57	A1
A2	14	58	A3
Vcc(5V)	15	59	A5
A4	16	60	A7
NC	17	61	A9
A6	18	62	NC
A8	19	63	GND
NC	20	64	NC
NC	21	65	/RAS1
/RAS0	22	66	/CAS2
/CAS0	23	67	GND
/CAS1	24	68	/CAS3
NC	25	69	/RAS3
/RAS2	26	70	/WE
Vcc(5V)	27	71	PD1
PD2	28	72	PD3
PD4	29	73	GND
PD6	30	74	PD5
NC	31	75	PD7
NC	32	76	PD8
DQ17	33	77	NC
DQ9	34	78	NC
NC	35	79	DQ35
DQ10	36	80	DQ27
Vcc(5V)	37	81	DQ28
DQ11	38	82	DQ29
DQ12	39	83	DQ30
DQ13	40	84	DQ31
DQ14	41	85	DQ32
DQ15	42	86	DQ33
DQ16	43	87	DQ34
GND	44	88	GND

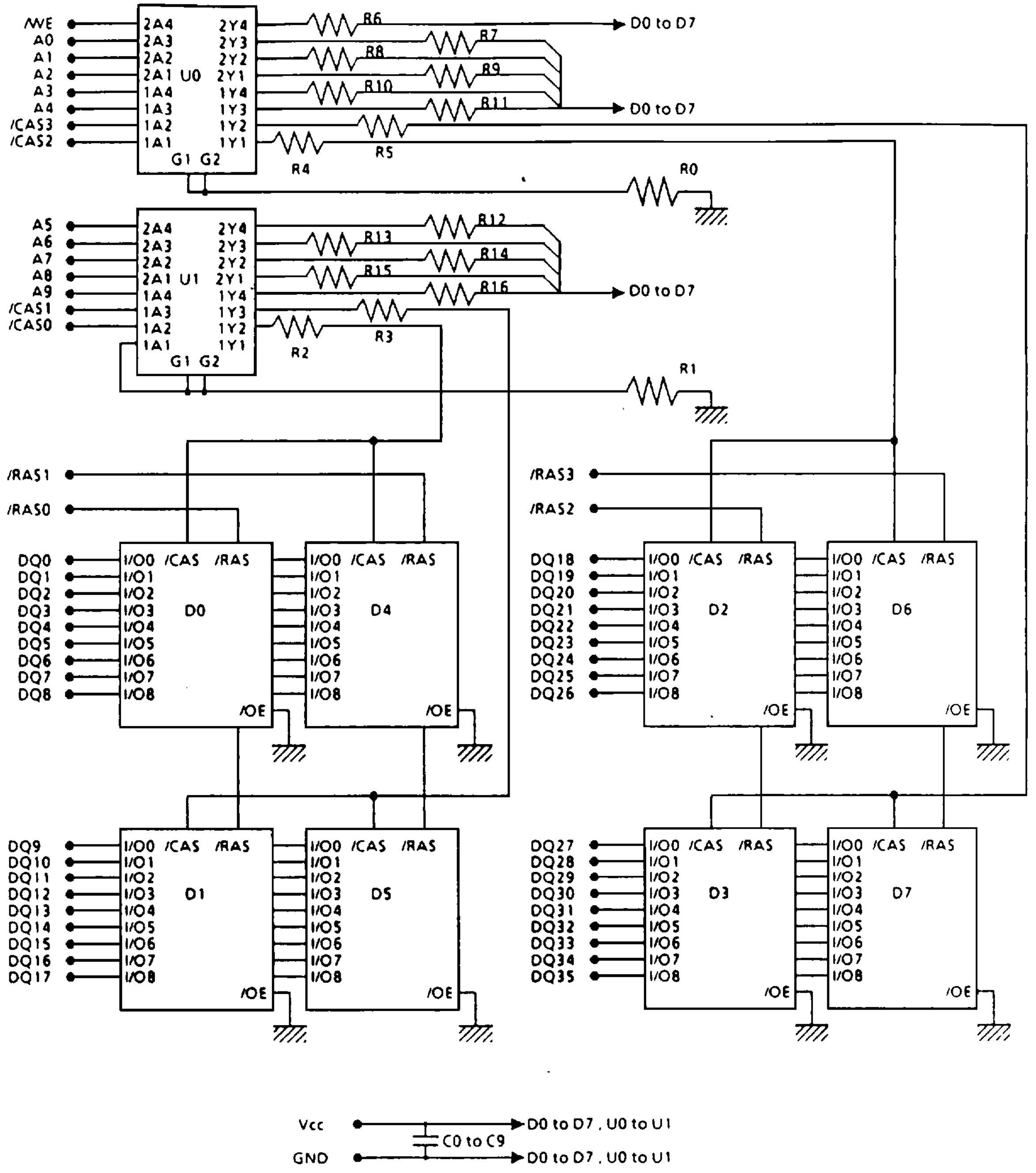
■ Pin Description

Pin Name	Description	
A0 to A9	Address input	
—	Row address	A0 to A9
—	Column address	A0 to A8
—	Refresh address	A0 to A9
/WE	Write enable	
/RAS0 to /RAS3	Row address strobe	
/CAS0 to /CAS3	Column address strobe	
DQ0 to DQ35	Data input/output	
PD1 to PD8	Presence detect pins	
Vcc	Power supply	
GND	Ground	

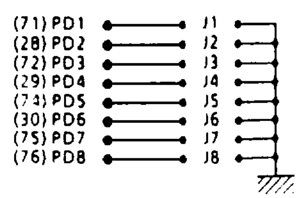
■ Presence Detect Pinout

Pin Name	Pin No.	HB56G136CC	
		-7L	-8L
PD1	71	NC	NC
PD2	28	Vss	Vss
PD3	72	Vss	Vss
PD4	29	Vss	Vss
PD5	74	Vss	Vss
PD6	30	Vss	NC
PD7	75	NC	Vss
PD8	76	NC	NC

Block Diagram

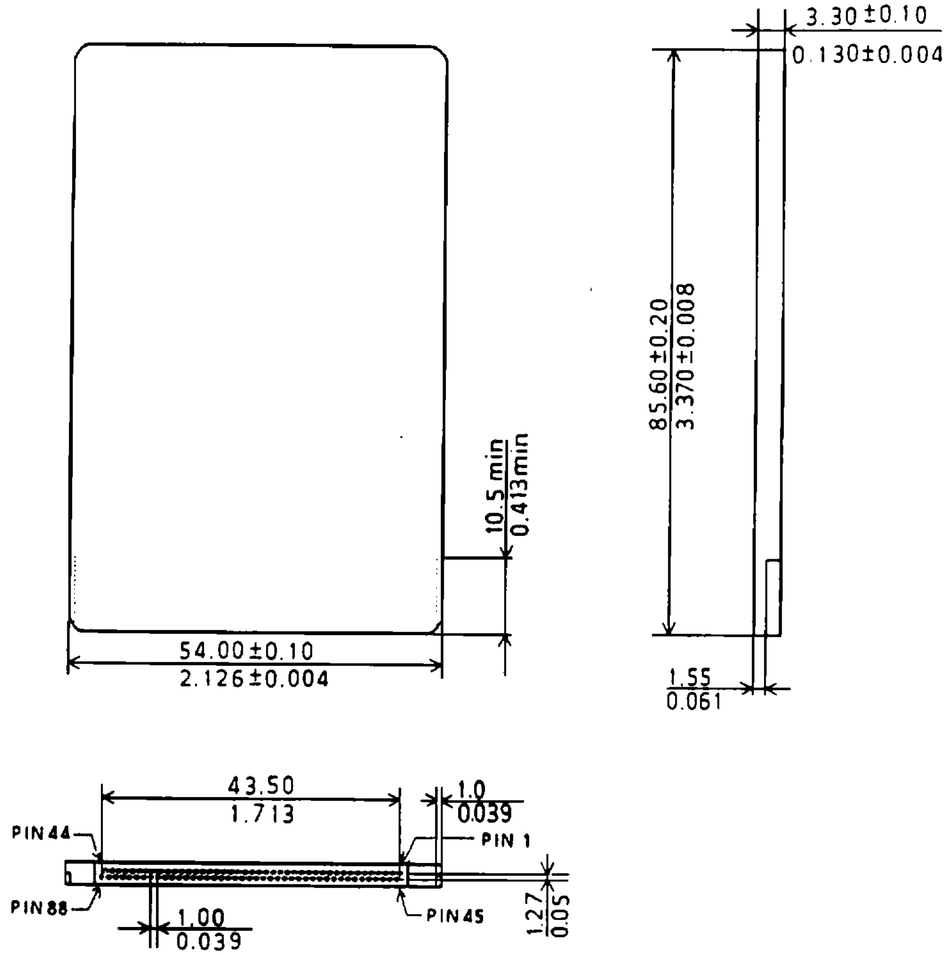


Note : D0 to D7 : HM514900LTT
U0 to U1 : SN74AC11244PW
C0 to C9 : Chip Capacitor
R0 to R16 : Chip Resistor



■ Physical Outline

Unit : $\frac{mm}{inch}$



■ Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	V_{IN}	– 1.0 to + 7.0	V
	(Output)	V_{OUT}	– 1.0 to + 7.0	V
Supply voltage relative to V_{SS}		V_{CC}	– 1.0 to + 7.0	V
Short circuit output current		I_{out}	50	mA
Power dissipation		P_T	4	W
Operating temperature		T_{opr}	0 to + 50	°C
Storage temperature		T_{stg}	– 40 to + 85	°C

■ Electrical Characteristics

☆ Recommended DC Operating Conditions ($T_a = 0$ to $+50°C$)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	/RAS , DQ	V_{IH}	2.4	—	6.25	V	1
	Others pin		3.7	—	5.75		
Input low voltage	/RAS , DQ	V_{IL}	– 1.0	—	0.8	V	1
	Others pin		– 0.5	—	1.4		

Note : 1. All voltage referenced to V_{SS}

☆ DC Electrical Characteristics (Ta = 0 to + 50°C, V_{CC} = 5V ± 5%, V_{SS} = 0V) 4)

Parameter	Symbol	HB56G136CC -7L Min.	HB56G136CC -7L Max.	HB56G136CC -8L Min.	HB56G136CC -8L Max.	Unit	Test Condition	Note
Operating current	I_{CC1}	–	470	–	430	mA	t_{RC} = min.	1,2
Standby current	I_{CC2}	–	17	–	17	mA	TTL interface /RAS = V_{IH} /CAS ≧ V_{CC} – 0.2V D_{OUT} = High-Z	
		–	2	–	2	mA	CMOS interface /RAS,/CAS ≧ V_{CC} – 0.2V D_{OUT} = High-Z	5
/RAS - only refresh current	I_{CC3}	–	470	–	430	mA	t_{RC} = min.	2
Battery backup current	I_{CC4}	–	3	–	3	mA	t_{RC} ≦ 125μA t_{RAS} ≦ 1μA /WE,Adress,Din = V_{IH} or V_{IL} D_{OUT} = High-Z	5
Standby current	I_{CC5}	–	42	–	42	mA	/RAS = V_{IH} /CAS = V_{IL} D_{OUT} = enable	1
/CAS before /RAS refresh current	I_{CC6}	–	470	–	430	mA	t_{RC} = min.	
Page mode current	I_{CC7}	–	470	–	430	mA	t_{PC} = min.	1,3
Input leakage current	I_{LI}	–10	10	–10	10	μA	0V ≦ V_{IN} ≦ 7V	
Output leakage current	I_{LO}	–10	10	–10	10	μA	0V ≦ V_{OUT} ≦ 7V D_{OUT} = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{OUT} = –5mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low I_{OUT} = 4.2mA	

Note : 1 . I_{CC} depends on output load condition when the device is selected , I_{CC} max. is specified at the output open condition.

2 . Address can be changed once or less while /RAS = V_{IL}.

3 . Address can be changed once or less while /CAS = V_{IH}.

4 . The supply voltage with all VCC pins must be on the same level.
The supply voltage with all VSS pins must be on the same level.

5. $t_{RAS} = t_{RAS(min)}$ to 1μS
Input voltage : All pins : V_{IH} ≧ V_{CC} – 0.2V or V_{IL} ≦ 0.2V.

☆ Capacitance (Ta = 25°C, V_{CC} = 5V ± 5%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input capacitance (Address)	C_{I1}	–	20	pF	1
Input capacitance (/WE , /CAS)	C_{I2}	–	20	pF	1
Input capacitance (/RAS)	C_{I3}	–	35	pF	1
Output capacitance (DQ0 to DQ35)	$C_{I/O}$	–	35	pF	1,2

Note : 1 . Capacitance measured with Boonton Meter or effective capacitance measuring method.
2 . /CAS = V_{IH} to disable D_{OUT}.

☆ AC Characteristics (Ta = 0 to 50°C, V_{CC} = 5V ± 5%, V_{SS} = 0V) 1), 14)

- Read , Write and Refresh Cycle (Common parameters)

Parameter	Symbol	HB56G136CC -7L Min.	HB56G136CC -7L Max.	HB56G136CC -8L Min.	HB56G136CC -8L Max.	Unit	Note
Ramdom read or write cycle time	t_{RC}	130	–	150	–	ns	
/RAS precharge time	t_{RP}	50	–	60	–	ns	
/RAS pulse width	t_{RAS}	70	10000	80	10000	ns	
/CAS pulse width	t_{CAS}	20	10000	20	10000	ns	
Row address set-up time	t_{ASR}	7	–	7	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	ns	
/RAS to /CAS delay time	t_{RCD}	20	43	20	53	ns	8
/RAS to column address delay time	t_{RAD}	15	28	15	33	ns	9
/RAS hold time	t_{RSH}	27	–	27	–	ns	
/CAS hold time	t_{CSH}	70	–	80	–	ns	
/CAS to /RAS precharge time	t_{CRP}	22	–	22	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	–	128	–	128	ms	15

- Read Cycle

Parameter	Symbol	HB56G136CC -7L Min.	-7L Max.	-8L Min.	-8L Max.	Unit	Note
Access time from /RAS	t_{RAC}	–	70	–	80	ns	2,3
Access time from /CAS	t_{CAC}	–	27	–	27	ns	3,4,13
Access time from address	t_{AA}	–	42	–	47	ns	3,5,13
Read command set-up time	t_{RCS}	7	–	7	–	ns	
Read command hold time to /CAS	t_{RCH}	0	–	0	–	ns	
Read command hold time to /RAS	t_{RRH}	0	–	0	–	ns	
Column address to /RAS lead time	t_{RAL}	42	–	47	–	ns	
Output buffer turn-off time	t_{OFF}	0	22	0	22	ns	6

- Write Cycle

Parameter	Symbol	HB56G136CC -7L Min.	-7L Max.	-8L Min.	-8L Max.	Unit	Note
Write command set-up time	t_{WCS}	0	–	0	–	ns	10
Write command hold time	t_{WCH}	15	–	15	–	ns	
Write command pulse width	t_{WP}	10	–	10	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	11
Data-in hold time	t_{DH}	22	–	22	–	ns	11

- Refresh Cycle

Parameter	Symbol	HB56G136CC -7L Min.	-7L Max.	-8L Min.	-8L Max.	Unit	Note
/CAS set-up time (/CAS before /RAS refresh cycle)	t_{CSR}	17	–	17	–	ns	
/CAS hold time (/CAS before /RAS refresh cycle)	t_{CHR}	10	–	10	–	ns	
/RAS precharge to /CAS hold time	t_{RPC}	10	–	10	–	ns	

- Fast Page Mode Cycle

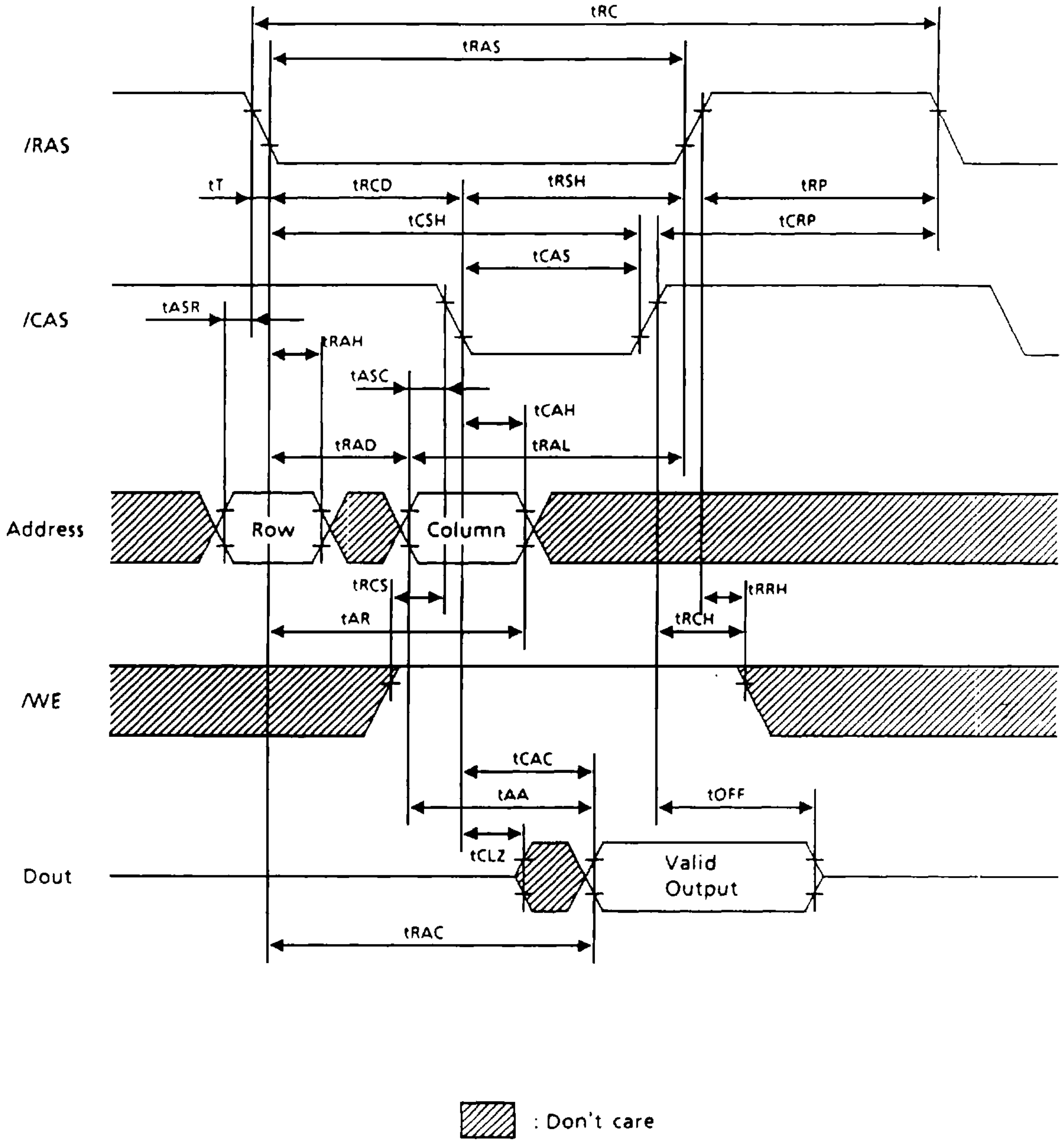
Parameter	Symbol	HB56G136CC -7L Min.	HB56G136CC -7L Max.	HB56G136CC -8L Min.	HB56G136CC -8L Max.	Unit	Note
Fast page mode cycle time	t_{PC}	50	–	55	–	ns	
Fast page mode /CAS precharge time	t_{CP}	15	–	15	–	ns	
Fast page mode /RAS pulse width	t_{RASC}	–	100000	–	100000	ns	12
Access time from /CAS precharge	t_{ACP}	–	47	–	52	ns	3,13
/RAS hold time from /CAS precharge	t_{RHCP}	47	–	52	–	ns	

Notes

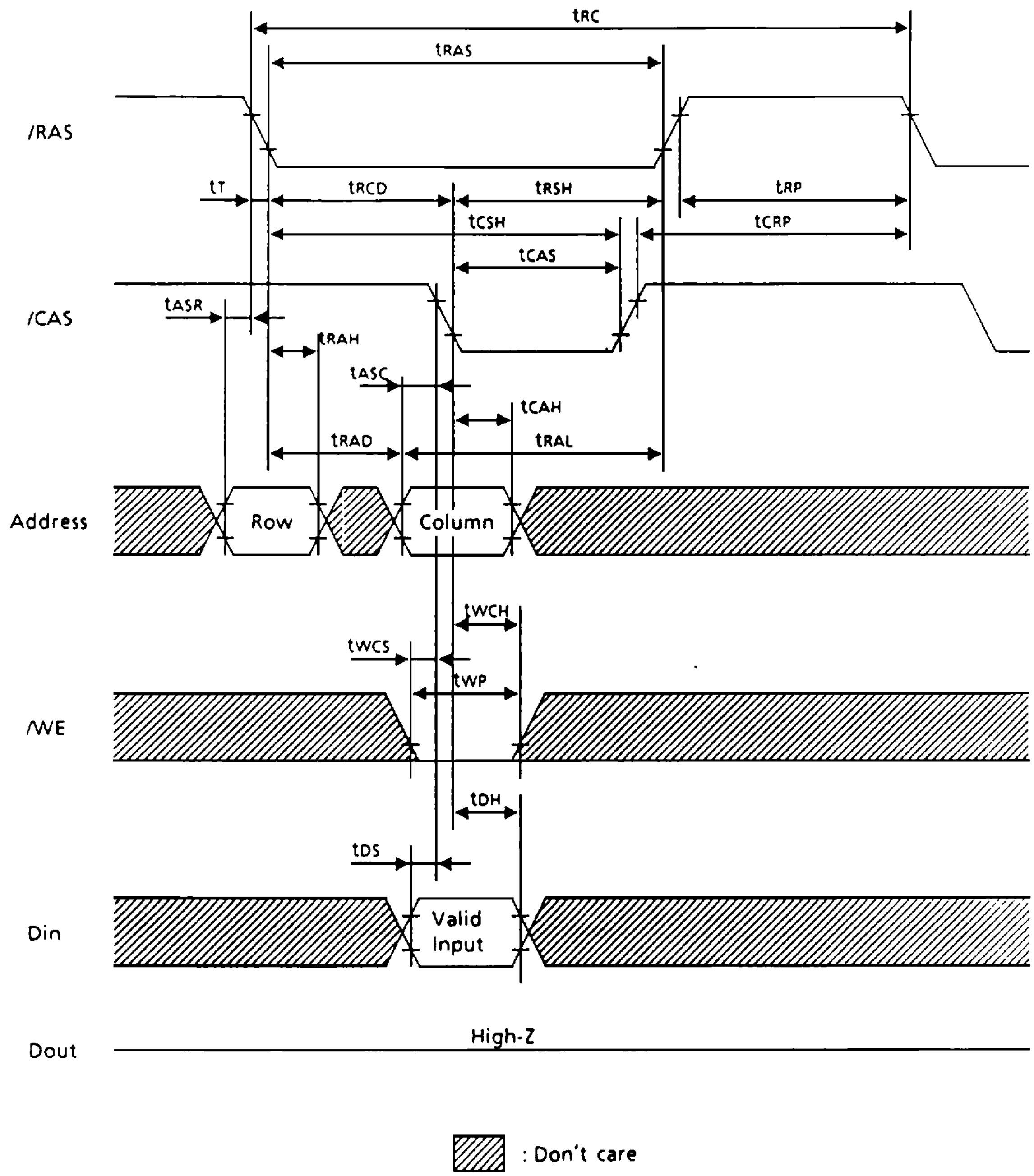
1. AC measurements assume $t_T = 5ns$.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min.))
11. These parameters are referenced to /CAS leading edge in an early write cycle.
12. t_{RASC} defines /RAS pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (/RAS clock such as /RAS-only refresh).
15. t_{REF} defines is 1,024 refresh cycles.

■ Timing waveform

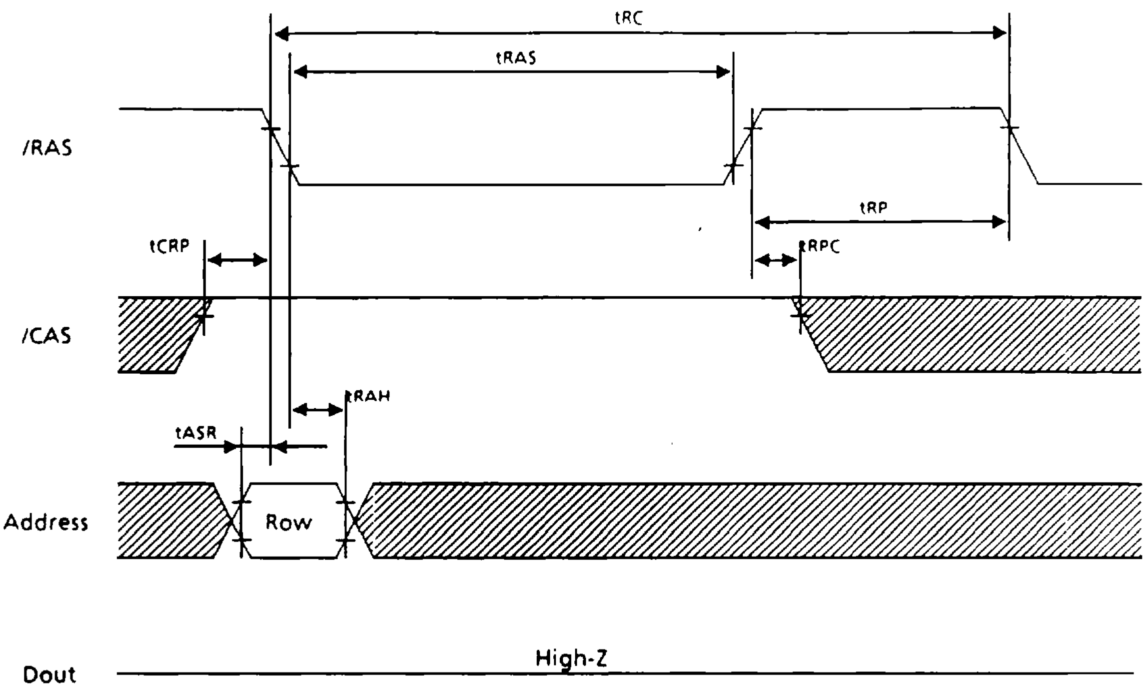
Read cycle



Early Write Cycle

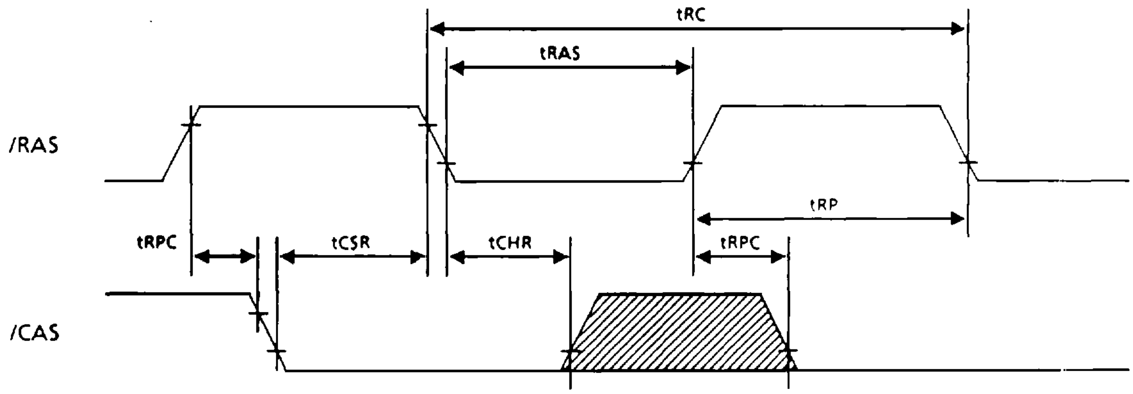


/RAS Only Refresh Cycle



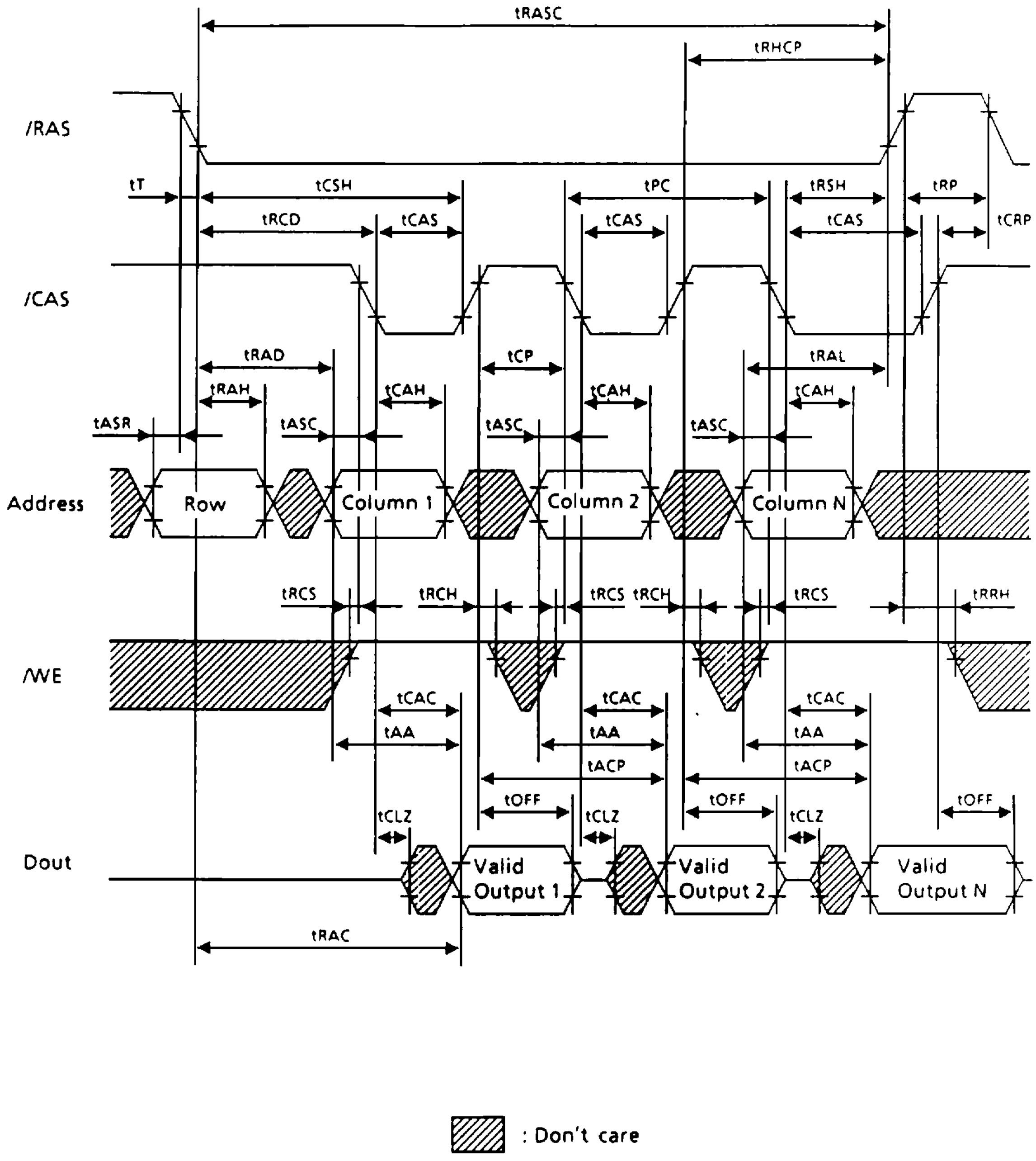
1 /WE : Don't care
2 [hatched] : Don't care

/CAS before /RAS Refresh Cycle

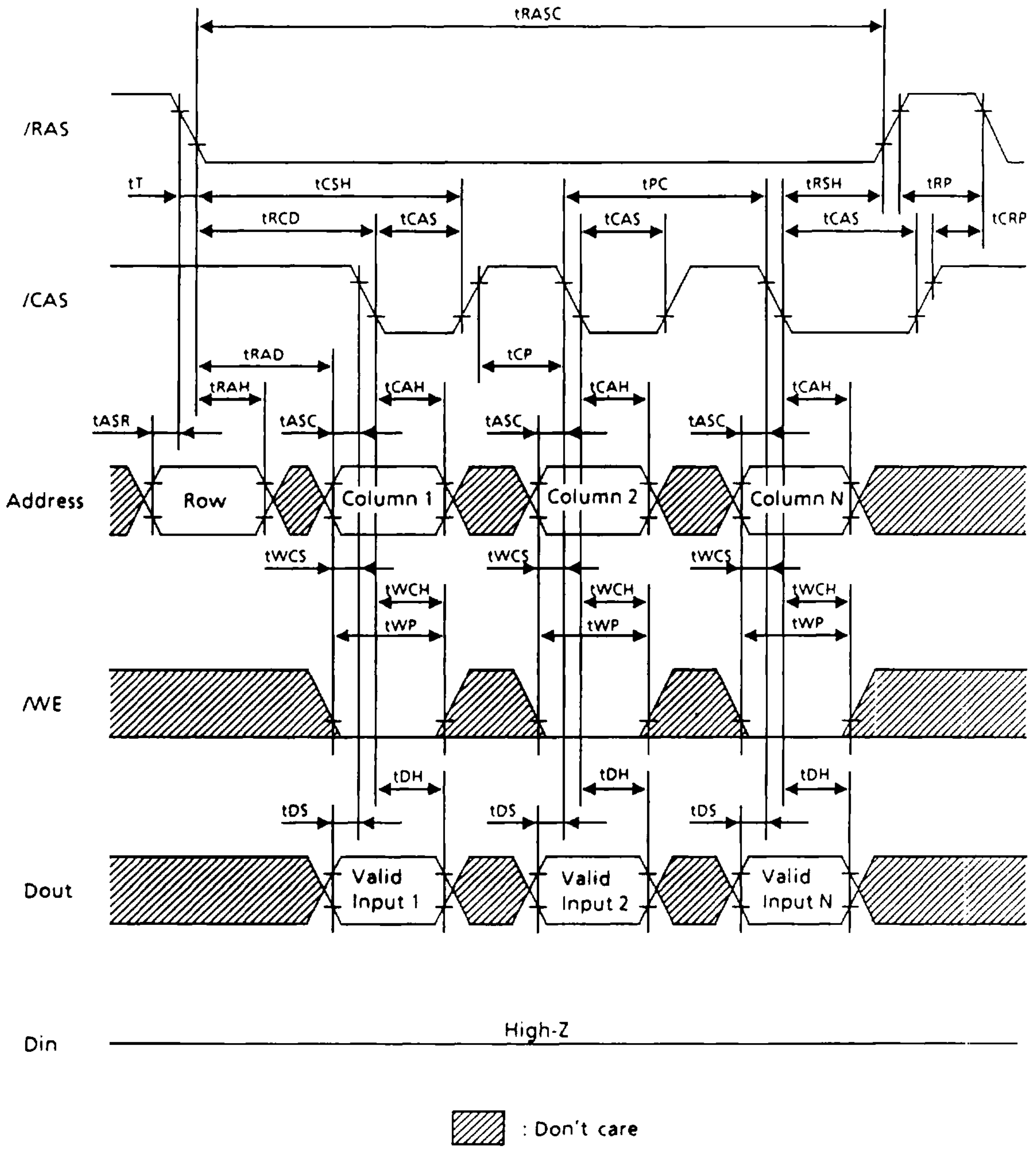


1 Address, Din : Don't care
2 Dout : High-Z
3 [hatched] : Don't care
4 /WE = VIH

Fast Page Mode Read Cycle



Fast Page Mode Early Write Cycle



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■ Revision Record

Rev.	Date	Content of Modification	Drawn by	Approved by
0	Jul. 01. '92	Initial issue	T. Sugano	O. Sakai