MOTOROLA

SN54/74LS682
SN54/74LS684
SN54/74LS688

8-BIT MAGNITUDE COMPARATORS

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS682, 684, 688 are 8-bit magnitude comparators. These device types are designed to perform comparisons between two eight-bit binary or BCD words. All device types provide $\overline{P=Q}$ outputs and the LS682 and LS684 have $\overline{P>Q}$ outputs also.

The LS682, LS684 and LS688 are totem pole devices. The LS682 has a 20 kΩ pullup resistor on the Q inputs for analog or switch data.

TYPE	$\overline{P=Q}$	$\overline{P>Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	PULLUP
LS682	yes	yes	no	totem-pole	yes
LS683	yes	yes	no	open-collector	yes
LS684	yes	yes	no	totem-pole	no
LS685	yes	yes	no	open-collector	no
LS686	yes	yes	yes	totem-pole	no
LS687	yes	yes	yes	open-collector	no
LS688	yes	no	yes	totem-pole	no
LS689	yes	no	yes	open-collector	no

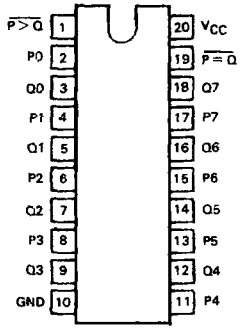
FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES			
P, Q	$\overline{G}$, $\overline{GT}$	$\overline{G2}$	$\overline{P=Q}$	$\overline{P>Q}$
P = Q	L	L	L	H
P > Q	L	L	H	L
P < Q	L	L	H	H
X	H	H	H	H

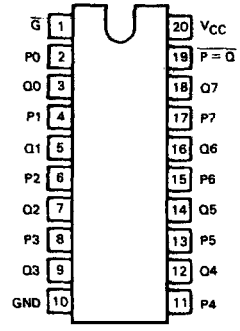
H = high level, L = low level, X = irrelevant

CONNECTION DIAGRAMS
(TOP VIEW)

SN54LS/74LS682/684



SN54LS/74LS688



J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

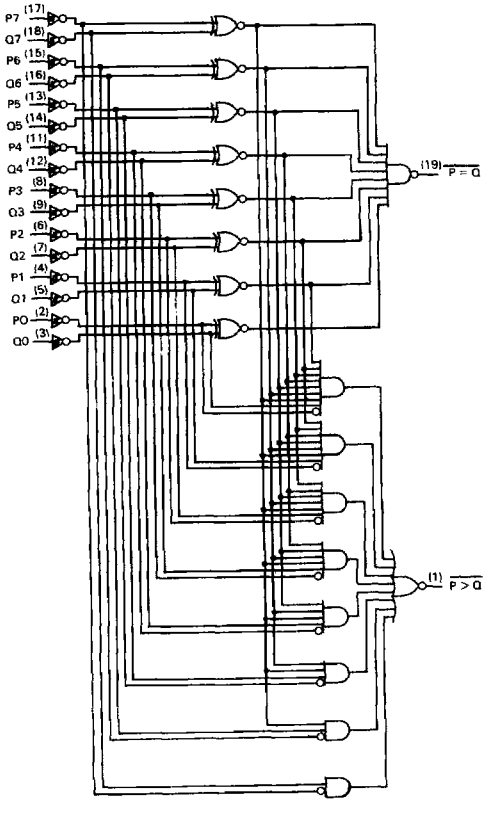
GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

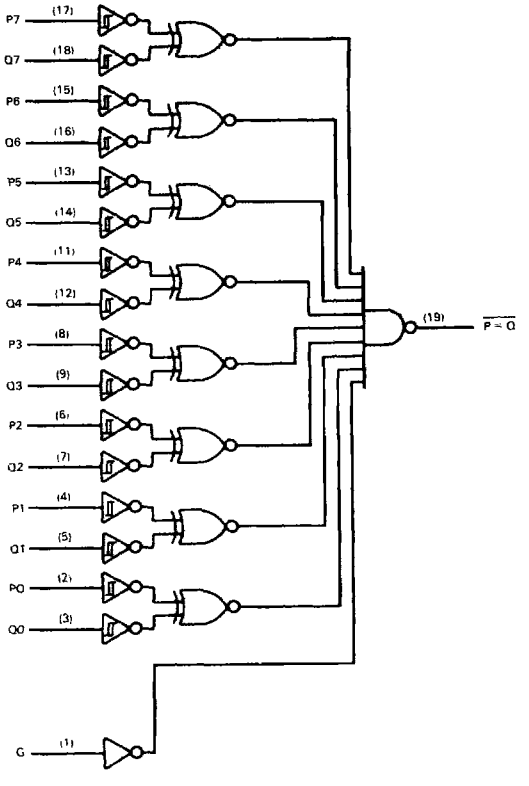
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
		LS682-Q Inputs			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
		Others			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current	LS682-Q Inputs			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
		Others			−0.2	mA	
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX
I_{CC}	Power Supply Current	LS682			70	mA	V_{CC} = MAX
		LS684			65	mA	
		LS688			65	mA	

LOGIC DIAGRAMS



SN54LS/74LS682 thru LS684



SN54LS/74LS688

AC CHARACTERISTICS: $T_A = 25°C$

SN54LS/74LS682

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P = Q}$		13 15	25 25	ns	$V_{CC} = 5.0$ V $C_L = 45$ pF $R_L = 667\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P = Q}$		14 15	25 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P > Q}$		20 15	30 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P > Q}$		21 19	30 30	ns	

SN54LS/74LS684

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P = Q}$		15 17	25 25	ns	$V_{CC} = 5.0$ V $C_L = 45$ pF $R_L = 667\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P = Q}$		16 15	25 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P > Q}$		22 17	30 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P > Q}$		24 20	30 30	ns	

SN54LS/74LS688

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P = Q}$		12 17	18 23	ns	$V_{CC} = 5.0$ V $C_L = 45$ pF $R_L = 667\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P = Q}$		12 17	18 23	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, $\overline{G1}$ to $\overline{P = Q}$		12 13	18 20	ns	