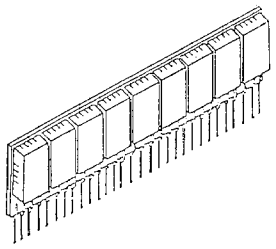
HB561009A-12, HB561009A-15, HB561009A-20

Preliminary
MARCH, 1986

HITACHI

262,144 × 9-bit Dynamic Random Access Memory Module



HB561009A

■ GENERAL DESCRIPTION

The HB561009A is a 2304K dynamic random-access memory module organized as 262,144 × 9-bits [bit nine (PD, PQ) is generally used for parity and is controlled by PCAS] in a 30-pin single-in-line package comprising nine HM50256CP, 262,144 × 1-bit dynamic RAM's in 18-pin Plastic Leaded Chip Carrier mounted on top of a substrate together and eight 0.1μF decoupling capacitors mounted beneath the chip carriers.

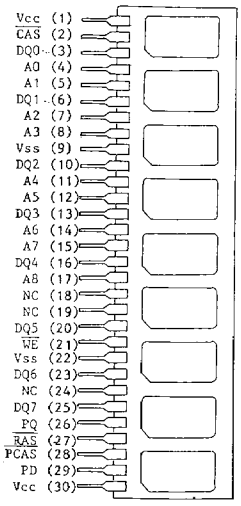
■ FEATURES

- 262,144 words × 9-bits Organization
- Industry standard 30-Pin Single Inline Package Memory Module
- Single 5V (± 10%)
- Utilizes nine 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561009A operates as nine HM50256CP as shown in the functional block diagram (P.2).
- Low Power:
  Operating—2,160 mW TYP. (tRC = 260ns)
  Standby—135 mW TYP.
- High Speed:

	Access Time from $\overline{RAS}$ (MAX)	Access Time from $\overline{CAS}$ (MAX)	Read or Write Cycle (MIN)
HB561009A-12	120ns	70ns	220ns
HB561009A-15	150ns	75ns	260ns
HB561009A-20	200ns	100ns	330ns

- Page Mode Capability
- TTL Compatible
- 256 Refresh Cycles (4ms)
- 3 Variations of Refresh
  $\overline{RAS}$ only Refresh
  $\overline{CAS}$ before $\overline{RAS}$ Refresh
  Hidden Refresh
- Operating Ambient Air, Temperature 0 ~ 70°C
- Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines
- Separate $\overline{CAS}$ control for one separate pair of Data-In and Data-Out lines
- The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout

■ PIN ARRANGEMENT



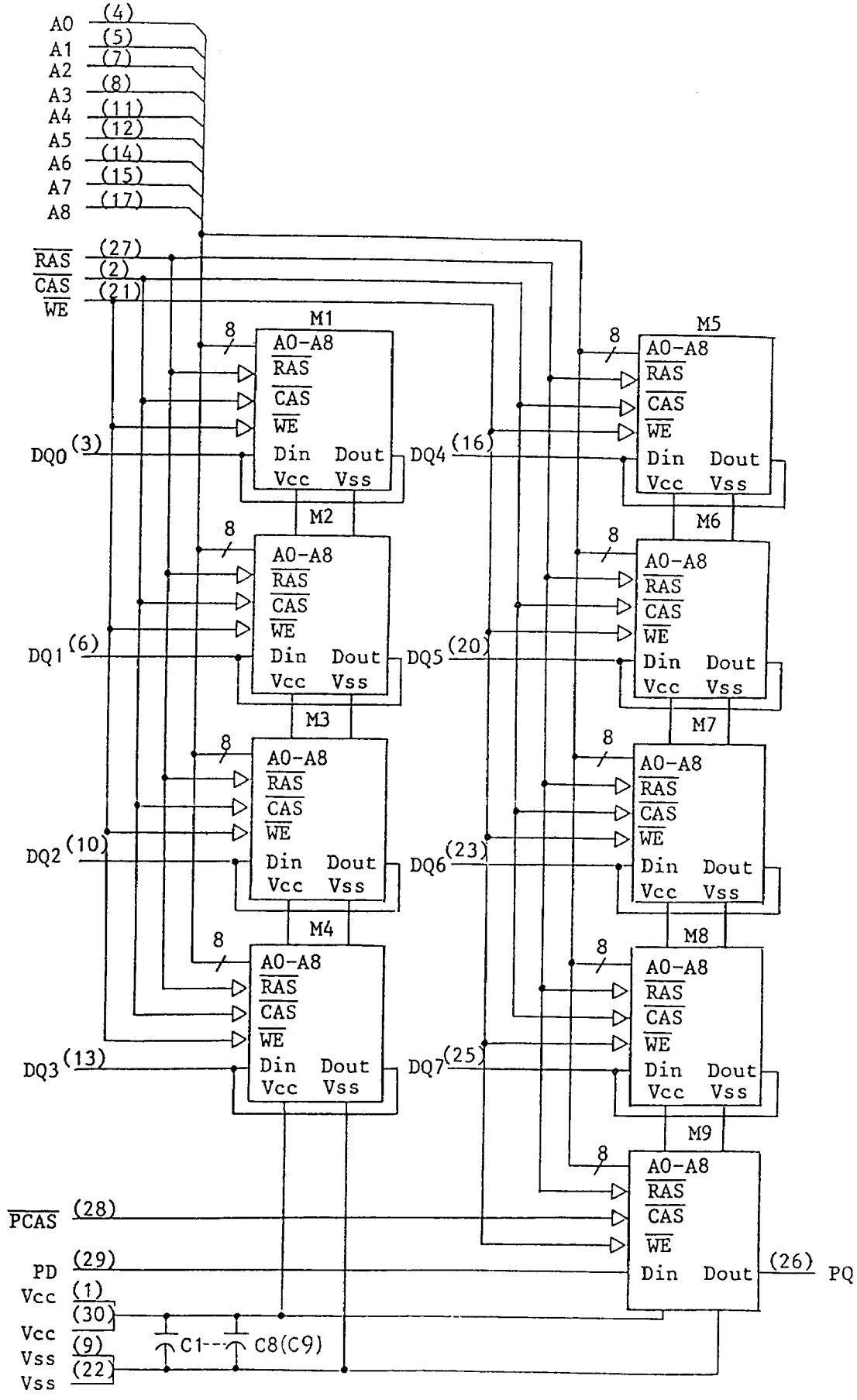
(Top View)

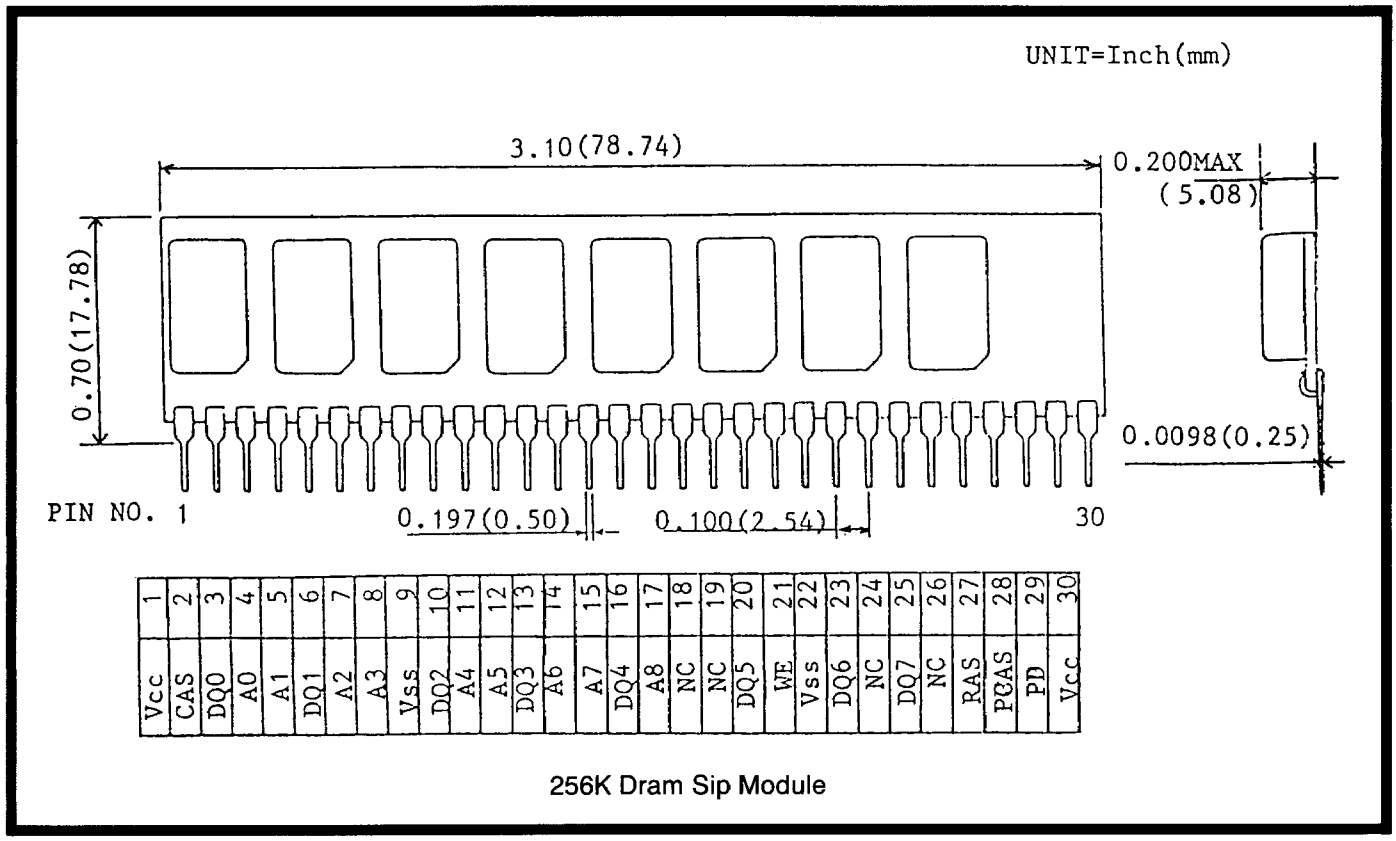
PIN NOMENCLATURE

A_0–A_8	Address Inputs
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobes
DQ0–DQ7	Data In/Data Out
PD	Data In
NC	No Connection
PQ	Data Out
$\overline{RAS}$	Row Address Strobes
V_{CC}	+5V Supply
V_{SS}	Ground
$\overline{WE}$	Write Enable

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ FUNCTIONAL BLOCK DIAGRAM





256K Dram Sip Module

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{ss}	–1V to 7V
Operating Temperature, T_a (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	–55°C to 125°C
Power Dissipation	9W
Short Circuit Output Current	50 mA

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Vcc	Supply voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High voltage	2.4		6.5	V	1
V_{IL}	Input Low voltage	-1.0		0.8	V	1

Notes:
All voltages referenced to V_{ss}

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to 70°C V_{cc} = 5V ± 10%, V_{ss} = 0V)

Symbol	Parameter	Min	Max	Unit	Notes
Icc1	Operating current tRC = 330 ns tRC = 260 ns		 495 630	mA	1
Icc2	Standby current		40	mA	
Icc3	Refresh current tRC = 330 ns tRC = 260 ns		 378 477	mA	$\overline{RAS}$ only Refresh
Icc5	Standby current (Dout Enable)		90	mA	1
Icc6	Refresh current tRC = 330 ns tRC = 260 ns		 405 522	mA	$\overline{CAS}$ before $\overline{RAS}$ Refresh
Ii(L)	Input leakage 0 < Vin < 7V	-10	10	uA	
Io(L)	Output leakage 0 < Vout < 7V	-10	10	uA	Dout is disabled
VOH	Output levels High Iout = -5 mA	2.4	Vcc	V	
VOL	Low Iout = 4.2 mA	0	0.4	V	

■ AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Type	Max	Unit	Notes
CI1	Address		60	pF	2
CI2	Clocks		75	pF	2
CI3	DQ		17	pF	2,3
CI4	PQ		12	pF	2,3
CI5	PD		10	pF	2

Notes:

1. I_{cc} depends on output loading condition when the device is selected, I_{cc} max is specified at the output open condition.
2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
3. $\overline{CAS}$ = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

1), 9), 10) (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

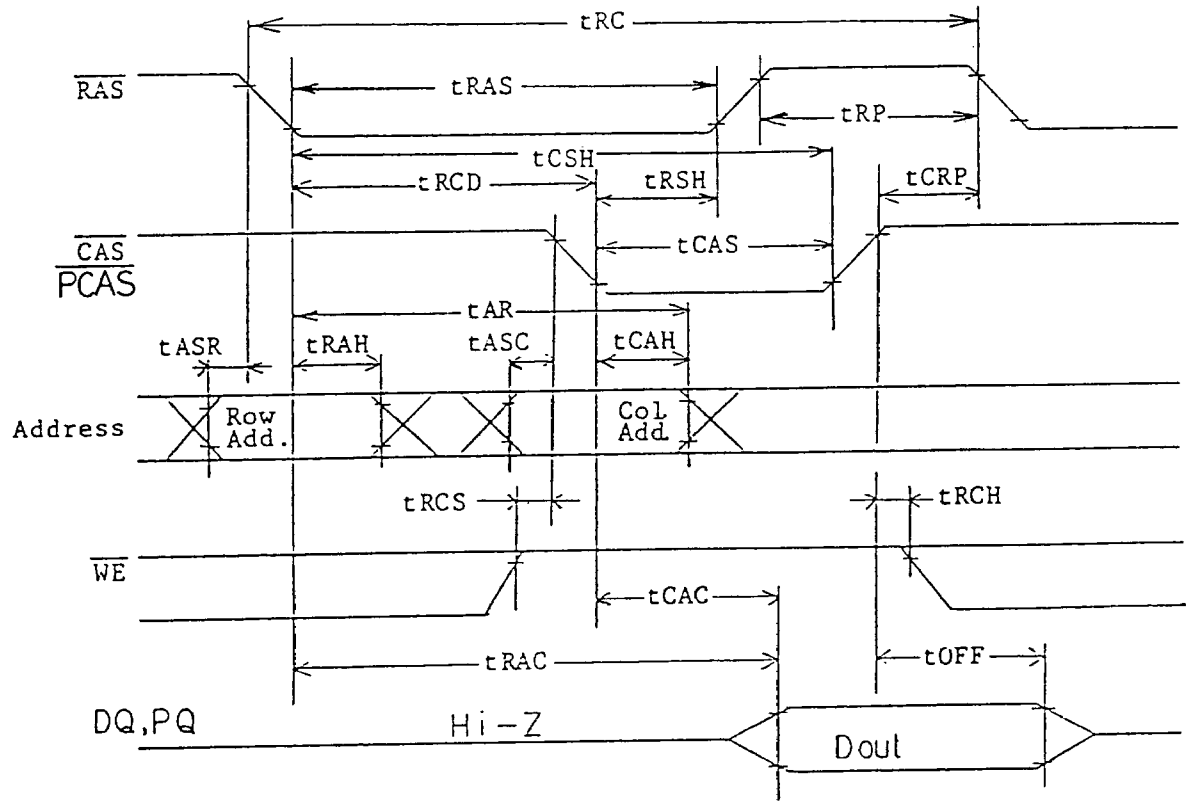
Symbol	HB561009A-12		HB561009A-15		HB561009A-20		Unit	Note
	min	max	min	max	min	max		
tRAC		120		150		200	ns	2,3
tCAC		70		75		100	ns	3,4
tOFF		30		40		50	ns	5
tT	3	50	3	50	3	50	ns	6
tRC	220		260		330		ns	
tRP	90		100		120		ns	
tRAS	120	10000	150	10000	200	10000	ns	
tCAS	70	10000	75	10000	100	10000	ns	
tRCD	35	50	35	75	35	100	ns	7
tRSH	70		75		100		ns	
tCSH	120		150		200		ns	
tCRP	10		10		10		ns	
tASR	0		0		0		ns	
tRAH	15		15		20		ns	
tASC	0		0		0		ns	
tCAH	25		25		30		ns	
tAR	75		100		130		ns	
tWCS	0		0		0		ns	8
tWCH	40		45		55		ns	
tWCR	90		120		155		ns	
tWP	40		45		55		ns	
tRWL	40		45		55		ns	
tCWL	40		45		55		ns	
tDS	0		0		0		ns	8
tDH	40		45		55		ns	8
tDHR	90		120		155		ns	
tRCS	0		0		0		ns	
tRCH	0		0		0		ns	
tRRH	10		10		10		ns	
tREF		4		4		4	ms	
tCPN	50		60		80		ns	
tCSR	10		10		10		ns	
tCHR	120		150		200		ns	
tRPC	0		0		0		ns	

Notes:

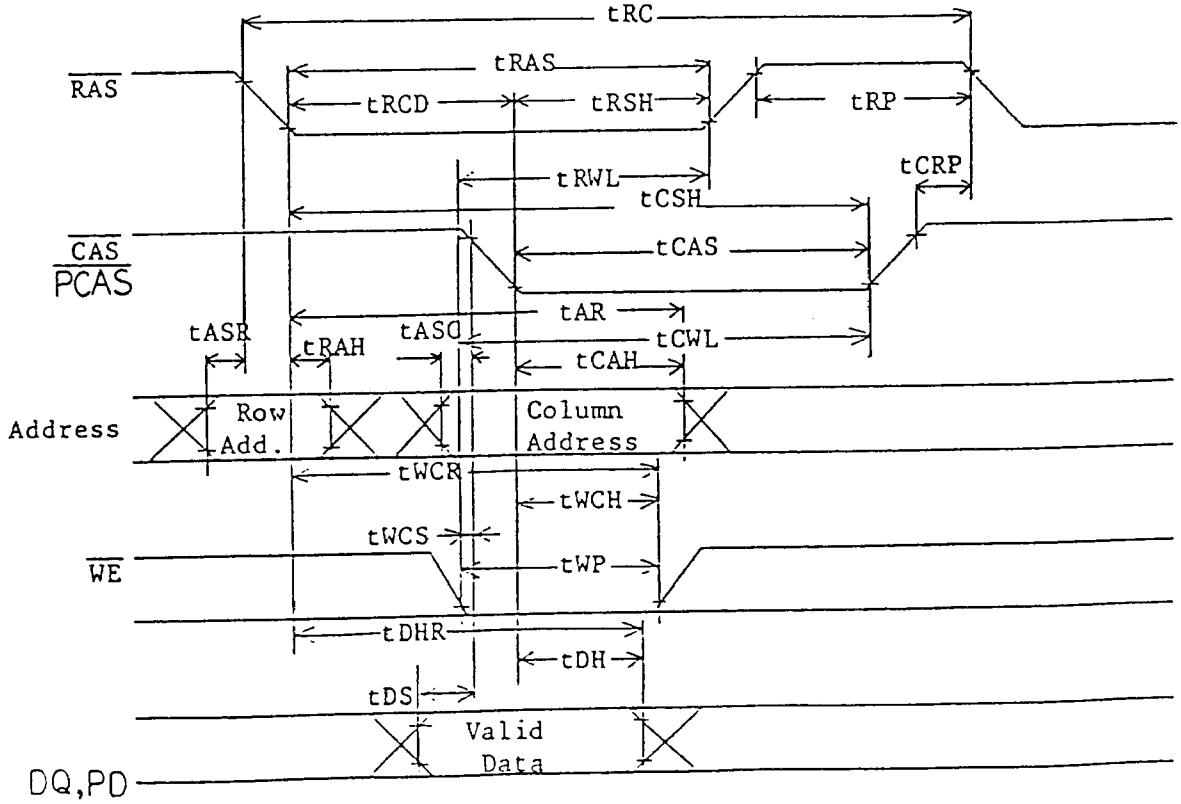
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} < t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100$_p$F.
4. Assumes that $t_{RCD} > t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met; t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. Early write cycle only ($t_{WCS} > t_{WCS}$ (min))
9. An initial pause of 100μs is required after power-up, then execute at least 8 initialization cycles.
10. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycle are required before using internal refresh counter.

■ WAVE FORMS

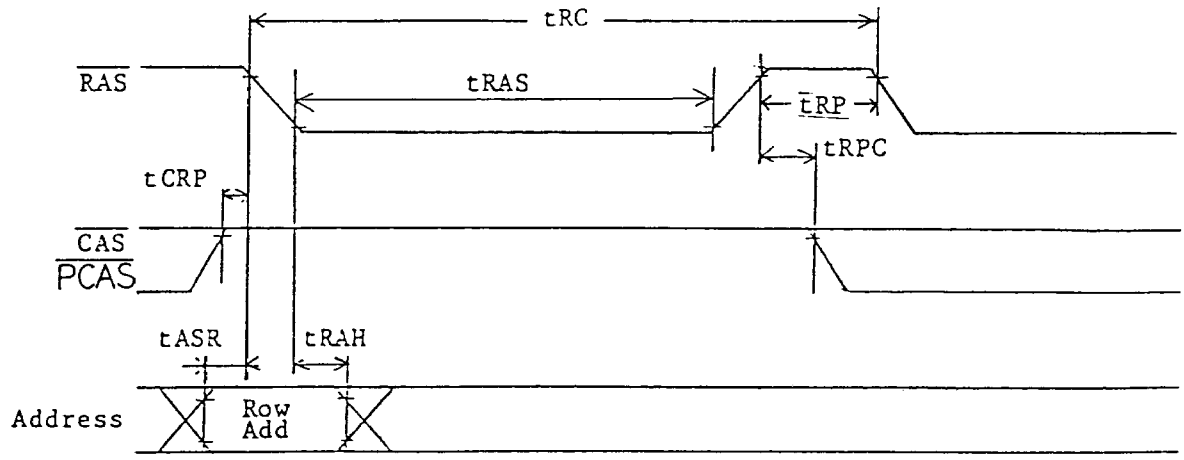
Read Cycle



Write Cycle

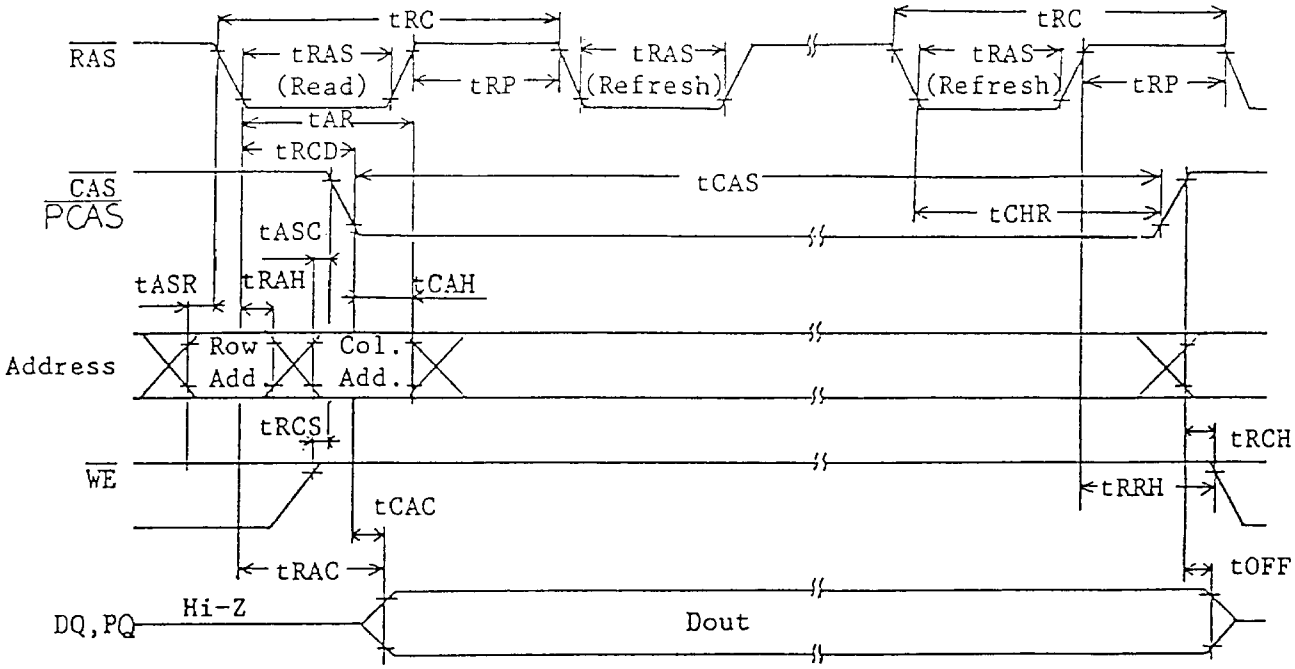


$\overline{\text{RAS}}$ Only Refresh Cycle

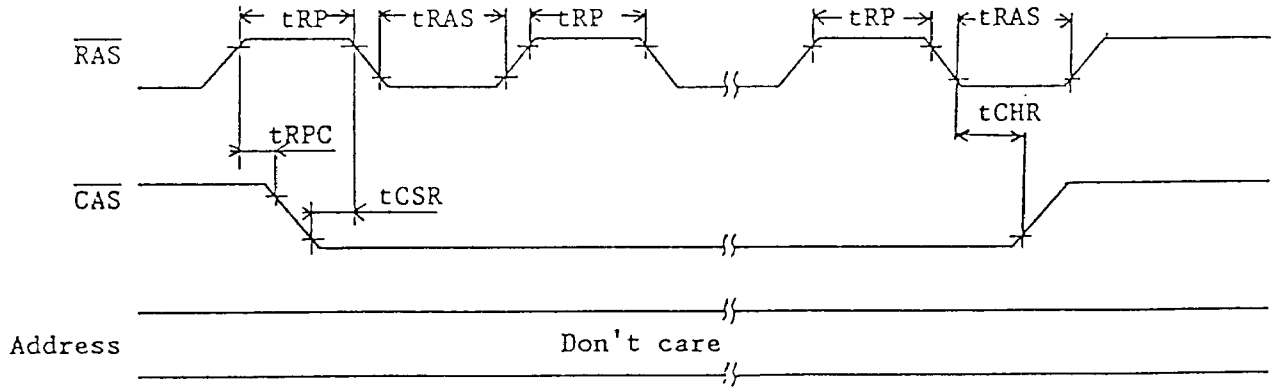


Refresh Address A0–A7 (AX0–AX7)

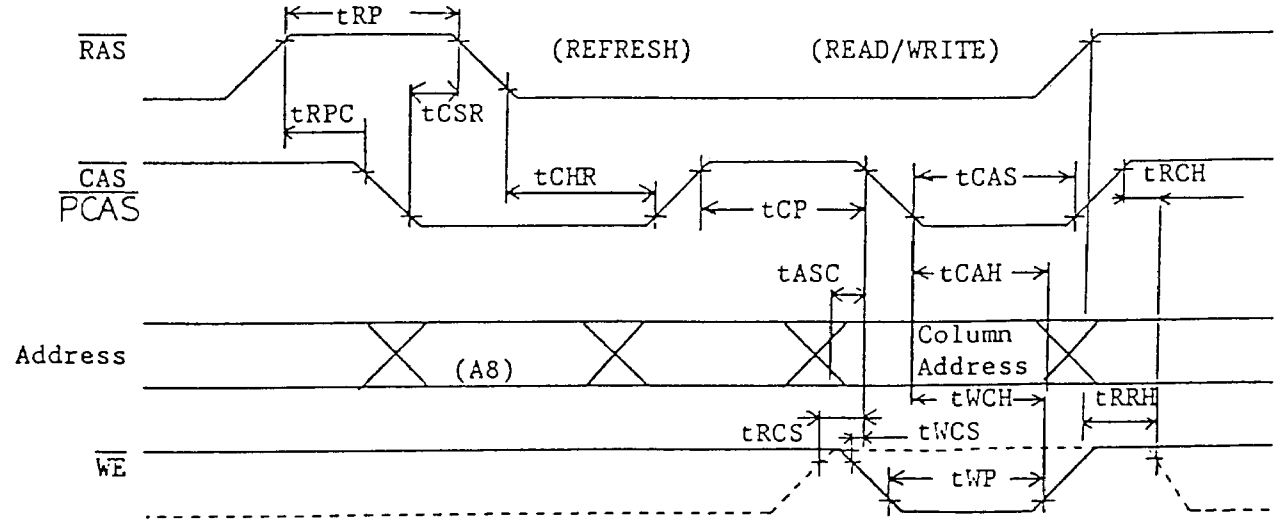
Hidden Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

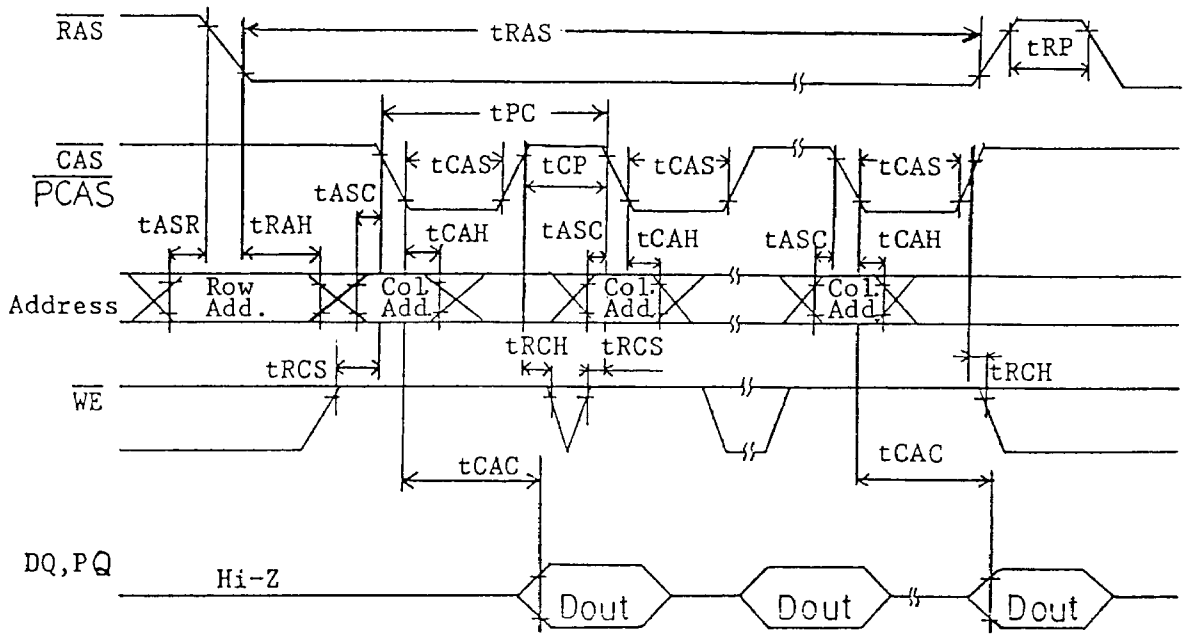


Counter Test

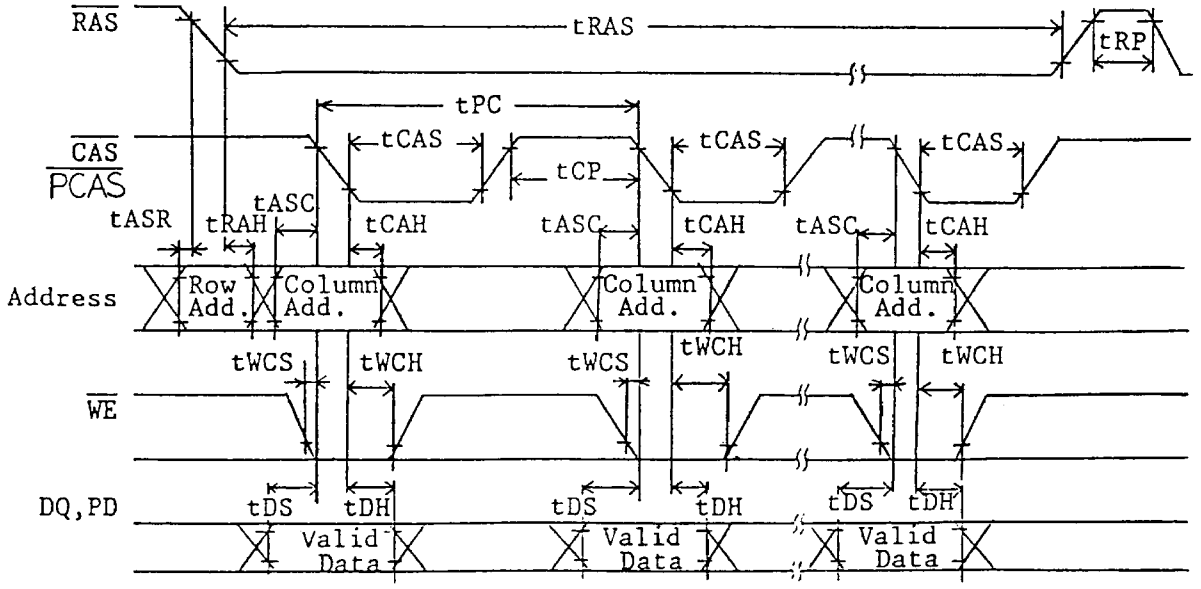


	HB561009A-12		HB561009A-15		HB561009A-20		unit	note
	min	max	min	max	min	max		
Icc7		513		432		333	mA	
tPC	130		145		190		ns	
tCP	50		60		80		ns	

Page Mode Read Cycle



Page Mode Write Cycle



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NOVEMBER, 1986-2

3M Printed in U.S.A.