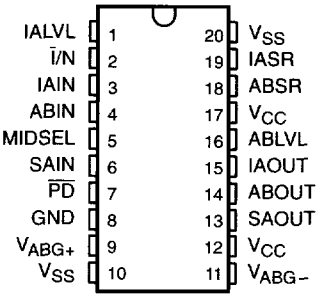
- **TTL-Compatible Inputs**
- **CCD-Compatible Outputs**
- **Variable Output Slew Rates With External Resistor Control**
- **Full-Frame Operation**
- **Frame-Transfer Operation**
- **Solid-State Reliability**
- **Adjustable Clock Levels**

DW PACKAGE
(TOP VIEW)



description

The TMS3473B is a monolithic CMOS integrated circuit designed to drive the parallel image-area gate (IAG), parallel storage-area gate (SAG), and antiblooming gate (ABG) inputs of the Texas Instruments virtual-phase CCD image sensors. The TMS3473B interfaces the CCD image sensor to a user-defined timing generator; it receives TTL input signals from the timing generator and outputs level-shifted and slew-rate-adjusted signals to the image sensor.

The TMS3473B allows operation of the CCD image sensor in either the interlace or noninterlace mode. When the TMS3473B Ī/N input is connected to V_{SS}, the interlace mode is selected (see Figure 1); when Ī/N is connected to V_{CC}, the noninterlace mode is selected (see Figure 2).

The ABOUT output follows the ABIN input and switches between V_{ABG+} and V_{ABG-}. The IAOUT and SAOUT outputs follow the IAIN and SAIN inputs, respectively, and switch between V_{CC} and V_{SS}. Additionally, ABOUT and IAOUT can each be made to output midlevel voltages. DC inputs to ABLVL and IALVL determine the mid-level voltages that can be output on ABOUT and IAOUT, respectively. A high logic level on the MIDSEL input causes ABOUT to output its midlevel voltage; a low logic level on MIDSEL causes IAOUT to output its midlevel voltage if the interlace mode is selected.

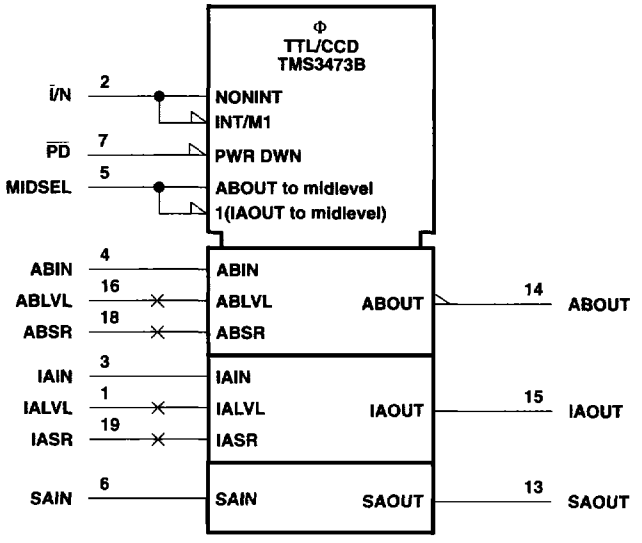
Slew-rate adjustment of the IAOUT and ABOUT outputs is accomplished by connecting IASR to V_{CC} and ABSR to V_{ABG+} through external resistors. The larger the resistor values used, the longer the rise and fall times will be.

A low logic level on the $\overline{PD}$ input causes the TMS3473B to power down and all outputs to assume their low levels (IAOUT and SAOUT to V_{SS}, ABOUT to V_{ABG-}).

The TMS3473B is supplied in the DW package and is characterized for operation from –20°C to 45°C.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

logic symbol



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ABIN	4	I	Antiblooming in
ABLVL	16	I	DC antiblooming midlevel voltage
ABOUT	14	O	Antiblooming out
ABSR	18	I	Antiblooming slew rate
GND	8		Ground
IAIN	3	I	Parallel image area in
IALVL	1	I	DC parallel image area midlevel voltage
IAOUT	15	O	Parallel-image-area out
IASR	19	I	Parallel-image-area slew rate
$\overline{I/N}$	2	I	Interlace/noninterlace select
MIDSEL	5	I	IAOUT/ABOUT midlevel voltage select
$\overline{PD}$	7	I	Power down
SAIN	6	I	Parallel storage area in
SAOUT	13	O	Parallel storage area out
V_{ABG+}	9	I	Positive ABG supply voltage
V_{ABG-}	11	I	Negative ABG supply voltage
V_{CC}†	12	I	Positive supply voltage
V_{CC}†	17	I	Positive supply voltage
V_{SS}†	10	I	Negative supply voltage
V_{SS}†	20	I	Negative supply voltage

† All pins of the same name should be connected together externally.

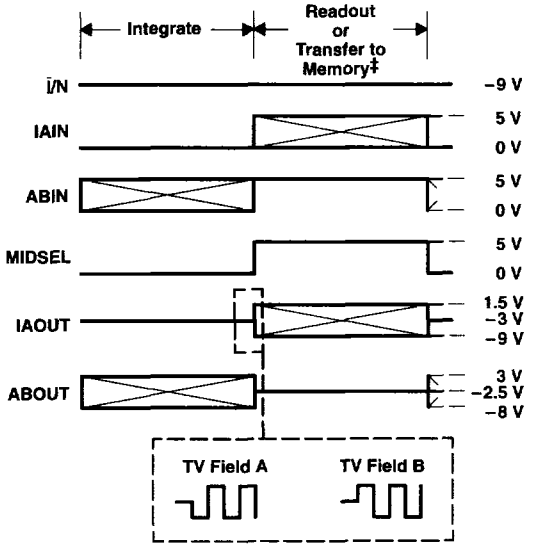


Figure 1. Parallel-Driver Timing Diagram (interlace mode)

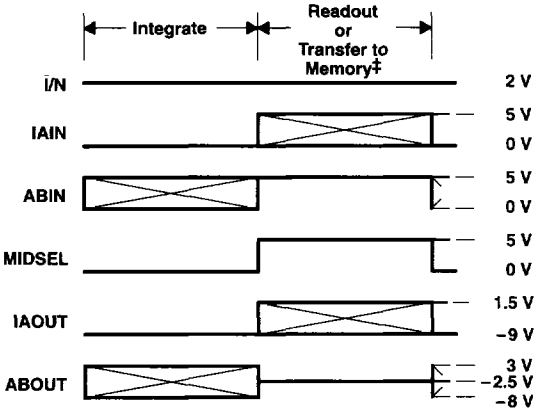


Figure 2. Parallel-Driver Timing Diagram (noninterlace mode)

‡ A readout occurs if the TMS3473B is driving a full-frame CCD image sensor; a transfer to memory occurs if the TMS3473B is driving a frame-transfer CCD image sensor.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply voltage, V_{CC} (see Note 1) ..... 4.4 V
Negative supply voltage, V_{SS} (see Note 2) ..... –11.1 V
Positive ABG supply voltage, V_{ABG+} ..... 5.6 V
Negative ABG supply voltage, V_{ABG-} ..... –8 V
ABG supply voltage differential ($V_{ABG+} - V_{SS}$) ..... 15.2 V
Operating free-air temperature range, T_A ..... –30°C to 75°C
Storage temperature range ..... –55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Continuous total power dissipation, $T_A \leq 25°C$: Unmounted device (see Figure 3) DW package .. 825 mW
Mounted device (see Figure 3) DW package ... 1150 mW

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminal.
2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels only.

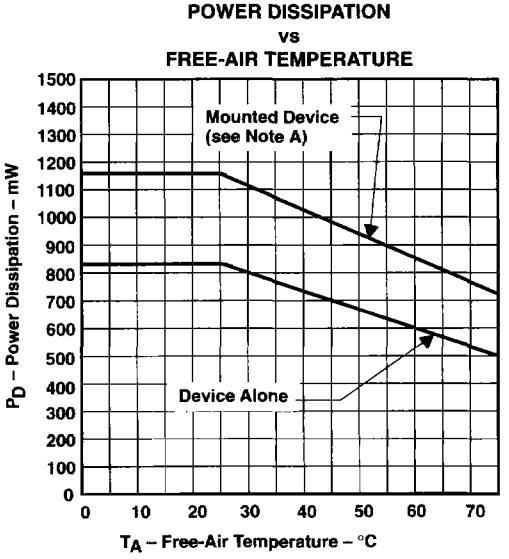


Figure 3

NOTE A: The mounted-device derating curve in Figure 3 was obtained under the following conditions:
The board was 50 mm by 50 mm by 1.6 mm thick.
The board material was glass epoxy.
The copper thickness of all the etch runs was 35 microns.
Etch run dimensions – DW package – All 20 etch runs were 0.4 mm by 22 mm.
Each chip was soldered to the board.
An aluminum cooling fin 10 mm by 10 mm by 1 mm thick was coupled to the chip with thermal paste.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC}†		0	1	4.4	V
Negative supply voltage, V_{SS}†		−11.1	−10	−9.7	V
Positive ABG supply voltage, V_{ABG+}†		1	3.5	4.4	V
Negative ABG supply voltage, V_{ABG-}†		−11.1	−7	−6.2	V
Power supply voltage differential ($V_{CC} - V_{SS}$)				15.5	V
DC parallel image area midlevel voltage, IALVL‡	Z < 5 kΩ	−6	−5	−2	V
DC antiblooming midlevel voltage, ABLVL	Z < 2.5 kΩ	−3.5	−2.5	1	V
High-level input voltage, V_{IH}	ABIN, MIDSEL, $\overline{PD}$, IAIN, or SAIN	2.5	5		V
	I/N	$V_{CC} - 0.4$			
Low-level input voltage, V_{IL}	ABIN, MIDSEL, $\overline{PD}$, IAIN, or SAIN		0	0.9	V
	I/N			$V_{SS} + 0.4$	
Input voltage, V_I	ABLVL	−3.5		1	V
	IALVL	−6		−2	
Clock rate	IAIN, SAIN§			3.58	MHz
	ABIN§			2	
Input resistance, R_{in}	IALVL, ABLVL	2.5			kΩ
Slope resistance bias		10		50	kΩ
Input capacitance, C_{in}	ABLVL	1			μF
Operating free-air temperature, T_A		−20		45	°C

† V_{CC}, V_{SS}, V_{ABG+}, and V_{ABG-} have 100-mA current limits. Adequate decoupling capacitors are required from these pins to ground.
‡ Proper adjustment is required for interlace-mode operation.
§ Different CCD image sensors have different maximum clock rates. See the individual CCD image sensor data sheets for these rates.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 2)

PARAMETER			TEST CONDITIONS†	MIN	MAX	UNIT
V_{OH}	High-level output voltage	ABOUT	I_{OH} = 180 mA (peak)	V_{ABG+} – 0.2	V_{ABG+} + 0.2	V
		IAOUT, SAOUT	I_{OH} = 730 mA (peak)	V_{CC} – 0.5	V_{CC} + 0.5	
V_{OL}	Low-level output voltage	ABOUT	I_{OL} = 180 mA (peak)	V_{ABG-} – 0.3	V_{ABG-} + 0.3	V
		IAOUT, SAOUT	I_{OL} = 730 mA (peak)	V_{SS} – 0.6	V_{SS} + 0.8	
I_{IH}†	High-level input current	ABIN, IAIN, SAIN, MIDSEL, $\overline{PD}$	V_{IH} = 5 V	0	–50	μA
		I/N	V_{IH} = V_{CC} = 2 V		±10	
I_{IL}†	Low-level input current	ABIN, IAIN, SAIN, MIDSEL, $\overline{PD}$	V_{IL} = 0 V		±10	μA
		I/N	V_{IL} = V_{SS} = –10 V		±10	
I_{AB}	Antiblooming current		Average load, See Note 3		20	mA
I_{SS}	Supply current		No load, $\overline{PD}$ = 0 V		1.5	mA
			Average load, See Note 4		25	

† These parameters are measured with V_{SS} = –10.3 V, V_{CC} = 2.1 V, V_{ABG+} = 4.3 V, V_{ABG-} = –7 V, and with IASR connected to V_{CC} and ABSR connected to V_{ABG+}, both through 22-kΩ resistors.

NOTES: 2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels only.

3. The load consists of a TC241 CCD image sensor with the ABG input clocked at 2 MHz using ABG mode 3 (see the TMS3471C data sheet for details on mode 3).

4. The load consists of a TC241 CCD image sensor with the IAG and SAG inputs clocked at 2.1 MHz.

switching characteristics

PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT
t_r	Rise time	ABOUT	V_{CC} = 2.1 V, T_A = 25°C,	V_{ABG+} = 4.3 V, V_{SS} = –10.3 V,	V_{ABG-} = –7 V, See Note 5	60	140	ns
		IAOUT, SAOUT				40	180	
t_f	Fall time	ABOUT				45	100	ns
		IAOUT, SAOUT				30	110	

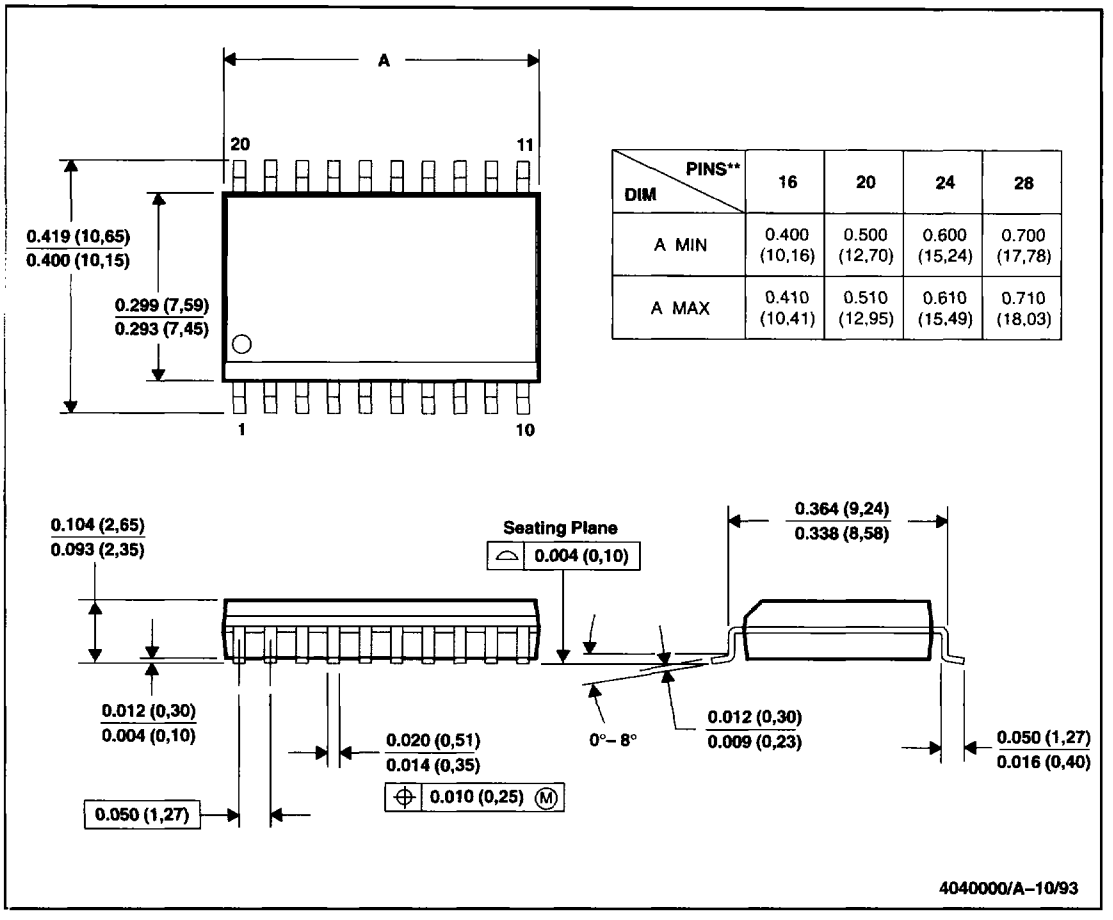
NOTE 5: IASR is connected to V_{CC} and ABSR is connected to V_{ABG+}, both through 22-kΩ resistors. The load consists of a TC241 CCD image sensor with ABG clocked at 2 MHz using ABG mode 3 (see the TMS3471C data sheet for details on mode 3).

MECHANICAL DATA

DW/R-PDSO-G**

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).