POP-3 Device

STM-1/STS-3/STS-3c SDH/SONET POH Terminator with Telecom Bus Interface

TXC-06303

TECHNICAL OVERVIEW

PRODUCT PREVIEW

FEATURES

- Parallel SDH/SONET line interface
  - Parity detection/generation
- Path overhead byte processing
  - RAM access for path overhead bytes
  - B3 byte BIP detection with BER measurement
  - J1 byte TIM or 64-byte LF/CR alignment
  - C2 byte PSL, unequipped, PDI detection
  - G1 byte RDI (single-bit or three-bit), path REI (FEBE) detection
  - H4 byte multiframe detection according to ITU-T G.783 with optional V1 pulse generation
  - K3 byte new byte indication and debouncing for STM-1 operation only
- Path overhead byte insertion
  - From RAM, interfaces, terminal, ring (mate device) or receive side (e.g., RDI)
- N1 byte tandem connection processing with TIM (ETSI) or optional data link access (ANSI)
- Telecom Bus terminal interface
  - Clock, byte data, parity, C1J1V1, SPE, POH byte, AIS indication, bus active indication
- Telecom Bus terminal interface source timing mode
  - Transmit timing for downstream devices from reference clock and frame pulse
  - Optional V1 pulse
- Additional interfaces
  - POH bytes (for VC-4 or each STS-1)
  - Alarm Indication Port (AIP) for path ring operation
  - Scan and drive leads (two each)
- Receive and transmit pointer rejustification to receive and transmit reference clock and frame pulse
  - Pointer leak register control
  - Positive (PJ) and negative (NJ) justification counters
  - Bypass option
- Receive pointer tracking
  - AIS, LOP, NDF and false pointer detection
- Receive and transmit line/path AIS generation, including E1 byte indications
- Motorola or Intel microprocessor interface for memory access
- Boundary scan, loopbacks, optional PRBS generator/detector
- Single +3.3 volt, ±5% power supply; 5 volt input signals accepted
- 256-lead plastic ball grid array package

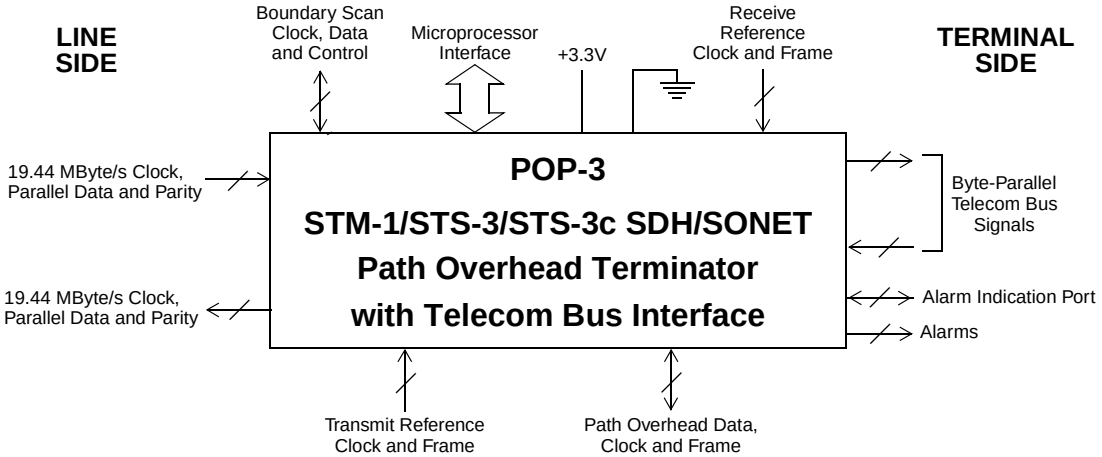
DESCRIPTION

The TranSwitch POP-3 (TXC-06303) is an STM-1/STS-3/STS-3c path overhead processing device that provides a Telecom Bus interface for downstream devices. The POP-3 device provides an 8-bit parallel interface on the line side. The POP-3 performs pointer tracking, and receive and transmit pointer justification. It also performs POH byte processing. All POH bytes are provided in RAM for access by the microprocessor or via the POH interface. In the transmit direction, the POP-3 will either interface to downstream timing or provide the necessary timing. The POH bytes can be inserted from RAM, the serial POH interface, a mate POP-3 device for path ring applications, or directly from the terminal side.

The POP-3 can also generate receive and transmit line and path AIS. For testing, the device provides boundary scan, a PRBS generator and analyzer, B3 byte BER measurements, programmable BIP error mask generation, line and terminal loopbacks, and STS-1 terminal loopback. The POP-3 provides either Motorola or Intel microprocessor access. Performance counters can be configured to be saturating or rollover. The interrupts, with mask bits, can be programmed for activation by positive, negative, or positive and negative, alarm transitions, or positive levels. A software polling register is also provided.

APPLICATIONS

- Add/drop multiplexers
- Cross connect systems
- Data communications systems
- High order multiplexer/terminal systems



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* Please note that TranSwitch provides documentation for all of its products. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

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OVERVIEW

The POP-3 provides a path overhead byte termination for a STM-1 AU-4, STM-1 AU-3, STS-3, or STS-3c format. Upstream line access to the POP-3 is provided by a 19.44 MHz byte-parallel interface.

The POP-3 provides pointer tracking for the STM-1 AU-4, STS-3c, three STM-1 AU-3s or three STS-3 STS-1 formats. The pointer tracking state machine has been implemented based on the requirements specified in the ETSI 1015 document. Both positive and negative pointer movements are counted. In addition to the various alarms provided by this state machine, false concatenation is detected and the size bits can be programmed or disabled.

The POH bytes are monitored and checked, and they are passed through the POP-3 to the receive terminal interface. Processing of the POH bytes includes: J1 byte TIM comparisons, three-bit or single-bit RDI detection, and other related POH functions. A B3 byte bit error rate (BER) measurement circuit and tandem connection processing for the N1 byte are also provided. The tandem connection circuit supports both the ANSI format with programmable HDLC data link access and ETSI message processing. The ETSI format is fully supported, including a 16-byte TIM comparison. The N1 byte may be terminated with B3 byte compensation, or passed through to the receive terminal interface. The POH bytes are also provided at the POH interface for external access.

The POP-3 provides optional pointer justification against a reference clock and frame pulse. Both positive and negative pointer justification events are counted. Each of the three pointer FIFOs is equipped with a 16-bit pointer leak rate adjustment. The H1/H2 byte pointer generation circuit conforms to the state machine specified in ITU-T/ETSI standards. In addition, the size bits in the H1/H2 bytes, and the s-bits in the Y bytes (STM-1 AU4 or STS-3c format), are programmable.

The POP-3 provides the ability to generate path AIS, and a TranSwitch-defined path AIS format at the receive terminal side. Enable bits are used to control the generation of the AIS signal when an alarm is declared. In addition, the microprocessor can control the generation of the various AIS signals.

The receive and transmit terminal interfaces are compatible with the Telecom Bus that TranSwitch uses in its other SDH/SONET products. The receive terminal interface consists of byte-wide data and signals which identify the locations of the POH and payload (SPE) and the C1 (J0) and J1 bytes. In addition, an internal H4 byte multiframe detector/generator can insert a V1 pulse into the C1J1 signal in order to identify the locations of the V1/V2 bytes in the tributary signals for downstream circuits. Other options provided at the terminal interface include a parity bit, a fail indication (AIS) bit, a bus activity indication bit, the ability to force the data bus to a tri-state condition, programmable even or odd parity, the ability to invert the output clock, and a POH byte marker signal.

An option are provided for generating and inserting a fixed A1/A2 framing pattern or a microprocessor-written pattern. In addition, the device can be configured to provide an in-band AIS/RDI indication in the E1 bytes.

In the transmit direction, the POP-3 can be configured to provide a normal timing mode or a source timing mode. In normal timing mode, the downstream device or circuit provides the input timing and data signals. In the source timing mode, the POP-3 provides the timing signals for the downstream device or circuits, with data provided as an input. A data adjustment delay circuit is provided for offsetting the round-trip delay between the downstream circuit and the POP-3.

The POP-3 provides the choice of controlling the insertion of the POH bytes in the STM-1 VC-4 (STS-3c) and individual STM-1 AU-3 (STS-3 STS-1) formats. Individual POH byte control is provided. The insertion of POH bytes into the VC-4 (SPE) or each of the VC-3s (STS-1s) can be bypassed or configured for a path terminating mode. In the bypassed mode, the POH bytes are transmitted in line side format without processing. One exception is made for the N1 byte, which may be used for tandem connection applications. The other mode, path terminating mode, enables the POP-3 to insert the POH bytes into the VC-4 or each of the VC-3 (STS-1) formats from either memory map locations, the POH interface, the local receive side, or a mate POP-3 in a ring configuration. Tandem connection capability is also provided, including the ability to insert an HDLC data chan-

nel for ANSI applications or a 16-byte message and frame, and other signals, for ETSI applications. The ability to generate TCODI, TCRDI, etc., is also provided, with enable bits for the various alarms when the ETSI format is selected.

Optional pointer justification and generation is provided relative to a reference clock and framing pulse. Both positive and negative pointer justification events are counted. A 16-bit pointer leak rate register is provided for the FIFO. The s-bits in the Y bytes and the values of the size bits within the H1/H2 pointer are programmable.

The ability to generate an unequipped, or a supervisory unequipped, format for the VC-4 and for each of the STS-1s is provided. The POP-3 can also be programmed to generate a tributary TU/VT (TU-3, TU-2/VT6, TU-12/VT2, or TU-11/VT1.5) unequipped format. An option is provided in which an external signal can generate a tributary AIS signal in place of the tributary unequipped format. The POP-3 can also generate path AIS based on transmit alarms or under microprocessor control.

The microprocessor interface is selectable for either Intel or Motorola devices. A hardware interrupt and a global software polling register are provided. The software polling register enables the microprocessor to determine the location of the alarm. The interrupt structure uses mask bits for enabling/disabling the individual alarms. The latched bits for controlling the interrupt can be programmed to occur on a positive level (1), positive transition (0 to 1), negative transition (1 to 0), or both positive and negative transitions. Performance counters can be configured to either roll over to zero or to saturate when the count reaches all ones. The BIP/REI (FEBE) performance counters can be configured to count bit errors either individually or as blocks.

Testing capabilities include boundary scan, forcing all output leads to tri-state, BIP error mask with programmable frames in error, a B3 byte BER measurement circuit, line loopback, terminal loopback including looping back individual STS-1s (retiming feature must be enabled), and a PRBS generator and analyzer.

The POP-3 is equipped with two internal processors, one for the receive side and the other for the transmit side. The purpose of the internal processors is to perform many of the POH processes. For example, controlling the alarms which will generate path RDI.

FEATURES

The following is a list of features supported by the POP-3:

- Modes of operation
  - STM-1 AU-4 or STS-3c
    - POH byte termination with transmit pass-through option
  - STM-1 AU-3 or STS-3
    - POH byte termination with transmit pass-through option for each AU-3 or STS-1
- Byte-parallel line interface
  - Byte-wide data at 19.44 MHz
  - Optional framing pulse
  - Loss of clock detection
  - Parity detection (even or odd)
  - Receive clock reference 8 kHz generation
- External access
  - POH byte interface
  - Tandem connection data port interface
    - HDLC port (ANSI)
    - Access to any AU-3/STS-1
- Reference timing interfaces
  - 19.44 MHz clock and frame derived from transmit clock
  - Transmit retiming input (clock and data)
  - Source timing input (clock and data)
  - Receive retiming input (clock and data)
  - Input clocks monitored for loss of clock
- Terminal side interface
  - Telecom Bus standard (interface for SDH/SONET mappers)
    - Plus parity, and POH, bus active, and fail (AIS) indicators
    - Receive A1/A2 byte (fixed or microprocessor-written) insertion option
    - Transmit options
      - Normal timing mode
        - Timing and data signals are inputs
      - Source timing mode
        - Timing signals are outputs
        - Data signals are inputs
- Alarm Indication Port for APS ring applications
  - 81-bit frame with CRC-4 loss of frame and loss of clock detection
    - with CRC-4 error insertion check
  - New K3 byte, debounced K3 byte, B3 errors, path REI, path RDI, loss of signal, loss of frame and CRC-4
  - Write to local counters option for AIP interface: B3, path REI (FEBE)

- Pointer tracking
  - ETSI (ETSI 1015 document state machine)
  - Programmable size bits or disable
  - False concatenation detection
  - Option for AIS/LOP transition bypass
  - LOP, AIS, and NDF alarms
- POH byte termination
  - Receive direction
    - Write to RAM locations in memory map
    - Monitor POH bytes for various alarms
    - Process (e.g., AIS generation) with individual enable bits
    - Pass through POH bytes to terminal
  - Transmit direction
    - Insert into POH bytes
      - From terminal interface
        - With tandem connection option
      - From RAM locations in memory map (i.e., microprocessor-written values)
      - From POH interface
      - From receive side (e.g., RDI)
      - From AIP Port (e.g., RDI)
- POH bytes
  - J1 byte mismatch detection
    - 16-byte trail trace comparison
    - 64-byte (ANSI) with CR/LF alignment
    - No comparison
  - H4 byte
    - Bypass option
    - V1 reference generation
    - Detection and generation
    - LOM and OOF feature of detection (according to G.783)
  - C2 byte
    - Signal label mismatch
    - Unequipped detection and generation
    - VC AIS detection
    - PDI (ANSI) detection
  - G1 byte
    - Single-bit or three-bit RDI detection
    - Alarm enable bits plus processor control
    - REI (path FEBE) counter
    - Bit 8 control

- Tandem connection byte (N1/Z5)
  - Receive and transmit
    - Separate enable control options
  - ETSI TIM/TCODI/TCRDI etc., or ANSI (data link access) format selection
  - B3 byte compensation upon termination option
  - Receive and transmit IEC counters
  - Data link selection for STS-1s
- B3 byte BIP
  - B3 byte BER detection - programmable
  - 16-bit error counters

- Retiming and pointer generation
  - Receive and transmit FIFOs
    - Pointer leak rate is programmable
    - Automatic or microprocessor-controlled recentering capability
    - PJ and NJ counters
  - Programmable size bit selection
  - Programmable Y byte bits
  - Bypass option

- Test features
  - JTAG boundary scan
  - B3 BIP error mask with control of number of frames sent
  - Line loopback
  - Terminal loopback
    - VC-4 or individual STS-1s
  - High-Z all output leads
  - Pattern generator and analyzer
    - 2^{23}-1 pattern according to O-151

- Other features
  - VC-4/AU-3/STS-1 unequipped (force all bytes to zeros)
    - Supervisory unequipped (J1, G1, and B3 bytes valid with 522 Decimal pointer value) option
  - Tributary unequipped generation
    - Option to generate AIS
      - Three TUG-3s in VC-4
      - Any TU2/VT6, TU12/VT2, TU11/VT1.5

- Receive and transmit AIS generation
  - Path AIS
    - With TranSwitch-defined receive path AIS generation
  - Options
    - Microprocessor control
    - Alarms with enable bits
    - External lead option
    - E1 byte in-band indication generation
    - Transmit terminal detection
      - E1 byte
      - H1/H2 bytes

- Alarms and interrupts
  - Latched and unlatched alarms
    - Individual mask bits
  - Software polling register
  - Programmable interrupt transition
    - Positive level (1)
    - Positive transition (0 to 1)
    - Negative transition (1 to 0)
    - Positive and Negative transitions (0 to 1 and 1 to 0)

- Counters
  - Bit or block
  - Roll-over or saturation (with interrupt)

- Microprocessor bus
  - Split address/data buses
  - Selectable Intel or Motorola microprocessor interface compatibility

APPLICATION EXAMPLE

The POP-3 can be used in a wide range of telecommunications applications:

- Add/drop multiplexers
- Cross connect systems
- Data communications systems
- High order multiplexer/terminal systems

Figure 1 shows four POP-3s connected to a TranSwitch PHAST-12. Each POP-3 is provided with a Telecom Bus interface. The Telecom Bus interface allows a connection to a TranSwitch mapper device, such as the L3M, L4M, QE1M or QT1M.

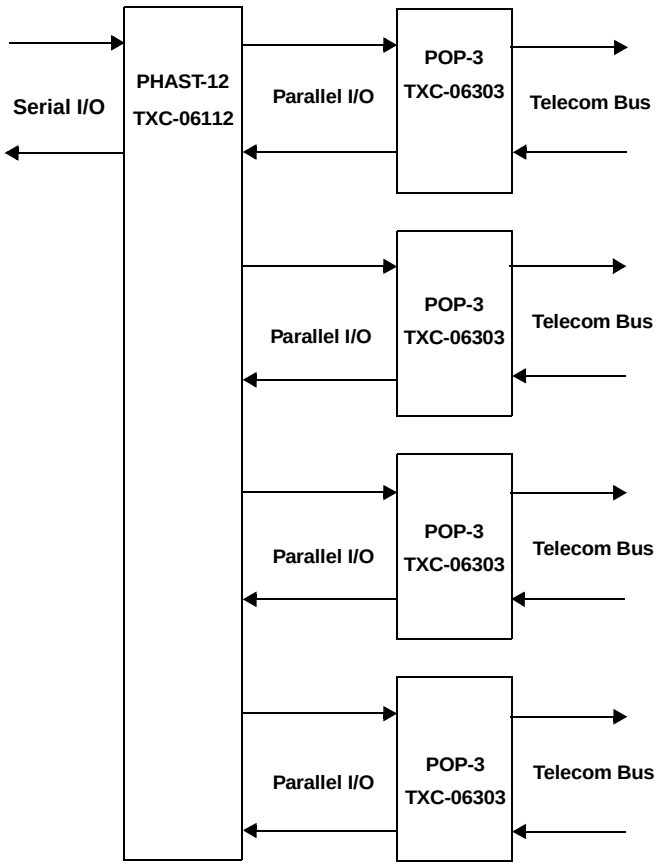

Figure 1. Typical Application using the POP-3 TXC-06303

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FUNCTIONAL DESCRIPTION

A block diagram of the POP-3 is shown in Figure 2 below.

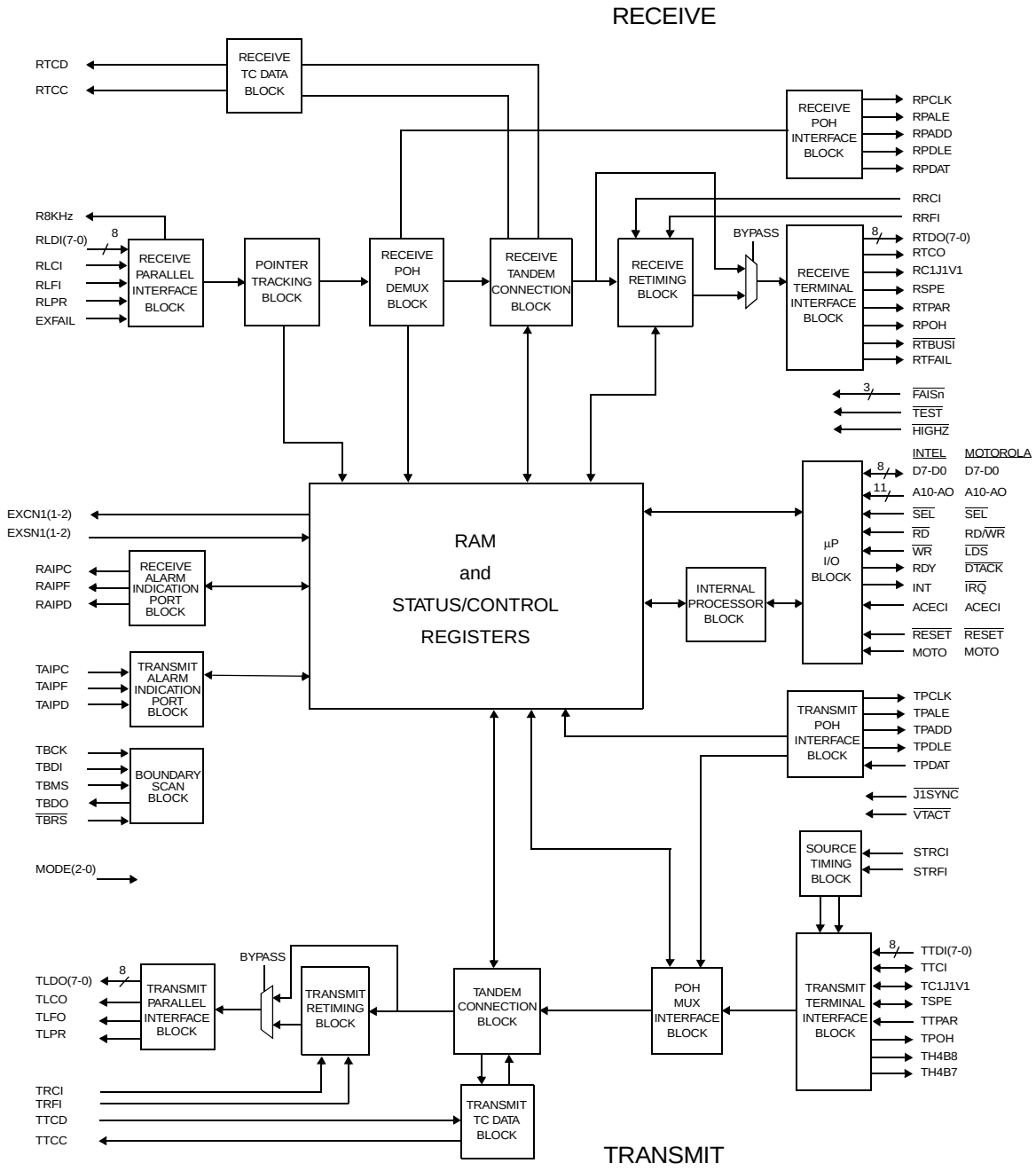

Figure 2. POP-3 TXC-06303 Block Diagram

The receive line side interface connects to the Receive Parallel Interface block. The parallel interface input signals consist of a byte-wide data interface (RLDI(7-0)), a framing pulse (RLFI), clock (RLCI), parity (RLPR), and an external signal fail indicator (EXFAIL). The parity calculation can be selected to be either odd or even, calculated over the data byte or over the data byte plus the framing pulse. Other than providing an indication for the microprocessor, a parity error will have no effect on the operation of the POP-3. However, a bit error in the data

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may cause a BIP error in addition to a parity error. The external signal fail indication can be used for supplying a loss of frame and/or loss of signal indication from an upstream device or circuit. The byte-wide data is also monitored for a loss of signal, with an alarm indication occurring if there are no transitions within the 125 microsecond frame. The 19.44 MHz clock is checked for stuck high or low states. In addition, an 8 kHz clock reference output signal is derived and provided on the R8KHZ lead.

The Pointer Tracking block determines the start of the J1 byte and the payload by processing the pointer bytes H1 and H2. Three pointer tracking state machines are provided for the AU-3 and STS-1 formats. The size bits can be disabled or programmed for the state machine. This block also provides a false concatenation detector. Positive and negative pointer movements are counted. Three alarms are provided: loss of pointer, path AIS and new pointer indication.

The Receive POH Demultiplexer block performs POH byte processing. This includes a 16-byte J1 byte TIM comparison, B3 byte BIP check and BER measurement, C2 byte mismatch, unequipped, VC AIS and PDI detection, G1 byte REI (FEBE) and single-bit or three-bit RDI detection, H4 byte multiframe detection and generation with a V1 pulse option, and K3 byte debouncing and alarm indication when the STM-1 AU-4 format is selected. All POH bytes are written into RAM locations in the memory map for microprocessor access and are provided at the POH interface.

The Receive POH Interface block formats the POH bytes into a serial bit stream for external access. Depending upon the mode of operation, up to three sets of POH bytes will be provided, for each of the AU-3s or STS-1s. The POH interface output signals consist of a clock (RPCLK), address enable signal (RPALE), address signal (RPADD), data enable signal (RPDLE), and data signal (RPDAT).

The Receive Tandem Connection block is responsible for processing the N1 byte, when enabled. The POP-3 can function with either the ANSI or ETSI tandem connection format. For both the ANSI and ETSI formats, the incoming IEC errors are counted. For the ANSI format, control bits are provided for selecting a data link interface for one of the three STS-1s. One of the three STS-1s may be carrying an HDLC data field. The POP-3 will not provide an HDLC controller. For higher order systems this selection can be disabled. For the ETSI format, the POP-3 will calculate the OEI and REI (FEBE) values as well as perform frame alignment, a 16-byte TIM comparison against a microprocessor-written message, TC RDI and TC ODI detection, and it will provide access to the spare bits in the multiframe structure. In addition, the POP-3 can terminate the N1 byte and compensate the B3 byte, or provide the N1 byte directly to downstream circuitry.

The Receive TC Data block formats the programmed data (ANSI), or bits 5 through 8 in the N1 byte (ETSI), for access. The serial data (RTCD) is clocked out by the clock output (RTCC) on its falling edges. The data is asynchronous relative to the frame.

The Receive Retiming block provides payload justification to an external clock (RRCI) and framing pulse (RRFI) using FIFOs. For STS-3 operation, three FIFOs are provided. The retiming block can be bypassed when required. Three measurements are taken, i.e., slow, fast and immediate on each side of center. A 16-bit register is used to control the leak rate. When the FIFO limits are exceeded, it can be reset automatically or by the microprocessor. The pointer is recalculated and inserted into the outgoing bit stream. The size bits and the s-bits in the Y bytes are programmable. Positive and negative justification movements against the reference are counted. The reference clock is also monitored for stuck high and low conditions.

The Receive Terminal Interface block generates line AIS, path AIS, or a TranSwitch-defined path AIS when a receive alarm is declared. A majority of the alarms have enable/disable bits by which an alarm can be prevented from causing the AIS signal downstream. AIS can also be forced using the external leads $\overline{\text{FAIS3}}$, $\overline{\text{FAIS2}}$ and $\overline{\text{FAIS1}}$, when enabled. The same leads can be used to send RDI when enabled. Output signals are data (RTDO(7-0)), clock (RTCO), SPE signal (RSPE), timing signal (RC1J1V1), POH indication signal (RPOH), parity bit (RTPAR), AIS indication (RTFAIL), and a bus activity signal ($\overline{\text{RTBUSI}}$). The output bus can also be forced to a tri-state condition for testing purposes. A clock inversion feature is provided which enables the POP-3 to clock the bus signals out on the opposite clock edge. An option is provided in which the E1/E2 bytes placed on the bus are used as an in-band AIS indication.

In the transmit direction, the Transmit Terminal Interface block provides a byte data interface to downstream cir-

cuitry. In the normal timing mode, data (TTDI(7-0)), clock (TTCI), SPE indicator (TSPE), timing signal (TC1J1V1) and parity (TTPAR) are input signals. When the source timing mode is enabled, the clock (TTCI), SPE indicator (TSPE), timing signal (TC1J1V1), POH column indicator (TPOH), and H4 multiframe indicator (TH4B7 and TH4B8) are output signals and the data (TTDI(7-0)) and parity (TTPAR) are input signals. The source timing mode is used in applications that require the POP-3 to provide the timing signals for downstream circuitry. Control bits are provided to compensate for delays between data and timing signals.

The Source Timing block generates the transmit terminal bus timing signals using an external reference clock (STRCI) and reference framing pulse (STRFI). The clock is monitored for a stuck high or low state.

The Transmit POH Multiplexer Interface block inserts the POH bytes into the transmitted STM-1 VC-4, three STM-1 AU-3s, STS-3c SPE, or three STS-3 STS-1 formats. Two general modes of operation are provided, a pass-through mode and a termination mode. In the pass-through mode, all POH bytes are transferred transparently through this block without processing. Options are provided to select any of the three AU-3s or STS-1s. Thus, one or more AU-3s or STS-1s can be transferred transparently through the POP-3. In path terminating mode, several options are available: the individual bytes may be inserted from a POH interface, from RAM locations in the memory map, from the local receive side for path RDI and REI (FEBE) indications, or by using RDI and REI (FEBE) indicators from an alarm indication port for path protected ring applications.

Unequipped or supervisory unequipped generations are provided. The POP-3 can also be programmed to generate an unequipped format for TU-3s, TU2 (VT6)s, TU12 (VT2)s, or TU11 (VT1.5)s. Using an external pulse ($\overline{\text{VTACT}}$) for the columns of the TU (VT) selected, a tributary AIS condition can be generated instead.

The Transmit POH Interface block provides timing output signals needed for clocking in up to three sets of POH bytes. The POH interface consists of a clock output (TPCLK), address enable signal output (TPALE), address signal output (TPADD), data enable signal output (TPDLE), and input data signal (TPDAT).

The Transmit Tandem Connection block is used for monitoring terminal side IEC errors and inserting tandem connection bit information into the N1 byte for either the ANSI or ETSI format. For the ANSI format, HDLC data from the Transmit TC Data block is inserted into bits 5 through 8 of the selected STS-1. When the ETSI format is selected, the POP-3 inserts the TC REI (FEBE) and TC OEI value, constructs the multiframe structure and inserts a microprocessor-written 16-byte TIM message, TC RDI and ODI states, and provides control of the spare bits in the frame. In addition, the POP-3 can also generate a tandem connection AIS indication.

The Transmit Tandem Connection Data block inputs HDLC serial data (TTCD) using the output clock (TTCC). Data is only supplied for the ANSI tandem connection format. Data is clocked in on rising edges of the clock.

The Transmit Retiming block provides payload justification to an external clock (TRCI) and framing pulse (TRFI) using a FIFO. The retiming block can be bypassed when required. Three measurements are taken, i.e., slow, fast and immediate on each side of center. A 16-bit register is used to control the leak rate. When the FIFO limits are exceeded, it can be reset automatically or by the microprocessor. The pointer is recalculated and inserted into the transmit bit stream. The size bits and the s-bits in the Y bytes are programmable. Positive and negative justification movements against the reference are counted. The reference clock is also monitored for stuck high and low conditions.

The transmit line side interface connects to the Transmit Parallel Interface block. The parallel interface output signals consist of a byte-wide data interface (TLDO(7-0)), framing pulse (TLFO), clock (TLCO), and a parity bit (TLPR). Even or odd parity may be selected, in addition to calculation of parity for the data bytes only or for the data bytes and the framing pulse.

All of the control registers, performance counters, status and alarm indications, and internal processors are accessed through the Microprocessor Input/Output Interface block. The POP-3 supports either an Intel-compatible or a Motorola-compatible microprocessor bus interface, with some signal leads performing different functions according to the type of interface selected via the MOTO lead.

When MOTO is low, the Intel microprocessor bus interface is selected and its signal leads consist of: an 8-bit bidirectional data bus (D7 - D0), an 11-bit address input bus (A10 - A0), a select input ($\overline{\text{SEL}}$), a read input ($\overline{\text{RD}}$), a write input ($\overline{\text{WR}}$), an interrupt request output (INT), and a ready output (RDY). D0 is defined as the least sig-

nificant bit.

When MOTO is high, the Motorola microprocessor bus interface is selected and its signal leads consist of: an 8-bit bidirectional data bus (D7 - D0), an 11-bit address input bus (A10 - A0), a select input ($\overline{SEL}$), an active low LDS ($\overline{LDS}$) signal for 68302 operation, a read/write input (RD/$\overline{WR}$), an interrupt request output ($\overline{IRQ}$), and a data transfer acknowledgment output ($\overline{DTACK}$). D0 is defined as the least significant bit.

An external clock (ACECI), asynchronous with respect to the other clocks connected to the POP-3, is used for the ACE Internal Processor block and for internal RAM arbitration (i.e., internal processor read/write operations versus external microprocessor read/write operations). This clock will operate at a frequency of 60 MHz.

The alarm reporting structure consists of unlatched and latched (event) alarm bit positions. The unlatched alarm bit positions will reflect the current status of the detection circuit (e.g., C2 mismatch detection). A latched alarm (event bit) may be selected to latch on either a positive level, positive transition or negative transition of the associated current status bit. A latched bit position, and all other latched bit positions in a register, are cleared during a microprocessor read cycle for that register.

The latched (event) bits are used to activate a hardware interrupt, when enabled. The POP-3 provides both a hardware indication (INT/$\overline{IRQ}$) and software polling register indications. The software polling register provides a way to have the processor read a register in memory to detect the alarm(s) that caused the interrupt, or the alarms that are set, without having to read all the alarm registers until the active alarms are found.

All counters are capable of counting events as either bits or blocks, unless otherwise specified. All 16-bit performance counters have a special 16-bit read operation which will allow uninterrupted access, without the danger of one byte changing while the other byte is read. All the performance counters can be configured to be either saturating or non-saturating. When a performance counter is configured to be saturating, the counter stops at its all-ones maximum count. A saturating counter is reset on a microprocessor read cycle. When a counter is configured to be non-saturating, it is not cleared on a microprocessor read cycle but continues to count, and it rolls over to all zeros on the count following all ones. Counts that occur during the read cycle are held, with the counter being updated afterwards. All the performance counters can be reset simultaneously by writing to a reset control bit.

The POP-3 supports the following boundary scan test instructions as specified in IEEE 1149.1 documents: EXTEST, SAMPLE, and BYPASS. The boundary scan test bus interface has four input signals: a test clock (TBCK), test mode select (TBMS), test data input (TBDI), and test reset ($\overline{TBRS}$). There is one output signal, test data output (TBDO).

A lead designated as $\overline{HIGHZ}$ is provided for customer testing. An active low placed on this lead sets all output leads except TBDO to the high impedance state for board testing.

In addition to line loopback, the POP-3 provides a test generator and analyzer that uses the PRBS sequence 2^{23}-1, which is defined by the ITU-T O.151 recommendation.

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SELECTED PARAMETER VALUES

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	3.9	V	Note 1
DC input voltage	V_{IN}	-0.5	5.0	V	Note 1, 3
Storage temperature range	T_S	-40	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Component Temperature x Time	TI		270 x 5	^oC x s	
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD		±2000	V	per MIL-STD-883D Method 3015.7

Notes:
1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended or warranted.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient			25	$^oC/W$	0 ft/min linear airflow.

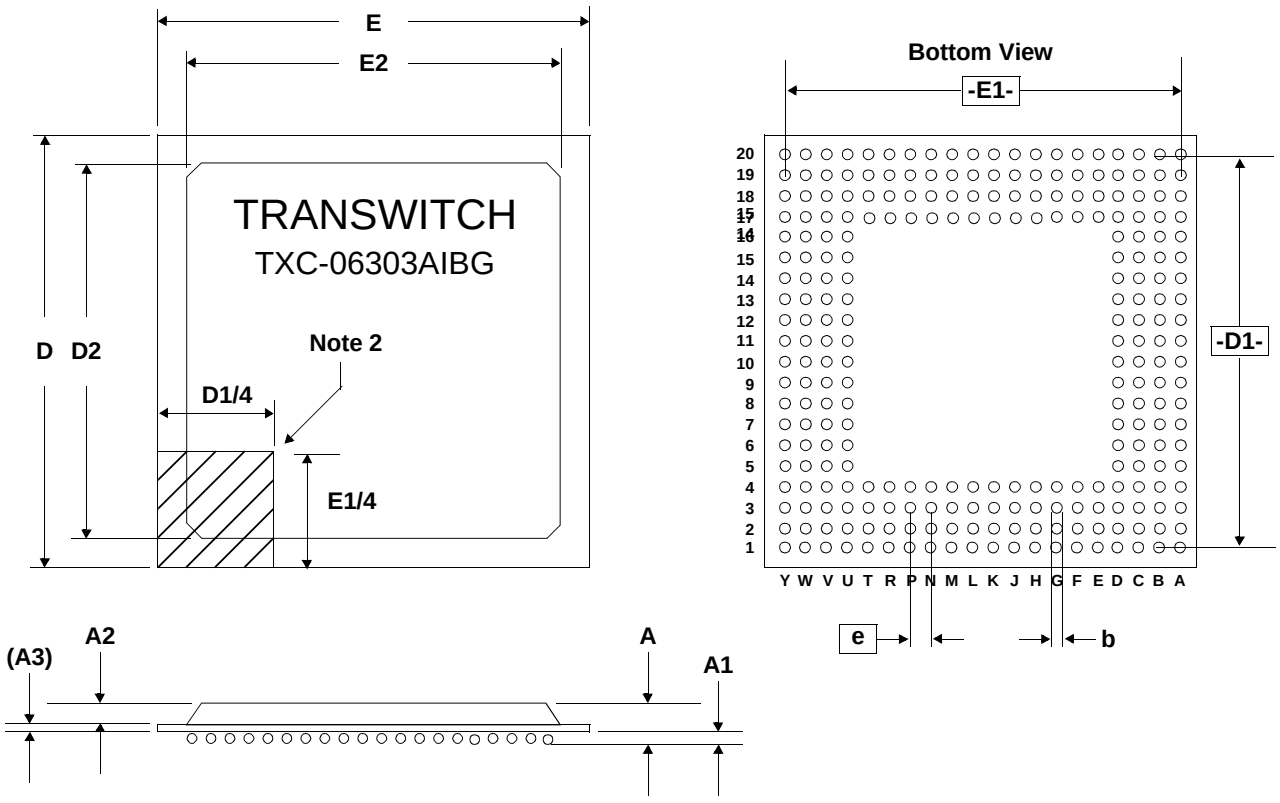
POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.15	3.30	3.45	V	
I_{DD}			243	mA	
Power Dissipation, P_{DD}			800	mW	

PRODUCT PREVIEW

PACKAGE INFORMATION

The POP-3 device is packaged in a 256-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 3**.**



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 20 x 20, JEDEC code MO-151-BAL-2.

Dimension (Note 1)	Min	Max
A	1.92	2.32
A1	0.50	0.70
A2	1.12	1.22
A3 (Ref.)	0.36	
b	0.60	0.90
D	27.00	
D1 (BSC)	24.13	
D2	23.50	24.70
E	27.00	
E1 (BSC)	24.13	
E2	23.50	24.70
e (BSC)	1.27	

Figure 3. POP-3 TXC-06303 256-Lead Plastic Ball Grid Array Package

PRODUCT PREVIEW

ORDERING INFORMATION

Part Number: TXC-06303AIBG 256-Lead Plastic Ball Grid Array Package

RELATED PRODUCTS

TXC-03452B, L3M VLSI Device (Level 3 Mapper). Maps a 44.736 Mbit/s DS3 or 34.368 Mbit/s E3 asynchronous line signal into an STM-1/STS-3/STS-1 formatted synchronous signal. Separate add/drop bus timing is available for loop multiplexers. The L3M provides the overhead processing for the mapped signal.

TXC-03456, L4M VLSI Device (Level 4 Mapper). Maps a 139.264 Mbit/s asynchronous line signal into an AU-4 VC-4/STS-3c SPE signal. The SONET/SDH signal is transmitted via the add bus with timing derived from the drop bus, add bus or an external source. The L4M provides test features such as line loopback, SONET/SDH loopback and on-chip test pattern generator and analyzer. The L4M meets strict jitter requirements to transport broadcast grade video signals.

TXC-04001B, ADMA-T1 VLSI Device (Dual 1.5-Mbit/s T1 to VT1.5/TU-11 Async Mapper-Desync). Maps two 1.544 Mbit/s DS1 signals into any two selected asynchronous mode VT1.5 virtual tributaries carried in a SONET STS-1 synchronous payload envelope. The DS1 signal interface provides selectable AMI or B8ZS coding and decoding, or NRZ operation. The ADMA-T1 interfaces with the PHAST-1, PHAST-3, SOT-1 or SOT-3 overhead terminator devices.

TXC-04002B, ADMA-E1 VLSI Device (Dual 2-Mbit/s E1 to TU-12 Async Mapper-Desync). Maps two 2.048 Mbit/s E1 signals into any two selected asynchronous mode TU-12 virtual tributaries carried in an SDH STM-1 signal (155.52 Mbit/s). The E1 serial signals are positive/negative rail with HDB3 coding and decoding, or optionally an NRZ data stream. The ADMA-E1 interfaces with the PHAST-3 or SOT-3 overhead terminator device.

TXC-04011, ADMA-T1P VLSI Device (Dual 1.5-Mbit/s T1 to VT1.5/TU-11 Async Mapper-Desync). This device is similar to the ADMA-T1 but has extended features and is supplied in a package with additional pins.

TXC-04251, QT1M VLSI Device (Quad T1 Mapper). Maps four 1.544 Mbit/s DS1 signals to and from asynchronous Virtual Tributaries 1.5 (VT1.5s) or Tributary Unit - 11s (TU-11s). A dual Telecom Bus is supported at either 19.44 MHz (STM-1/STS-3, 84 slots) or 6.48 MHz (STS-1, 28 slots) for add/drop or terminal systems. The QT1M interfaces with the PHAST-1, PHAST-3, SOT-1 or SOT-3 overhead terminator devices. It is the next-generation successor to the ADMA-T1 TXC-04001B two-channel device.

TXC-04252, QE1M VLSI Device (Quad E1 Mapper). Maps four 2.048 Mbit/s E1 signals to and from asynchronous Virtual Tributaries 2 (VT2s) or Tributary Unit - 12s (TU-12s). The QE1M contains a RISC microprocessor to handle VT-POH and VT alarms for both direct and tandem connection applications. A dual Telecom Bus is supported at either 19.44 MHz (STM-1/STS-3, 63 slots) or 6.48 MHz (STS-1, 21 slots) for add/drop or terminal systems. The QE1M interfaces with the PHAST-1, PHAST-3, SOT-1 or SOT-3 overhead terminator devices. It is the next-generation successor to the ADMA-E1 TXC-04002B two-channel device.

TXC-06112, PHAST-12 VLSI Device (Programmable, High-Performance ATM, SONET/SDH Terminator for Level 12). A single PHAST-12 device can terminate four individual STS-3c or STM-1 lines or a single OC-12/12c or STM-4/4c line. The PHAST-12 can terminate ATM payloads from any of the above signals into either a single 16-bit or 8-bit UTOPIA Level 1 PHY interfaces.

- NOTES -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