

SP93808

SUB-NANOSECOND OCTAL COMPARATOR

The SP93808 contains eight independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The gain of this comparator has been optimised for low propagation delay and high stability, therefore hysteresis is rarely required.

Each channel includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. The SP93808 can also be used as two matched quad devices, due to comparators 1 to 4 being clocked separately from comparators 5 to 8.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

ORDERING INFORMATION

SP93808 B HG (Industrial - Quad Cerpac (J-Form) package)

FEATURES

- -40°C to +85°C Temperature Range
- Typical Delay < 1 ns
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 8 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching < 100ps
- High Input Impedance
- Dual and Quad Versions SP93802/SP93804

APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers

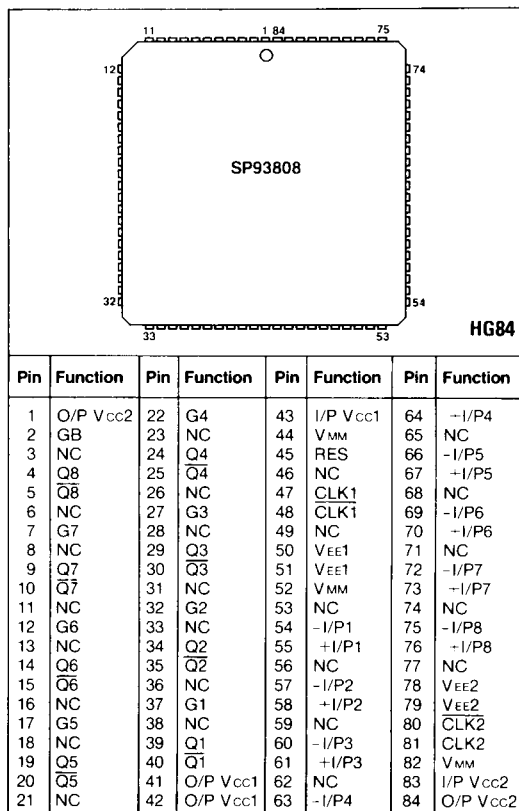


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V _{CC} - V _{MM}	+6V
Supply voltage V _{MM} - V _{EE}	-6V
Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C
Output current	≤30mA
Maximum input voltage	
Common mode positive	≤V _{CC}
Common mode negative	≥V _{EE}
Differential input voltage	≤±3.8V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$, I/P and O/P $V_{CC} = +5V \pm 0.25V$,
 $V_{EE} = -5V \pm 0.25V$, $V_{MM} = 0V$ (see Fig.4), Load = 50Ω to $V_{CC} - 2V$

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current	I_{CC}		65.5	84	mA	$V_{CC} = 5V$, $V_{EE} = -5V$ No load. Each comparator.
Negative supply current	I_{EE}		33.0	42	mA	$V_{CC} = 5V$, $V_{EE} = -5V$ No load. Each comparator.
Positive supply voltage	V_{CC}	I/P MAX +1.55	5.0	I/P MIN +7.3	V	
Negative supply voltage	V_{EE}	-5.5	-5	-4.9	V	
Input offset voltage	V_{OS}	-3.5		+3.5	mV	
Input bias current	I_B		5.25	9	μA	
Input offset current	I_{OS}		0.95	1.2	μA	
Input capacitance	C_I		1.5		pF	
Input impedance	R_I		(Note 1) 250		k Ω	Measured at DC
Differential input range	V_{DIF}			± 3.8	V	
Common mode input range	CMIR	-2.1		+2.6	V	
Output voltage high	V_{OH}	$V_{CC} - 1.050$		$V_{CC} - 0.81$	V	+25°C, $V_{IN} > 60mV$
		$V_{CC} - 1.140$		$V_{CC} - 0.91$	V	-40°C, $V_{IN} > 60mV$
		$V_{CC} - 0.965$		$V_{CC} - 0.704$	V	+85°C, $V_{IN} > 60mV$
Output voltage low	V_{OL}	$V_{CC} - 1.712$		$V_{CC} - 1.544$	V	+25°C, $V_{IN} < -60mV$
		$V_{CC} - 1.792$		$V_{CC} - 1.650$	V	-40°C, $V_{IN} < -60mV$
		$V_{CC} - 1.638$		$V_{CC} - 1.465$	V	+85°C, $V_{IN} < -60mV$
Gain (transparent mode)			20		dB	Differential
Common mode rejection	CMRR	50	50		dB	+25°C, with respect to I/P
Supply voltage rejection	PSRR		70		dB	+25°C, with respect to I/P offset
Clock input:						
Common mode range	CMRC	$V_{MM} + 2V$		$V_{CC} - 1.35V$	V	
Differential swing	DS	400		1600	mV	

NOTES 1. Guaranteed but not tested.

Dynamic Characteristics (Note 1) See dynamic test circuit Fig.9.

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Latch setup time	t_s		150		ps	20mV overdrive
Hold time	t_h		600		ps	20mV overdrive
Input to Q delay	t_{IQ}		800		ps	20mV overdrive
Latch to Q delay	t_{LQ}		1500		ps	20mV overdrive
Glitch capture regeneration	t_{RD}		900		ps	20mV overdrive at Qn
Propagation delay matching	t_{PDM}	-100		+100	ps	Within each device
Min. compare pulse width	t_{PW}		950		ps	20mV overdrive
Min. reset pulse width	t_{RM}		800		ps	
Max. flip flop reset time	t_{RR}		800		ps	
Min. hold time of Qn after reset	t_{GH}		800		ps	
Delay between Qn and Gn	t_{QG}		900		ps	
Propagation delay RES to Gn	t_{RG}		800		ps	

NOTES 1. Guaranteed but not tested.

PIN FUNCTIONS

Name	Pin	Description
I/P V _{cc1}	43	Positive supply connection for comparators 1 to 4, and the bandgap reference.
O/P V _{cc1}	41 & 42	Positive supply connection for the outputs Q _n , \bar{Q}_n and G _n of comparators 1 to 4 (emitter follower outputs, see Fig.5).
I/P V _{cc2}	83	Positive supply connection for comparators 5 to 8.
O/P V _{cc2}	1 & 84	Positive supply connection for the outputs Q _n , \bar{Q}_n and G _n of comparators 5 to 8 (emitter follower outputs, see Fig.5).
-I/P _n +I/P _n	54/55, 57/58, 60/61, 63/64, 66/67, 69/70, 72/73, 75/76	Inverting and non-inverting inputs to comparators 1 to 8, respectively.
Q _n /Q _n	40/39, 35/34, 30/29, 25/24, 20/19, 15/14, 10/9, 5/4	Q and \bar{Q} outputs of comparators 1 to 8, respectively.
G _n	37,32,27,22, 17,12,7,2	Outputs of glitch capture circuits 1 to 8, respectively.
RES	45	Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (G _n) of the Glitch capture circuits to '0'.
CLK1, $\overline{\text{CLK1}}$	47,48	Clock input pins for comparators 1 to 4. ECL active low signal which latches the outputs of comparators 1 to 4.
CLK2, $\overline{\text{CLK2}}$	80,81	Clock input pins for comparators 5 to 8. ECL active low signal which latches the outputs of comparators 5 to 8.
V _{EE1}	50 & 51	Negative supply voltage for comparators 1 to 4.
V _{EE2}	78 & 79	Negative supply voltage for comparators 5 to 8.
V _{MM}	44,82,52	Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref.

OPERATING NOTES

Transparent Mode

The SP93808 has been designed to maximise high input impedance and minimise propagation delay whilst maintaining a high gain.

While CLK is high ($\overline{\text{CLK}}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 20dB. In this mode, for example, a 20mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93808 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{\text{CLK}}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

Supply Connections

The SP93808 operates from supply voltages of 0V, -5V and -10V (Fig.3) or $\pm 5V$ (Fig.4). The choice of supply

connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from V_{cc}, then to interface with other ECL circuits directly, supplies of 0V, -5V, -10V should be provided. This will give an input common mode range of -2.4V to -7.3V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage (V_{MM}), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

Note that the O/P V_{cc} pins are connected to the collectors of the output emitter followers; load return currents should therefore be directed towards these device pins.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5V supply is not available.

The SP93808 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5V rails.

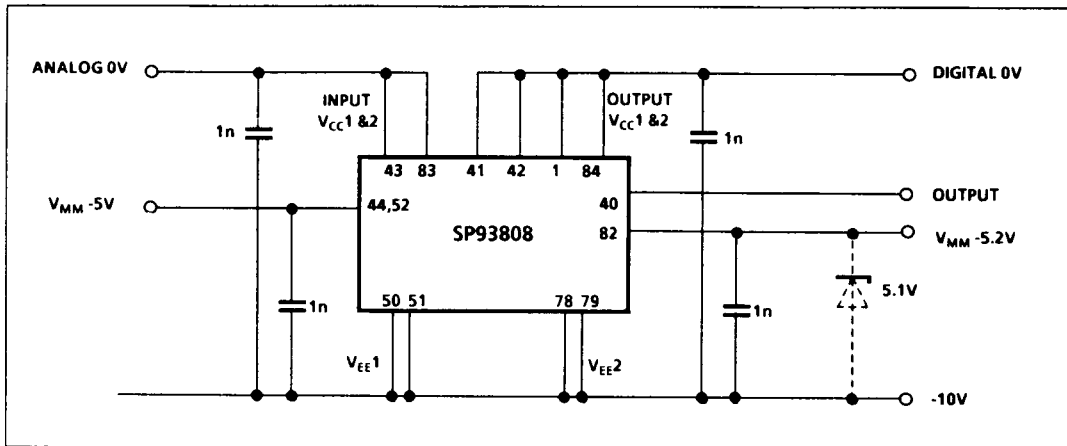


Fig.3 Connection to 0V, -5V and -10V

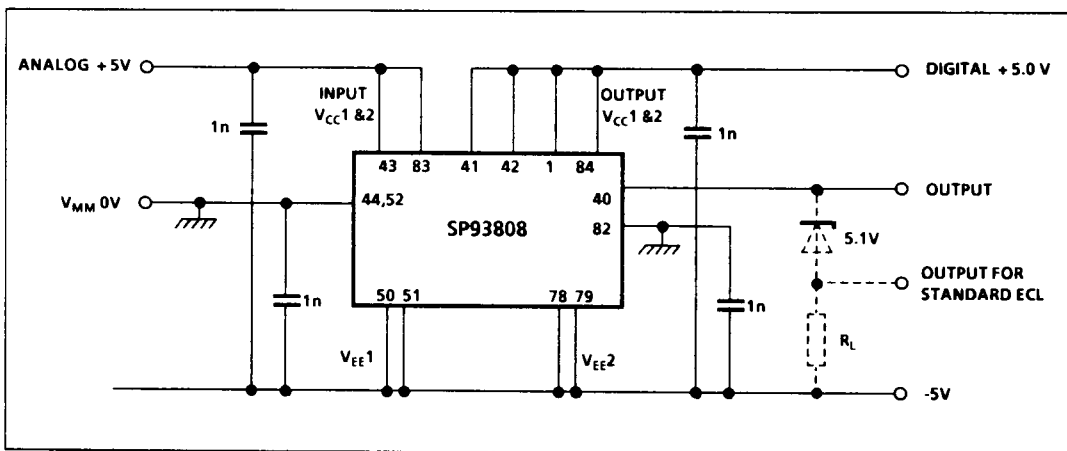


Fig.4 Connection to $\pm 5V$

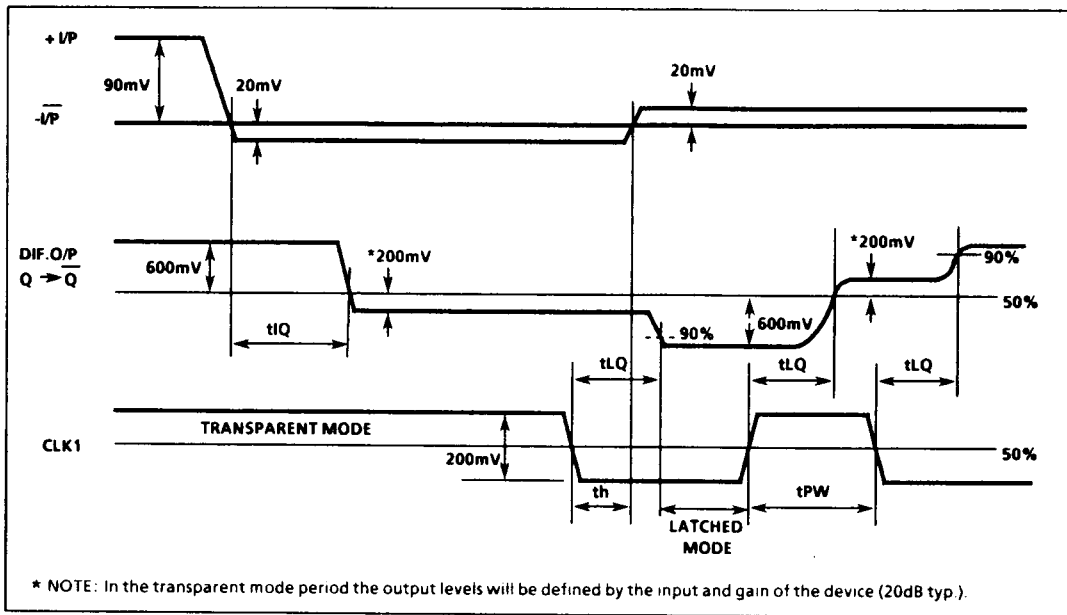


Fig.6 Comparator timing diagram

I/P	CLK	Q _n + 1
X	0	Q _n
1	1	1
0	1	0

X = Don't Care

Table 1 Truth table for comparator

Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' (V_{CC}-0.8V) the RES pin will reset the G_n output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Q_n goes positive by more than 20mV for a time > t_{RD} then the G_n output will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

RES	SET(1) (n + 1)	G _n + 1
1	X	0
0		
0		1
0	1	1
0	0	G _n (2)
	1	
	0	0

X = Don't Care

Table 2 Truth table for glitch capture circuit

NOTES

- 1 SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.8.
- 2 G_n = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

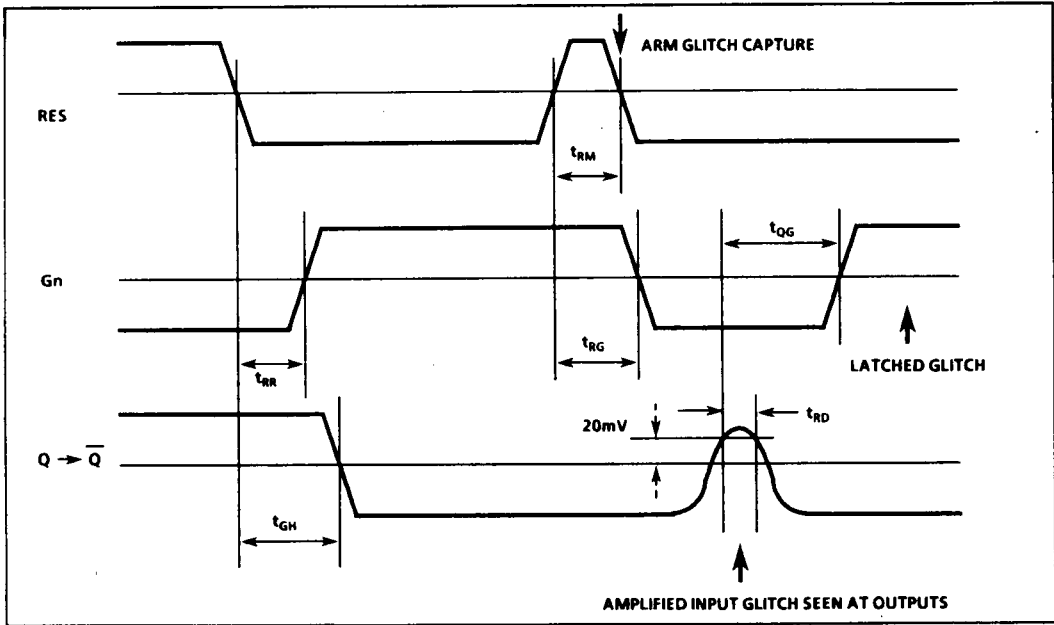


Fig.7 Glitch capture circuit timing

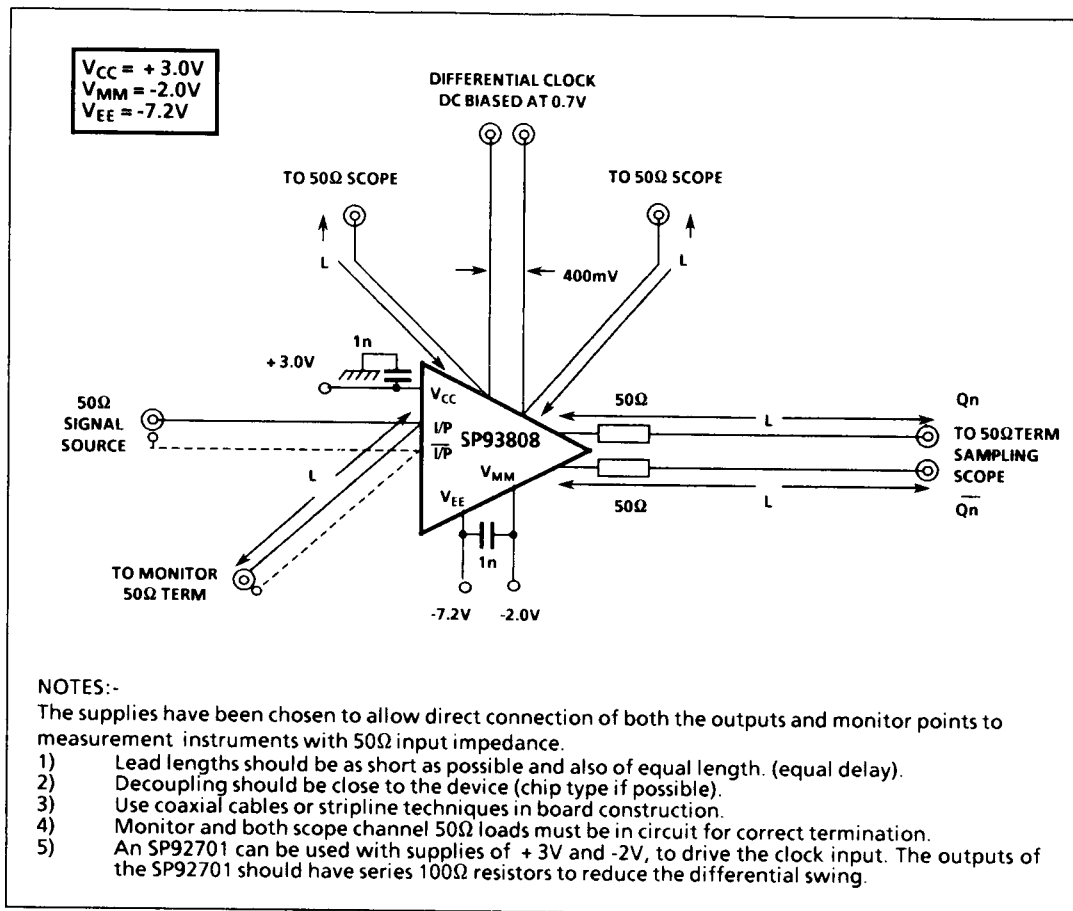


Fig.8 - Comparator Test Circuit (one channel)