4Mx1 Dynamic RAM CMOS, Monolithic

ADVANCE INFORMATION

The EDI414096C is a high performance, low power CMOS Dynamic RAM organized as 4Megabits x1. The use of four-layer poly process, combined with silicide technology and a single transistor dynamic storage cell, provide high circuit density with high performance.

The use of dynamic circuitry, including sense amplifiers, assures low power dissipation.

Multiplexed address inputs permit a low pin count for maximum system density.

In addition to the RAS\-only refresh mode, the hidden refresh mode and CAS\ before RAS\ refresh mode are available.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

Military product compliant to MIL-STD-883, paragraph 1.2.1, is available.

Features

4Mx1 bit CMOS Dynamic Random Access Memory

- Access Times 80, 100, 120, and 150ns
- Low Operating Power Dissipation
- Low Standby Power
- All Inputs/Outputs TTL Compatible

Package Styles

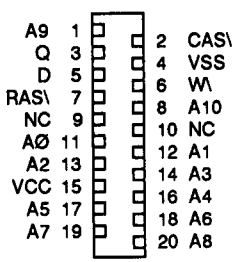
- 20(26) Lead Ceramic SOJ, No. 16
- 20 pin Ceramic ZIP, No.18

Single +5V (±10%) Supply Operation

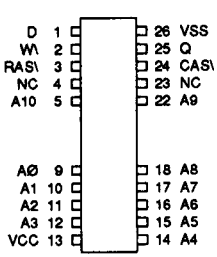
Pin Names

AØ-A10	Address Inputs
CAS\	Column Address Strobe
RAS\	Row Address Strobe
W\	Write Control Input
D	Data Input
Q	Data Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Pin Configurations and Block Diagram



ZIP



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