256M (8Mx32) GDDR3 SDRAM

HY5RS573225F

Revision History

Revision No.	History	Draft Date	Remark
0.1	Defined target spec.	Apr. 2003	
0.2	Full Revision	Oct. 2003	
0.3	Defined IDD Spec.	Dec. 2003	
0.4	Insert AC parameter (-12/ -13/ -14/ -15)	Apr. 2004	
0.5	Changed VDD/VDDQ from 1.8V to 2.0V in all frequencies	May 2004	
0.6	tRPRE, tRPST, tWPRE min/ max change	Oct. 2004	
0.7	AC, DC Parameter Change	Feb. 2005	
1.0	Driver Strength, IDD6, tDQSH/L, tCH/L change & tRCDW insert	Mar. 2005	
1.1	Changed IDD Value (2P/ 3P)	Sep. 2005	

DESCRIPTION

The Hynix HY5RS573225 is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. The Hynix HY5RS573225 is internally configured as a quad-bank DRAM.

The Hynix HY5RS573225 uses a double data rate architecture to achieve high-speed opreration. The double date rate architecture is essentially a 4n-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the Hynix HY5RS573225 consists of a 4n-bit wide, every two-clock-cycles data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the Hynix HY5RS573225 is burst oriented; accesses start at a selected locations and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ of WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access. Prior to normal operation, the Hynix HY5RS573225 must be initialized.

FEATURES

- V_{DD}=2.0V ± 0.1V, V_{DDQ}=2.0V ± 0.1V
- Single ended READ Strobe (RDQS) per byte
- Single ended WRITE Strobe (WDQS) per byte
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Calibrated output drive
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- RDQS edge-aligned with data for READs; with WDQS center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data mask (DM) for masking WRITE data
- 4n prefetch
- Programmable burst lengths: 4
- 32ms, 4K-cycle auto refresh
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 1.8v Pseudo Open Drain I/O
- Concurrent Auto Precharge support
- tRAS lockout support, Active Termination support
- Programmable Write latency(1,2 or 3)

ORDERING INFORMATION

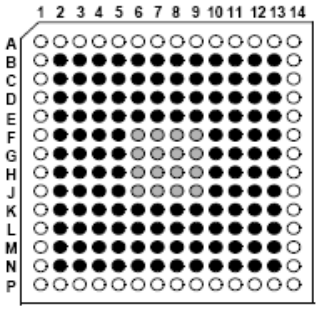
Part No.	Power Supply	Clock Frequency	Max Data Rate	Interface	Package
HY5RS573225F-12	VDD=2.0V, VDDQ=2.0V	800MHz	1600Mbps/pin	POD_18	12mmx12mm 144Ball FBGA
HY5RS573225F-13		750MHz	1500Mbps/pin		
HY5RS573225F-14		700MHz	1400Mbps/pin		
HY5RS573225F-15		650MHz	1300Mbps/pin		
HY5RS573225F-16		600MHz	1200Mbps/pin		
HY5RS573225F-18		550MHz	1100Mbps/pin		
HY5RS573225F-2		500MHz	1000Mbps/pin		
HY5RS573225F-22		450MHz	900Mbps/pin		

BALLOUT CONFIGURATION

	2	3	4	5	6	7	8	9	10	11	12	13
B	WDQS0	RDQS0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	RDQS3	WDQS3
C	DQ4	DM0	VDDQ	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	VDDQ	DM3	DQ27
D	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
E	DQ7	RFU3	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	RFU4	DQ24
F	DQ17	DQ16	VDDQ	VSSQ	VSS therm	VSS therm	VSS therm	VSS therm	VSSQ	VDDQ	DQ15	DQ14
G	DQ19	DQ18	VDDQ	VSSQ	VSS therm	VSS therm	VSS therm	VSS therm	VSSQ	VDDQ	DQ13	DQ12
H	WDQS2	RDQS2	VDDQ	VSSQ	VSS therm	VSS therm	VSS therm	VSS therm	VSSQ	VDDQ	RDQS1	WDQS1
J	DQ20	DM2	VDDQ	VSSQ	VSS therm	VSS therm	VSS therm	VSS therm	VSSQ	VDDQ	DM1	DQ11
K	DQ21	DQ22	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ10
L	DQ23	A3	VDD	VSS	RFU2	VDD	VDD	RFU1	VSS	VDD	A4	DQ8
M	VREF	A2	A10	$\overline{RAS}$	RESET	CKE	RFU5	ZQ	$\overline{CS}$	A9	A5	VREF
N	A0	A1	A11	BA0	$\overline{CAS}$	CK	$\overline{CK}$	$\overline{WE}$	BA1	A8/AP	A6	A7

	8M x 32
Configuration	2M x 32 x 4 banks
Refresh Count	4k
Bank Address	BA0, BA1
Row Address	A0~A11
Column Address	A0~A7, A9
AP Flag	A8

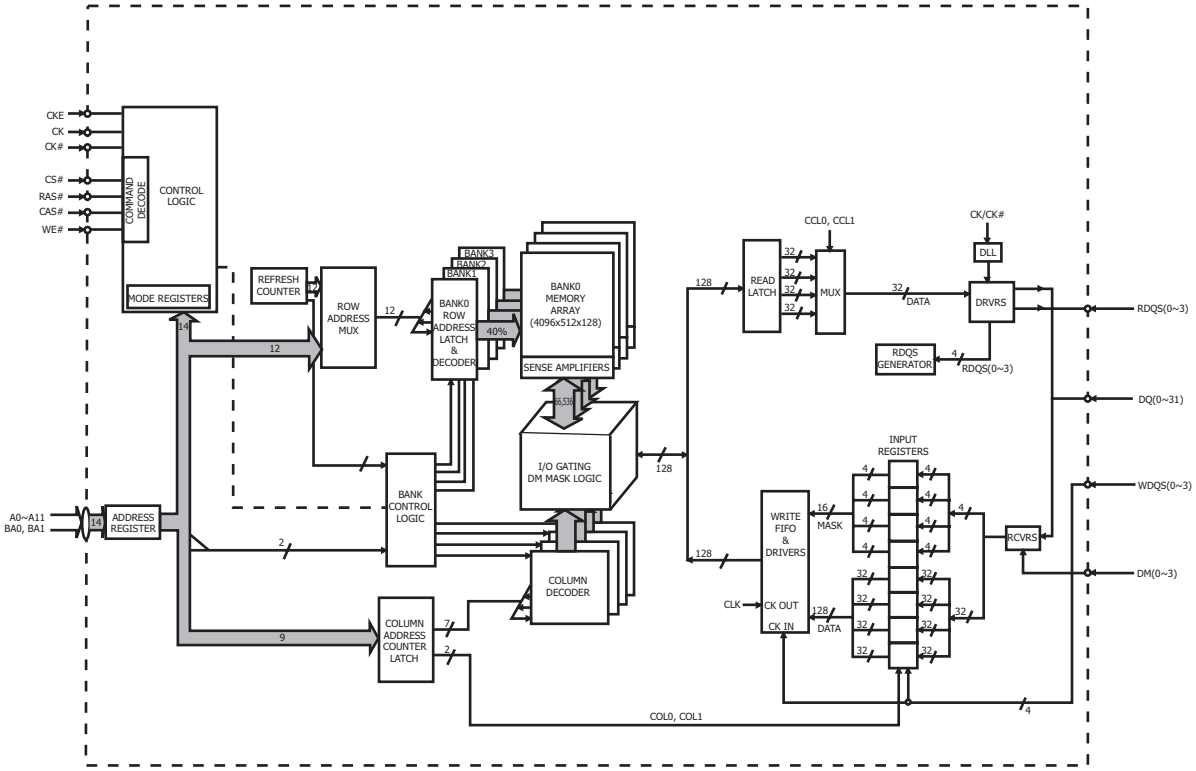
Package Top View
(see the balls through the package)



Ball Location
- ● Ball existing
- ◍ Thermal Ball or No Ball (VSS thermal balls or NC)
- ○ Depopulated Ball

FUNCTIONAL BLOCK DIAGRAM

4Banks x 2Mbit x 32 I/O Double Data Rate Synchronous DRAM



BALLOUT DESCRIPTIONS

FBGA BALLOUT	SYMBOL	TYPE	DESCRIPTION
N7, N8	CK, CK#	Input	Clock: CK and Ck# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
M7	CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations(all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, CKE and RES are disabled during POWER-DOWN. Input buffers (excluding CKE and RES) are disabled during SELF REFRESH.
M10	CS#	Input	Chip Select: CS# enables (registered LOW)and disables (registered HIGH) the command decoder. All commands (except DATA TERMINATOR DISABLE) are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
M5, N6, N9	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE#(along with CS#) define the command being entered.
C3, J12, J3, C12	DM0-DM3	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on rising and falling edges of WDQS.
N5, N10	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
N2:3, M3, L3, L12, M12, N12:13, N11, M11, M4, N4	A0-A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit(A8) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 LOW, bank selected by BA0, BA1) or all banks (A8 HIGH). The address inputs also provide the opcode during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
B7, C6, B6, B5, C2, D3, D2, E2	DQ0-7	I/O	Data Input/Output:
L13, K12:13, J13, G13:12, F13:12	DQ8-15	I/O	Data Input/Output:
F3:2, G3:2, J2, K2:3, L2	DQ16-23	I/O	Data Input/Output:
E13, D13:12, C13, B10:9, C9, B8	DQ24-31	I/O	Data Input/Output:
B3, H12, H3, B12	RDQS0-3	Output	READ Data Strobe: Output with read data. RDQS is edge-aligned with read data. It is used to capture data.
B2, H13, H2, B13	WDQS0-3	Input	WRITE Data strobe: Input with write data. WDQS is center aligned to the input data.

BALLOUT DESCRIPTIONS -CONTINUE

FBGA Ball Out	SYMBOL	TYPE	DESCRIPTION
C4:5 C7:8, C10:11 F4, F11, G4, G11, H4, H11 J4, J11, K4, K11	V_{DDQ}	Supply	DQ Power Supply: +2.0V ± 0.100V. Isolated on the die for improved noise immunity.
B4, B11, D4:6, D9:11, E6, E9, F5, F10, G5, G10, H5, H10, J5, J10, K5, K10	V_{SSQ}	Supply	DQ Ground: Isolated on the die for improved noise immunity.
D7:8, E4, E11, L4, L11	V_{DD}	Supply	Power Supply: +2.0V ± 0.100V
E5, E7:8, E10, K6:9, L5, L10	V_{SS}	Supply	Ground
M2, M13	V_{REF}	Supply	Reference voltage.
M9	ZQ	REFERENCE	External reference pin for Auto-calibration.
M6	RES	Input	Reset pin. The RES pin is a VDDQ CMOS input.
F6:9, G6:9, H6:9, J6:9	VSStherm	NC, Supply	NC or Could be used as VSS for thermal purpose
E3, E12, L6, L9, M8	RFU		Reserved for Future Use

NOTE: 1. NC pins not listed may also be reserved for other uses now or in the future. This table simply defines specific NC pins deemed to be of importance.

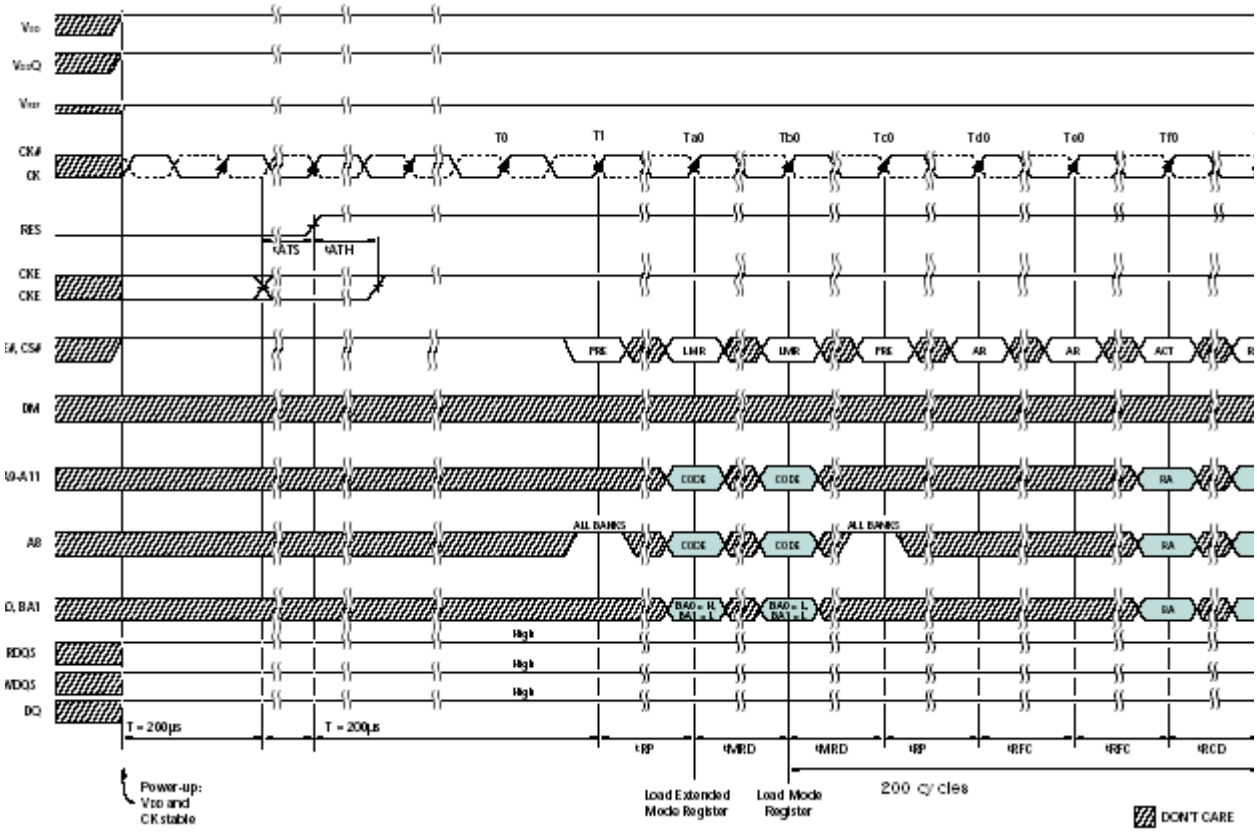
Initialization and Power Up

GDDR3 SGRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must be first applied to VDD and VDDQ simul-taneously, and then to VREF. VREF can be applied any time after VDDQ. Once power has been applied and the clocks are stable the GDDR3 device requires 200us before the RES pin transitions to high. Upon power-up and after the clock is stable, the on die termination value for the address and control pins will be set, based on the state of CKE when the RES pin transitions from LOW to HIGH. On the rising edge of RES, the CKE pin is latched to determine the on die termination value for the address and control lines. If CKE is sampled at a logic LOW then the on die termination will be set to 1/2 of ZQ and, if CKE is sampled logic HIGH then the on die termination will be set to the same value as ZQ. CKE must meet tATS and tATH on the rising of RES to set the on die termination for address and control lines. Once tATH is met, set CKE to HIGH. An additional 200us is required for the address and command on die terminations to calibrate and update.

RES must be maintained at a logic LOW-level value and CS must be maintained HIGH, during the first stage of power-up to ensure that the DQ outputs will be in a High-Z state.

After the RES pin transitions from LOW to HIGH wait until a 200us delay is satisfied. Issue DESELECT on the command bus during this time. Issue a PRECHARGE ALL command. Next a LOAD MODE REGISTER command must be issued for the extended mode register (BA1 LOW and BA0 HIGH) to activate the DLL and set operating parameters, followed by the LOAD MODE REGISTER command (BA0/BA1 both LOW) to reset the DLL and to program the rest of the operating parameters. 200 clock cycles are required between the DLL reset and any READ command to allow the DLL to lock. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be issued. Following these requirements, the GDDR3 SGRAM is ready for normal operation.



ODT Updating

The GDDR3 SGRAM uses a programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and VSSQ. The value of the resistor must be six times the desired driver impedance. For example, a 240Ω resistor is required for an output impedance of 40Ω To ensure that output impedance is one-sixth the value of RQ (within 10 percent), RQ should be in the range of 210Ω to 270Ω (35Ω - 45Ω output impedance).
CK and /CK are not internally terminated. CK and /CK will be terminated on the system module using external 1% resisters.

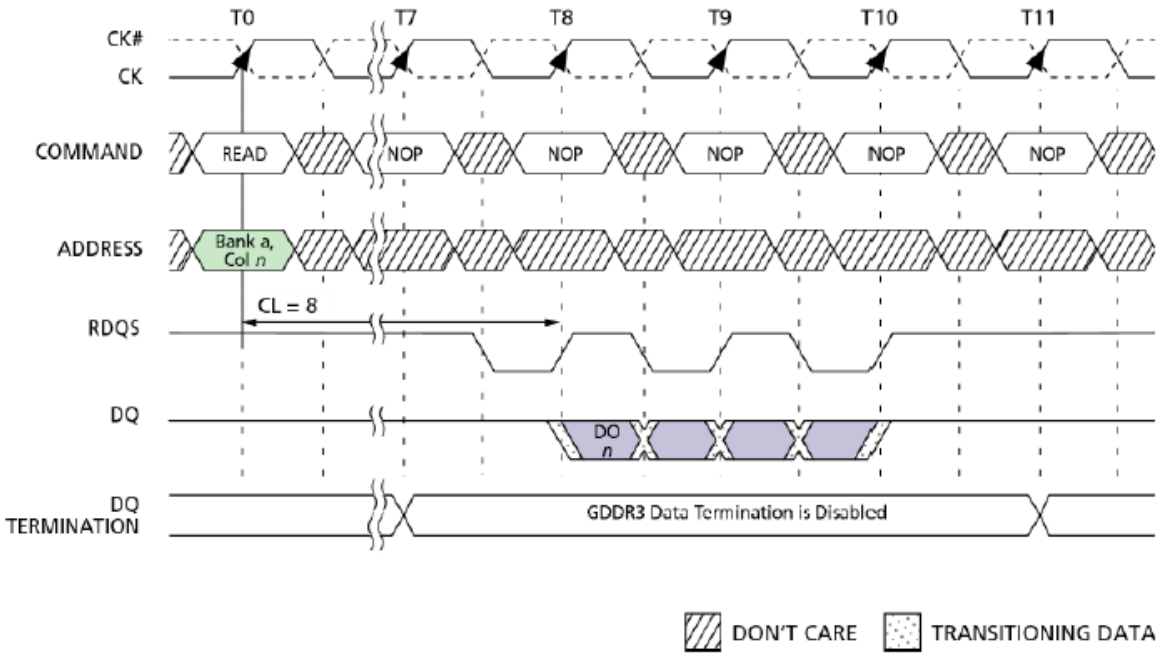
The output impedance and on die termination is updated during every AUTO REFRRESH commands to compensate for variations in supply voltage and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all datasheet timings and current specifications are met during an update.

A maximum of eight AUTO REFRESH commands can be posted to any given GDDR3 SGRAM, meaning that the maximum absolute interval between any AUTO REFRESH

command and the next AUTO REFRESH command is 9 x 7.8us (70.2us). This maximum absolute interval guarantees that the output drivers and the on die terminations of GDDR3 SGRAMs are recalibrated often enough to keep the impedance characteristics of those within the specified boundaries. During the minimum keep out time of tKO after AUTO REFRESH command, DES (i.e. /CS HIGH) should be issued on the command bus, and no activity on the address or data bus is recommended, because the signal integrity on the bus can not be guaranteed during this period.

ODT Control

Bus snooping for READ commands other than CS# is used to control the on die termination in the dual load configuration. The GDDR3 SGRAM will disable the DQ and RDQS on die termination when a READ command is detected regardless of the state of CS#. The on die termination is disabled x clocks after the READ command where x equals CL-1 and stay off for a duration of BL/2+2CK. In a two-rank system, both DRAM devices snoop the bus for READ commands to either device and both will disable the on die termination, for the DQ pins if a READ command is detected. The on die termination for all other pins on the device is always on for both a single-rank system and a dual-rank sys-



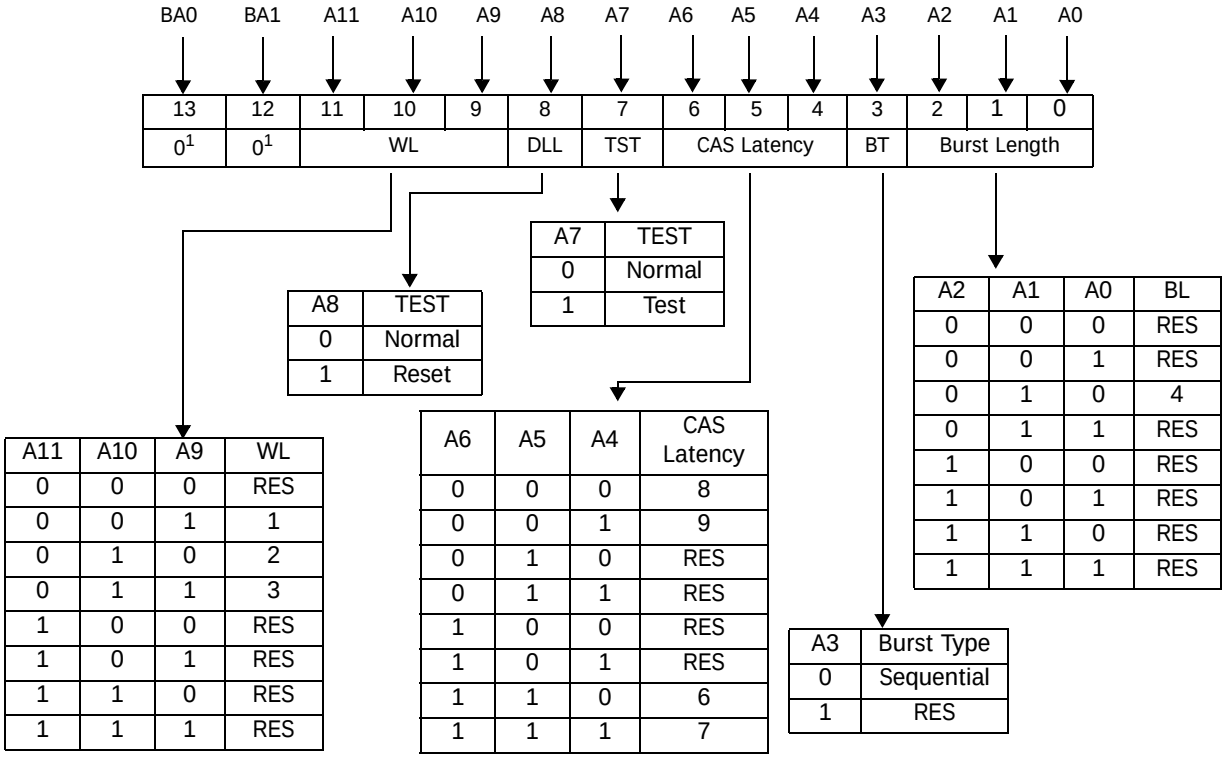
REGISTER DEFINITION

MODE REGISTER

The mode register is used to define the specific mode of operation of the GDDR3 x32. This definition includes the selection of a burst length, a burst type, a CAS latency, WRITE latency, and an operating mode, as shown in Figure 1. The mode register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential), A4-A6 specify the CAS latency,A7 specifies Test Mode, A8 specifies the DLL Reset, and A9-A11 specify the WRITE latency.



NOTE: 1. A13 and A12 (BA0 and BA1) must be “0”, “0” to select the Mode Register (vs. the Extended Mode Register)
2. RES: Reserved for future use. Set values to 0.

Figure 1: Mode Register Definition

Burst Length

Read and write accesses to the GDDR3 x32 are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ of WRITE command. Burst lengths of 4 is available.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2-Ai when the burst length is set to four (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bits are used to select the starting location within the block and only ‘00’ is allowed for GDDR3 SGRAM. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given bank must be programmed to be to the sequential mode; this is referred to as the burst type and is selected via bit A3. This device does not support the burst interleave mode.

The ordering of access within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

Table1
Burst Definition

Burst Length	Starting Column Address	Order of Accesses Within a Burst
		Type=Sequential
4	A1 A0	
	0 0	0-1-2-3

NOTE:

1. For a burst length of four, A2-A7 select the block of four burst; A0-A1 select the starting column within the block.
2. Burst 8 is not supported.

CAS Latency

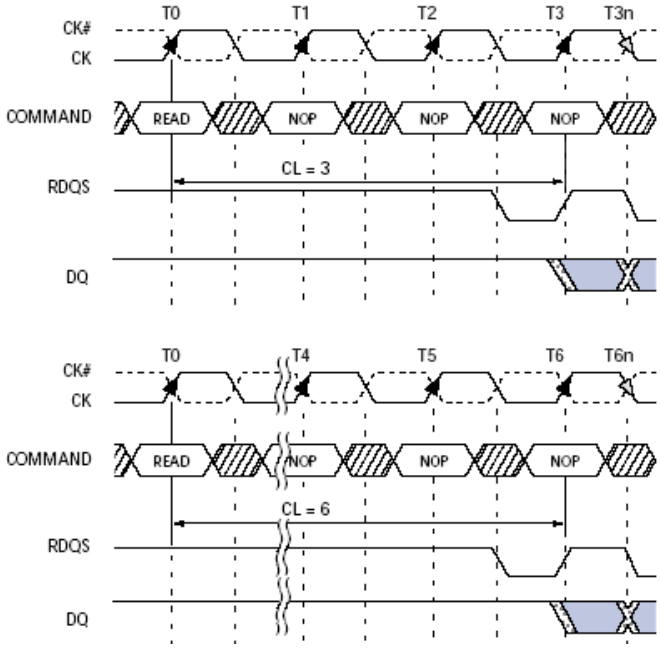
The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 3 to 9 clocks, as shown in Figure 2.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n +m. Table 2 indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Table 2: CAS Latency

	ALLOWABLE OPERATING FREQUENCY (MHz)			
SPEED	CL=9	CL=8	CL=7	CL=6
-12	800	-	-	-
-13	750	-	-	-
-14	-	700	-	-
-15	-	650	-	-
-16	-	-	600	-
-18	-	-	550	-
-2	-	-	-	500
-22	-	-	-	450



Burst Length=4 in the cases shown
shown with nominal tAC and nomial tDQSQ

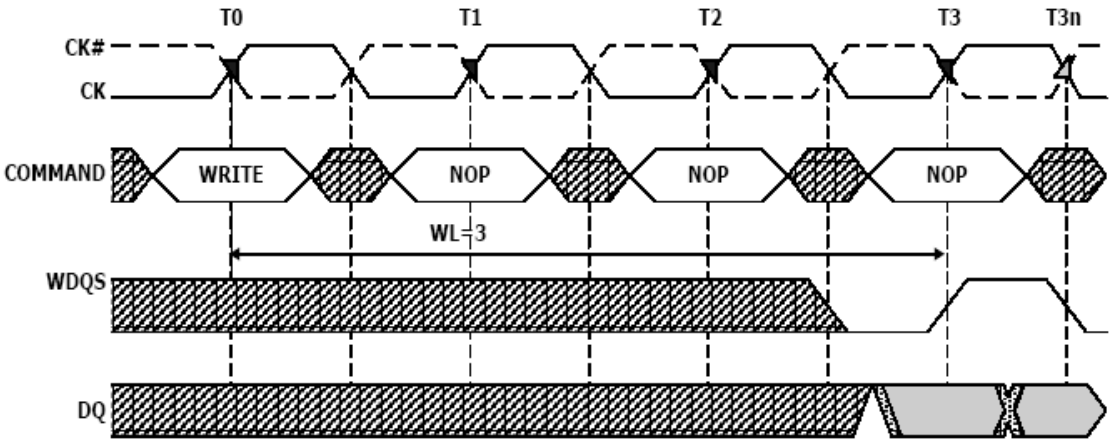
Figure 2: CAS Latency

Write Latency

The WRITE latency, WL, is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data as shown in Figure 2a. The latency can be set from 1 to 3 clock s depending on the operating frequency and desired current draw. Setting the WL to 1, 2 or 3 clocks will cause the device to enable the input receivers on all ACTIVE commands instead of the WRITE commands increasing the devices current draw.

If a WRITE command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n+m.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.



Burst Length =4 in the cases shown
shown with nominal tAC and nomial tDQSQ

Figure 2a
WRITE Latency

Test Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7 set to zero, and bits A0-A6 and A9-A11 set to the desired values. Test mode is entered by issuing a MODE REGISTER SET command with bit A7 set to one, and bits A0-A6 and A8-A11 set to the desired values. Test mode functions are specific to each Dram Manufacturer and its exact functions are hidden from the user.

DLL Reset

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A8 set to zero, and bits A0-A7 and A9-A11 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bit A8 set to one, and bits A0-A7 and A9-A11 set to the desired values.

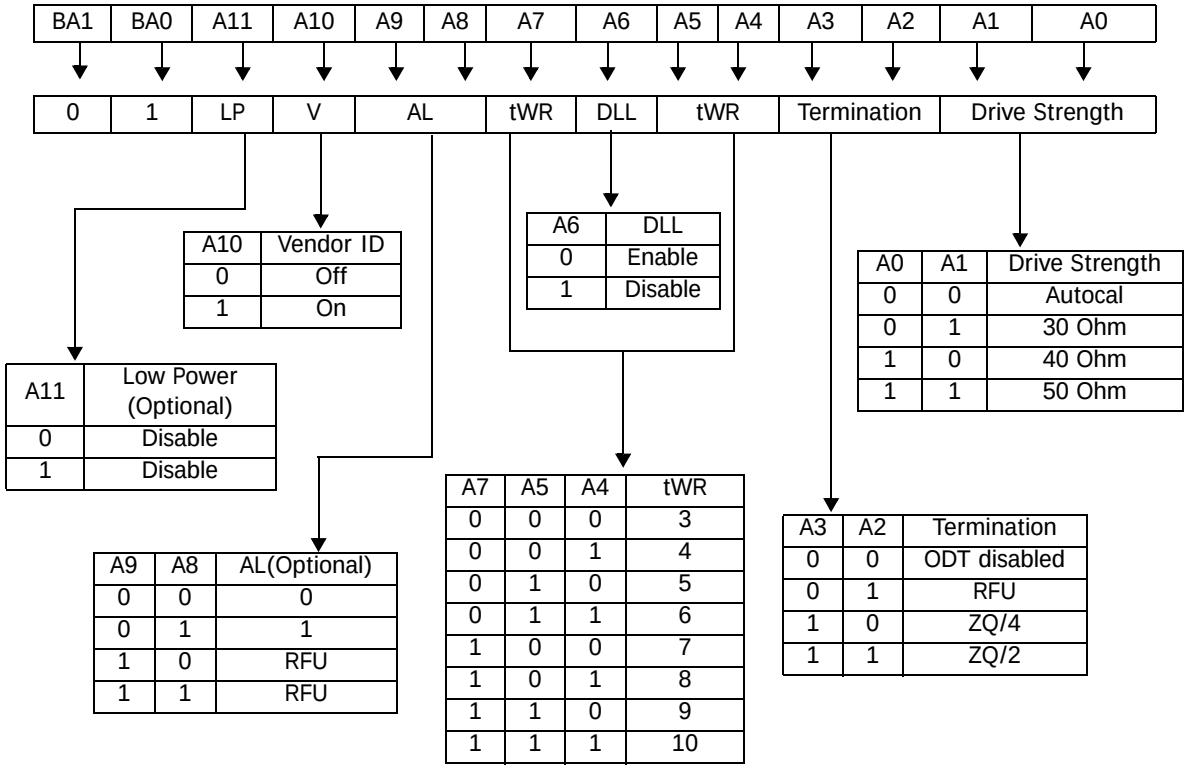
When a DLL Reset is complete the GDDR3 Dram reset bit A8 of the mode register is self clearing(i.e. automatically set to a zero. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

EXTENDED MODE REGISTER

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and tWR. These functions are controlled via the bits shown in Figure 3. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register(with BA0=1 and BA1=0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register(BA0/BA1 both LOW)to reset the DLL.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation. A LOAD MODE REGISTER command be issued to the mode register(BA0/BA1 both LOW) to reset the DLL after it has been enabled.

Figure 3
Extended Mode Register Definition



NOTE:

1. E13 and E12(BA0 and BA1) must be “1,0” to select the Extended Mode Register (vs. the base Mode Register).
2. RFU: Reserved for future use.
3. The ODT Disable function disables all terminators on the device.
4. The default setting at Power Up for A3A2 is 10 or 11
5. A11, A9A8 may be used optionally for Low Power mode, Additive Latency setting respectively. And Hynix GDDR3 has the Additive Latency implemented, but not the Low Power mode.
6. If the user activates bits in the extended mode register in an optional field, either the optional feature is activated (if option implemented in the device) or no action is taken by the device (if option not implemented).
7. The Drive Strength (A1A0) values of 30, 40 and 48 omhs are only intended as targets under typical conditions. In addition when any of these values are selected the termination values may scale with the selected impedence.
8. WR (write recovery time for autoprecharge) in clock cycles is calculated by dividing tWR (in ns) by tCK(in ns) and rounding up to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.)
Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

tWR

The value of tWR in the AC parametrics table on page 44-45 of this specification is loaded into register bits 7, 5 and 4. As described in the note, correct value for WR must be programmed by the user to guarantee proper operation.

Additive Latency

The Additive Latency function, AL, is used to optimize the comman bus efficiency.

The AL value is used to determine the number of clock cycles that is to be added to CL after CAS is captured by the rising edge of CK. Thus the total Read Latency is determined by adding CL and AL. The Additive Latency function is not a required feature but is implemented in Hynix GDDR3 SGRAM.

Data Termination

The Data Termination, DT, is used to determine the value of the internal data termination resisters.

The GDDR3 SGRAM supports 1/4 ZQ and 1/2 ZQ termination. When the termination is disabled both the address/command and data termination is disabled. Termination may be disabled for testing and other purposes.

Data Driver Impedence

The Data Driver Impedence, DZ, is used to determine the value of the data drivers impedence.

When autocalibration is used the data driver impedence is set to 1/6 ZQ and it's tolerance is +/- 10%. When any other value is selected the target impedence is set nominaly to the selected impedence. However, the accuracy is now determined by the device's specific process corner, applied voltage and operating tempurature.

Manufacturers Vendor Code and Revision Identification

The Manufacturers Vendor Code, V, is selected by issuing an EXTENDED MODE REGISTER SET command with bits A10 set to one, and bits A0-A9 and A11 set to the desired values.

When the V function is enabled the GDDR3 SGRAM will provide its manufacturers vendor code on DQ[3:0] and revision idenfication on DQ[7:4]. The code will be driven onto the DQ bus a mimimum of “0” to a maximum of CL+10ns after the EMRS that set A10 to 1. The DQ bus will be continued to be driven until a mimimum of “0” to a maximum of CL+10ns after a EMRS write sets A10 back to 0.

Manufacturer	DQ[3:0]
Reserved	0
Samsung	1
Infineon	2
Elpida	3
Etrom	4
Nanya	5
Hynix	6
Mosel	7
Winbond	8
ESMT	9
Reserved	A
Reserved	B
Reserved	C
Reserved	D
Reserved	E
Micron	F

Commands

Truth Table 1 provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/next state imformation.

TRUTH TABLE1-COMMANDS

(Note: 1)

NAME(FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT(NOP)	H	X	X	X	X	8
NO OPERATION(NOP)	L	H	H	H	X	8
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6,7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2
DATA TERMINATOR DISABLE	X	H	L	H	x	9, 11

TRUTH TABLE 1A-DM OPERATION

NAME (FUNCTION)	DM	DQS	NOTES
Write Enable	L	Valid	10
Write Inhibit	H	X	10

NOTES:

1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0-BA1 select either the mode register or the extended mode register(BA0=, BA1=0 select the mode register; BA0=1, BA1=0 select extended mode register; other combinations of BA0-BA1 are reserved). A0-A11 provide the opcode to be written to the selected mode register.
3. BA0-BA1 provide bank address and A0-A11 provide row address.
4. BA0-BA1 provide bank address; A0-A7 and A9 provide column address; A8 HIGH enables the auto precharge feature (nonpersistent), and A8 LOW disables the auto precharge feature.
5. A8 LOW: BA0-BA1 determine which bank is precharged.
   A8 HIGH: all banks are precharged and BA0-BA1 are “Don’t Care” except for CKE.
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. DESELECT and NOP are functionally interchangeable.
9. Cannot be in powerdown or self-refresh state
10. Used to mask write data; provided coincident with the corresponding data.
11. During a READ command a DATA TERMINATOR DISABLE command is executed simultaneously

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR x32. The GDDR3x32 is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected GDDR3x32 to perform a NOP (CS# LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0-A11. See mode register descriptions in the Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle,and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open(or activate) a row in a particular bank for a subsequent access.
The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A7, A9 selects the starting column location. The value on input A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A7, A9 selects the starting column location. The value on input A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE ommand is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been prechared, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank(idle state), or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A8 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. Auto precharge ensures that the precharge is

initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating $^{t}RAS_{min}$, as described for each burst type in the Operation section of this data sheet. The user must not issue another command to the same bank until the precharge time (^{t}RP)is completed.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the GDDR3 DRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 256Mb x32 GDDR3 x32 requires AUTO REFRESH cycles at an average interval of 7.8us (maximum).

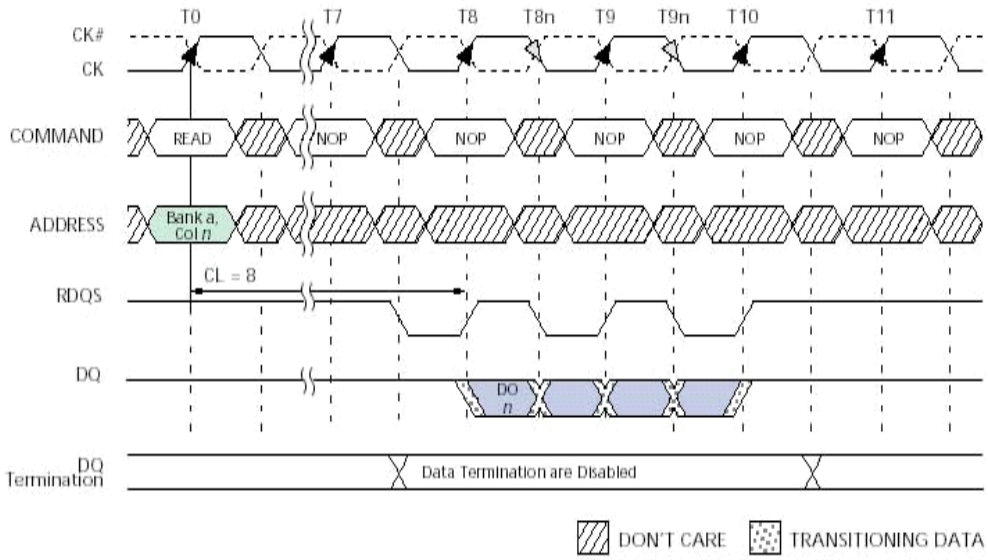
A maximum of eight AUTO REFRESH commands can be posted to any given GDDR3 x32, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 x7.8us (70.2us). This maximum absolute interval is to allow GDDR3 x32 output drivers and internal terminators to automatically recalibrate compensating for voltage and temperature changes. In a dual rank system the User must wait 10ns before issue commands to the opposite rank that is being refreshed. This is done to allow time for the termination update to occur.

DATA TERMINATOR DISABLE
(BUS SNOOPING FOR READ COMMANDS)

The DATA TERMINATOR DISABLE COMMAND is detected by the device by snooping the bus for READ commands excluding CS#. The GDDR3 Dram will disable its Data terminators when a Read command is detected. The terminators are disable starting at CL-1 Clocks after the READ command is detected and the duration is BL/2+2 CLOCKS. In a two rank system both dram devices will snoop the bus for read commands to either device and both will disable their terminators if a READ command is detected. The command and address terminators are always enabled. See figure 3a for an example of when the data terminators are disabled during a Read Command.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the GDDR3 x32, even if the rest of the system is powered down. When in the self refresh mode, the GDDR3 x32 retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELF REFRESH.
The active termination is also disabled upon entering Self Refresh and enabled upon exiting Self Refresh. (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are "Don't Care" during SELF REFRESH. The procedure for exiting self refresh requires a sequence of commands.
First, CK and CK# must be stable prior to CKE going back HIGH. Once CKE is HIGH, the GDDR3x32 must have NOP commands issued for $^{t}XSRD$ because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and output calibration is to apply NOPs for 200 clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.



NOTE:
1. DO n=data-out from column n.
2. Burst length=4.
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Shown with nominal ^{t}AC, and ^{t}DQSQ.
5. RDQS will start driving high 1/2 clock cycle prior to the first falling edge.
6. The Data Terminators are disabled starting at CL-1 and the duration is BL/2+2.
7. The Read command excludes CS#. Reads to either rank disable both ranks terminators

Figure 3a
Example: Data Termination Disable
During a Read Command

Operations

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the GDDR3 DRAM, a row in that bank must be "opened".

This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 4. After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 16ns with a 450MHz clock (2.2ns period) results in 7.2 clocks rounded to 8. This is reflected in Figure 5, which covers any case where $7 < {}^{t}RCD(MIN)/{}^{t}CK \leq 8$. (Figure 5 also shows the same case for ^{t}RCD; the same procedure is used to convert other specification limits from time units to clock cycles).

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

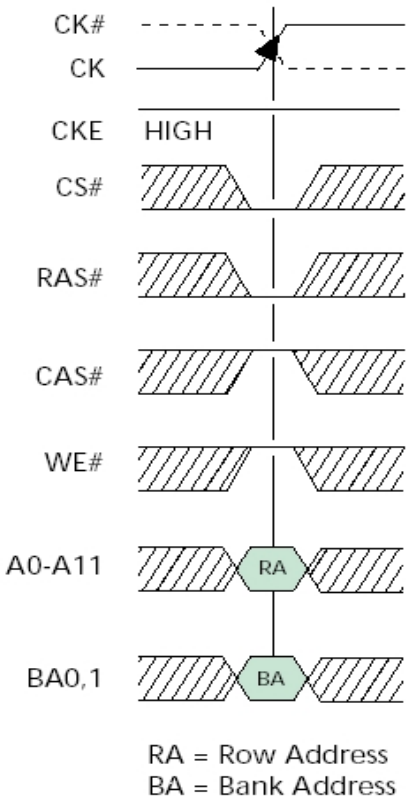


Figure 4
Activating a Specific Row in a Specific Bank

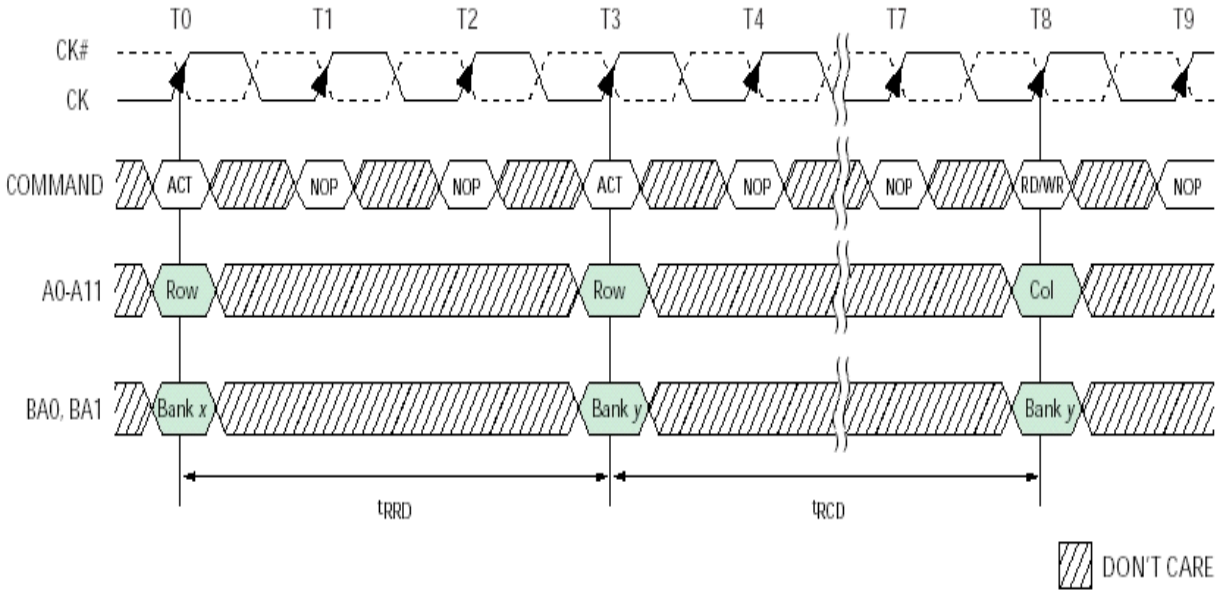


Figure 5
Example: Meeting ^{t}RCD

READ Timing

READ burst is initiated with a READ command.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after tRAS min has been met.

During READ bursts, the first valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative RDQS edges. The GDDR3 SGRAM drives the output data edge aligned to RDQS. And all outputs, i.e. DQs and RDQS, are also edge aligned to the clock.
Prior to the first valid RDQS rising edge, a cycle is driven and specified as the READ preamble. The preamble consists of a half cycle High followed by a half cycle Low driven by the GDDR3 SGRAM. The cycle on RDQS consisting of a half cycle Low coincident with the last data-out element followed by a half cycle High is known as the read postamble, and it will be driven by the SGRAM. The SGRAM toggles RDQS only when it is driving valid data out onto the bus.

Upon completion of a burst, assuming no other command has been initiated; the DQs and RDQS will go to be in Hi-Z state. VDD do to the on die termination. long as the bus turn around time is met. READ data cannot be terminated or truncated.

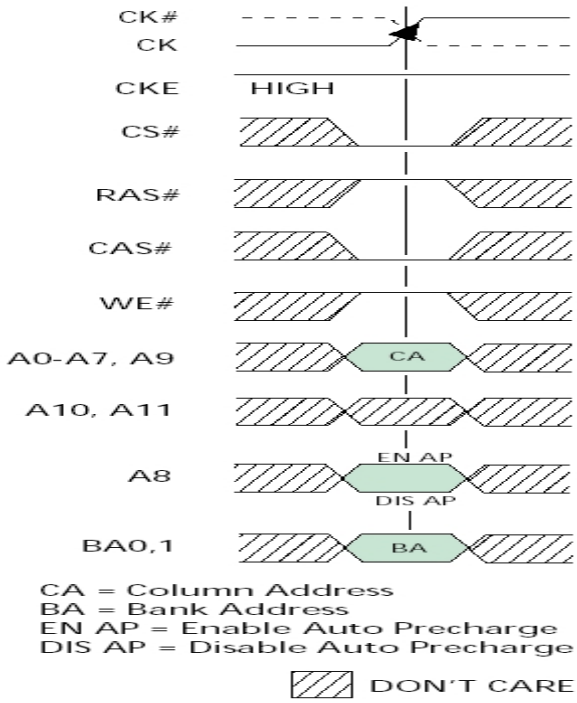
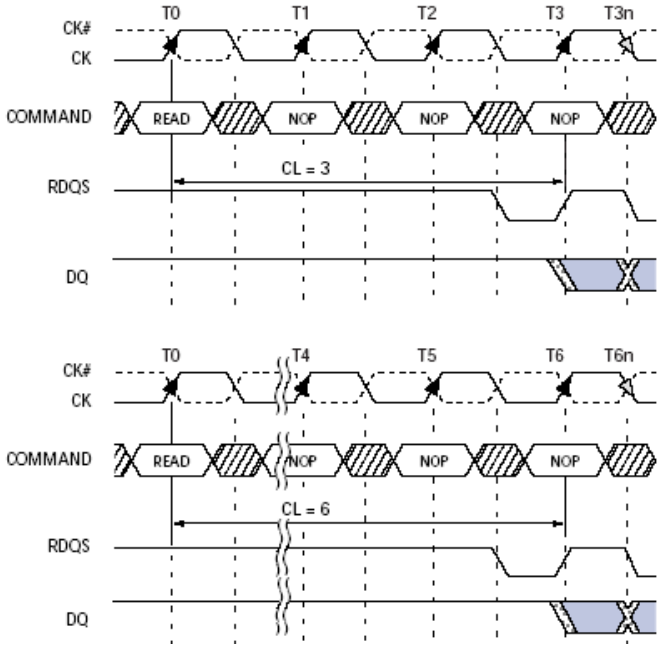


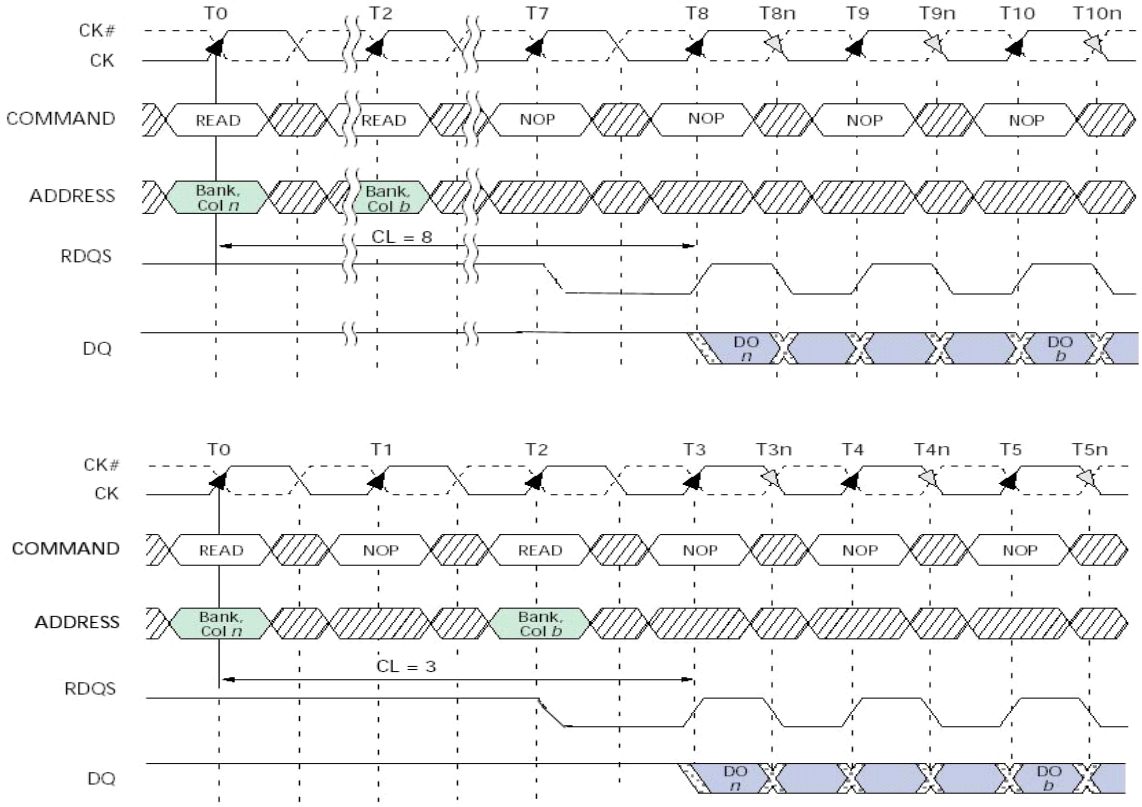
Figure 6
READ Command



NOTE:

1. DO n=data-out from column n.
2. Burst length=4.
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Shown with nominal ^{t}AC, and ^{t}DQSQ
5. RDQS will start driving high 1/2 clock cycle prior to the first falling edge.

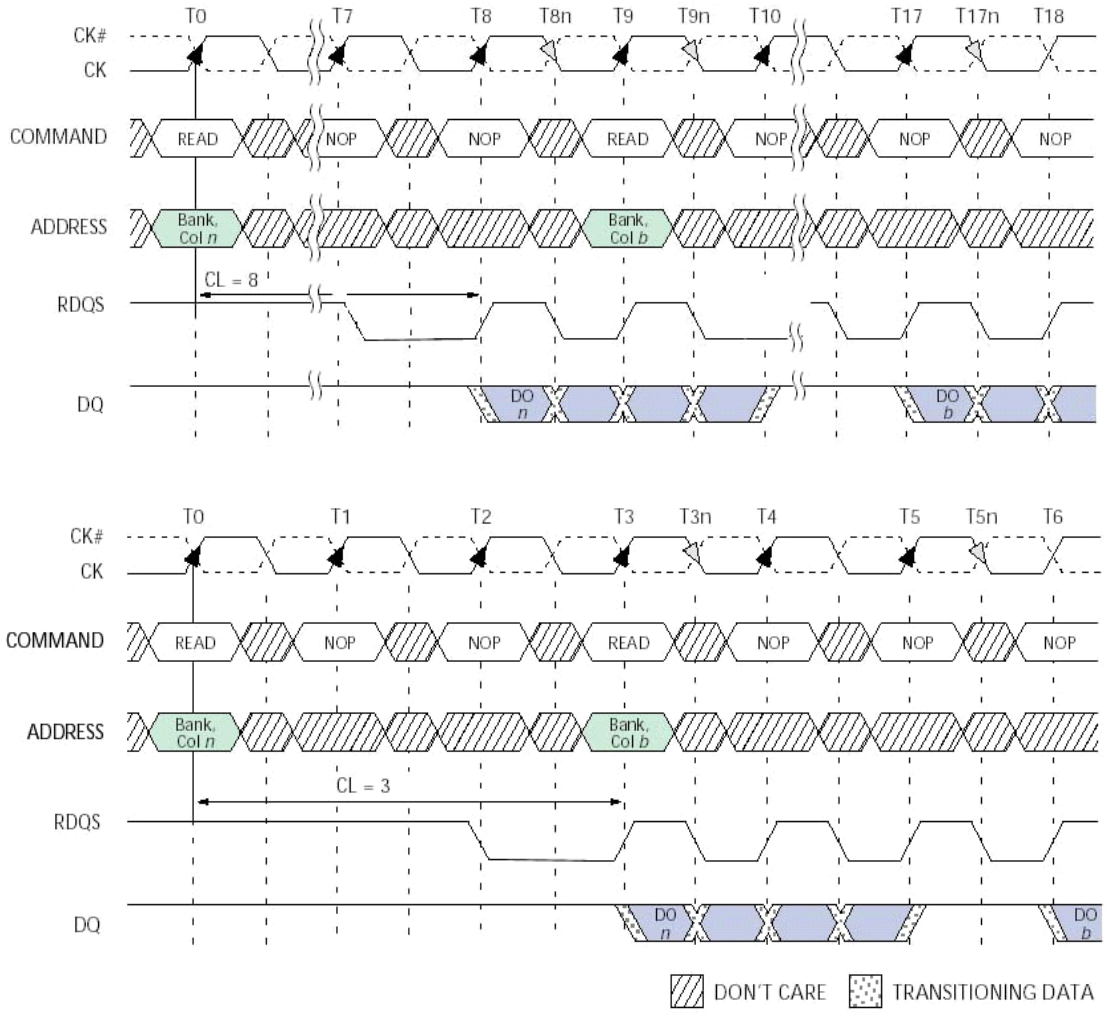
Figure 7
READ Burst



NOTE:

1. DO n (or b)=data-out from column n(or column b).
2. Burst length=4
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Three subsequent elements of data-out appear in the programmed order following DO b.
5. Shown with nominal ^{t}AC, and ^{t}DQSQ.
6. Example applies only when READ commands are issued to same device.
7. RDQS will start driving high one half clock cycle prior to the first falling edge of RDQS.

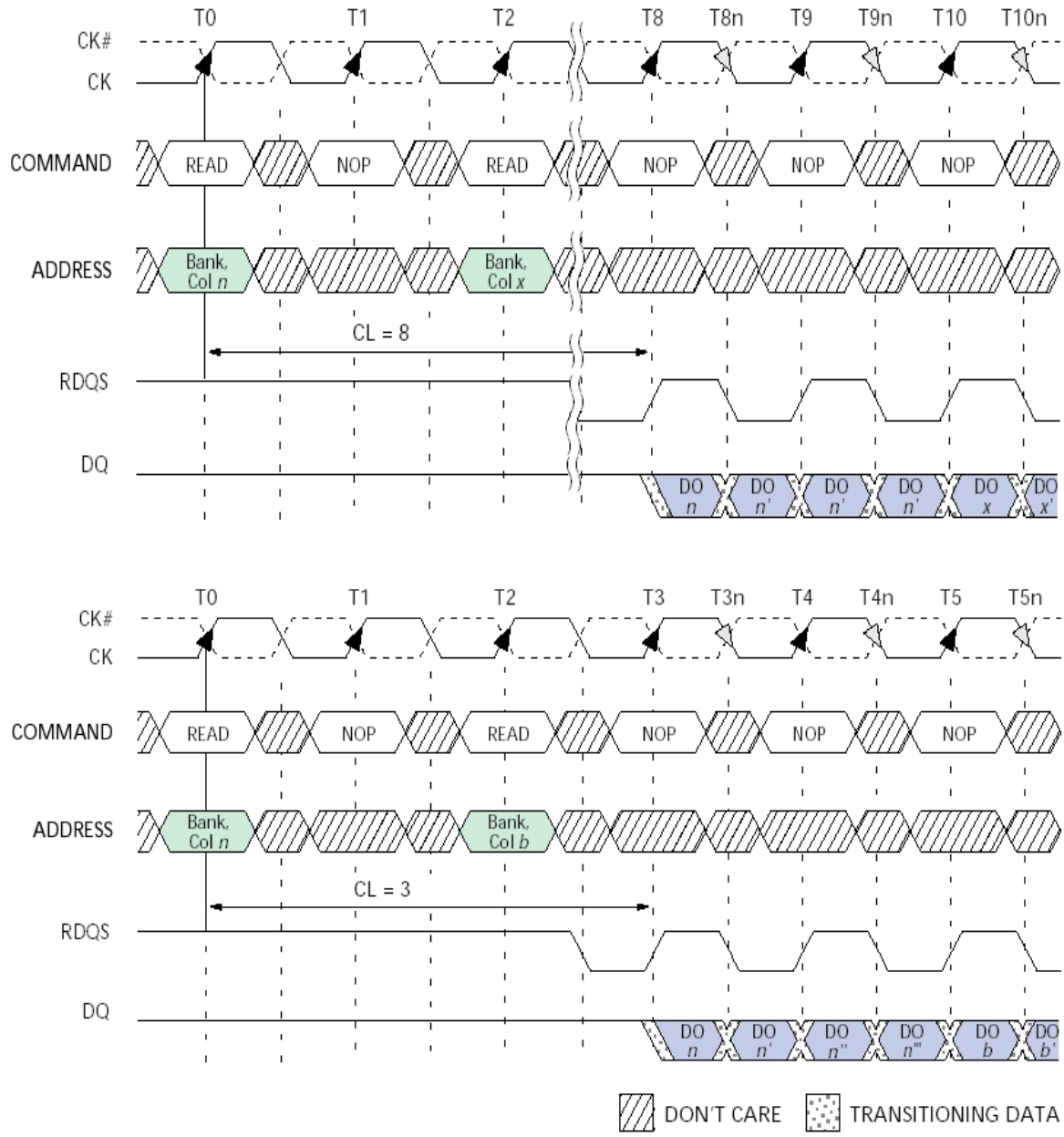
Figure 8
Consecutive READ Bursts



NOTE:

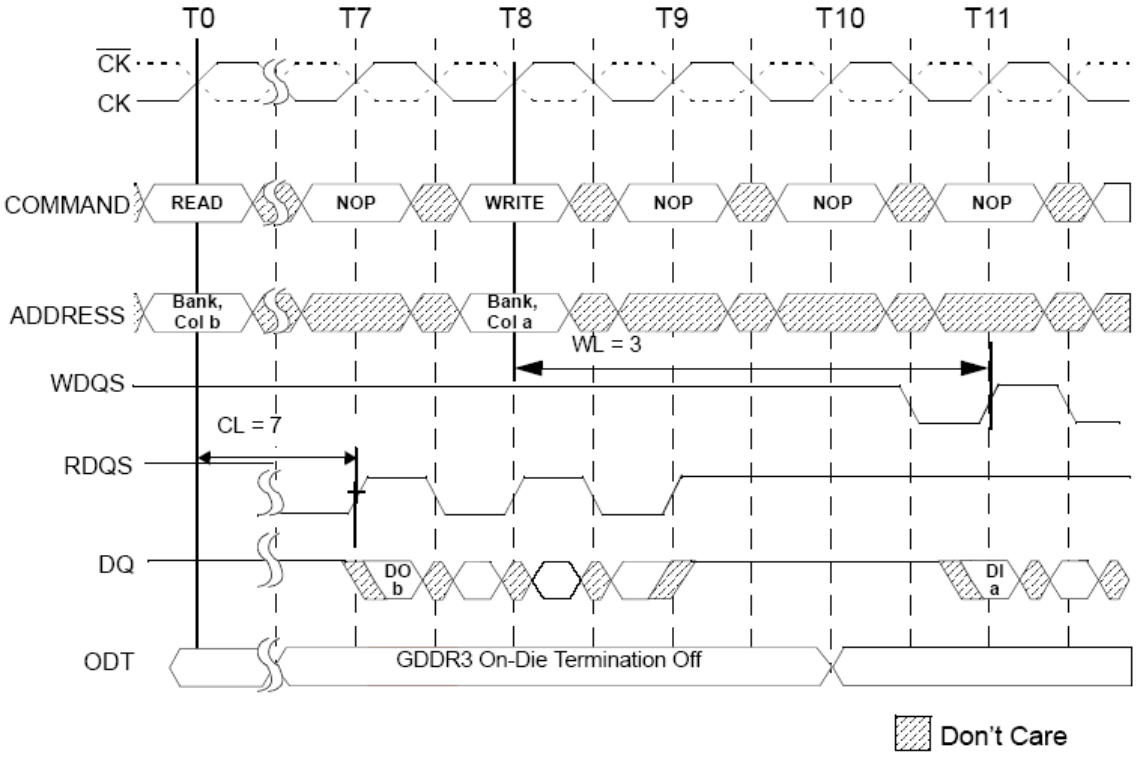
1. DO n (OR B)=DATA-OUT FROM COLUMN N(OR COLUMN B).
2. Burst length=4
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Three subsequent elements of data-out appear in the programmed order following DO b.
5. Shown with nominal ^{t}AC, and ^{t}DQSQ.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

Figure 9
Nonconsecutive READ Bursts



NOTE:
1. DO n (or x or b or g)= data-out from column n(or column X or column b or column g).
2. Burst length=4
3. n' of x' or b' or g' indicates the next data-out following DO n or DO x or DO b or DO g, respectively.
4. READs are to an active row in any bank.
5. Shown with nominal ^{t}AC , and ^{t}DQSQ.
6. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

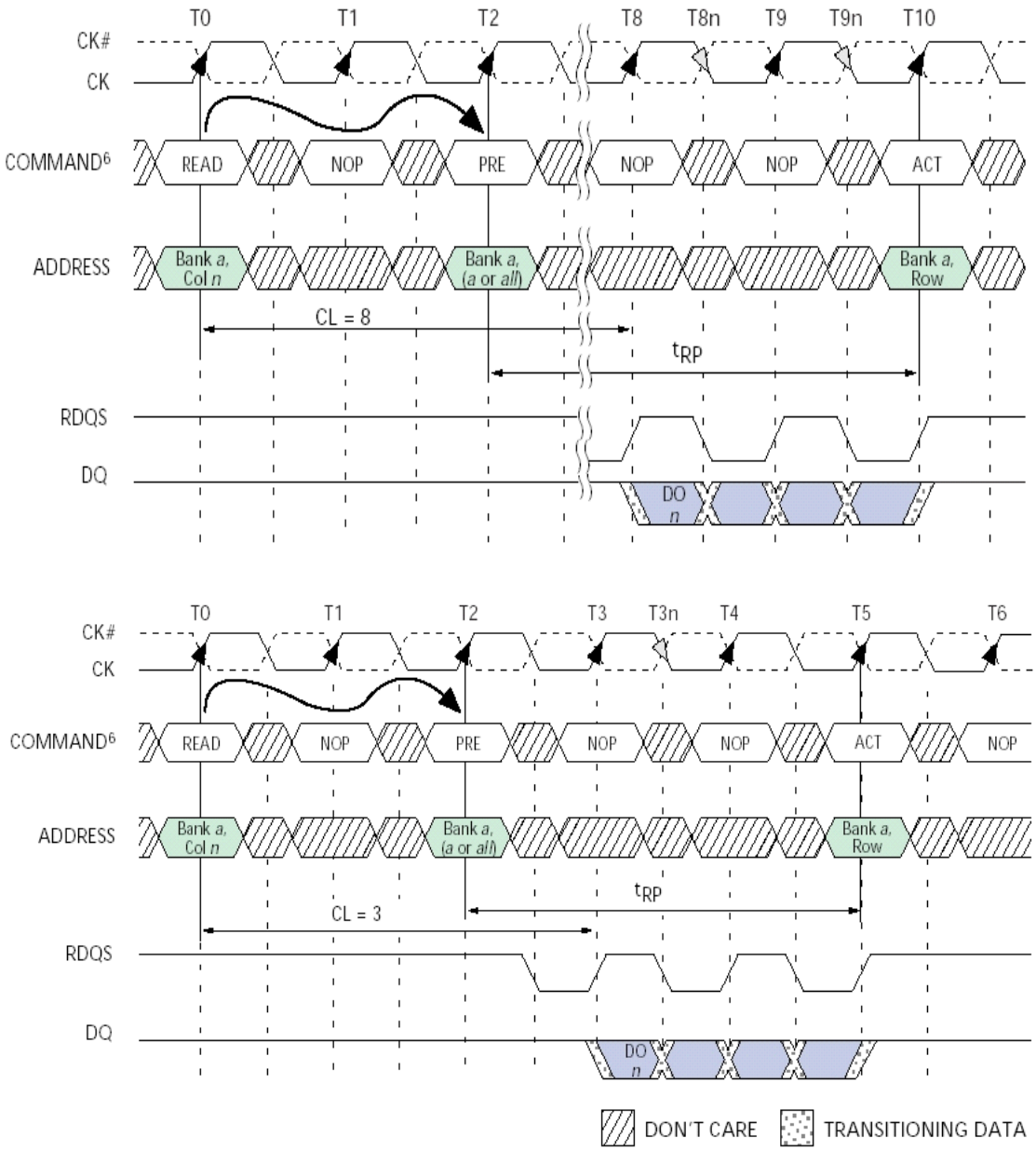
Figure10
Random READ Accesses



NOTE:

1. Write data can not be driven onto the DQ bus for 2 clock cycles after the READ data is off the bus.
2. The timing diagram covers a READ to a WRITE command from different banks on the same part or the same row in the same bank.

Figure 12
READ to WRITE



NOTE:

1. DO n=data-out from column n.
2. Burst length=4
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Shown with nominal ^{t}AC, and ^{t}DQSQ.
5. READ to PRECHARGE equals two clocks, which allows two data pairs of data-out.
6. PRE-PRECHARGE command; ACT=ACTIVE command.
7. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS

Figure 13
READ to PRECHARGE

WRITE Timing

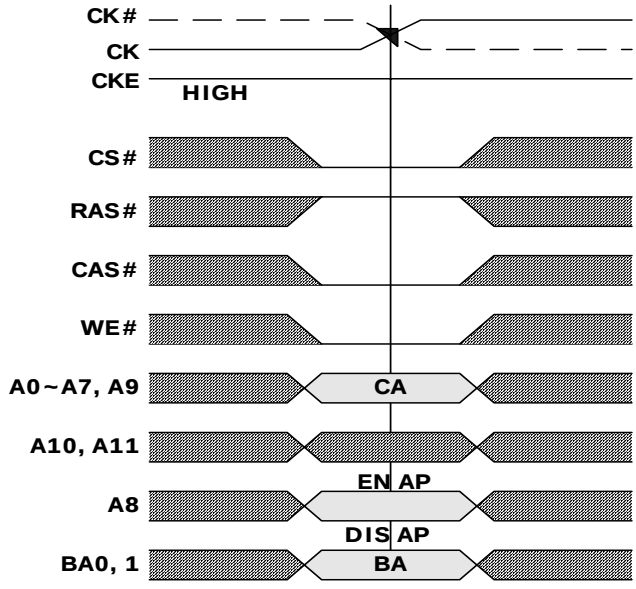
WRITE burst is initiated with a WRITE command.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that burst access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after tRAS min has been met.

During WRITE bursts, the first valid data-in element will be registered on the rising edge of WDQS following the write latency set in the mode register and subsequent data elements will be registered on successive edges of WDQS. Prior to the first valid WDQS rising edge, a cycle is needed and specified as the WRITE Preamble. The preamble consists of a half cycle High followed by a half cycle Low driven by the controller. The cycle on WDQS following the last data-in element is known as the write postamble and must be driven High by the controller, it can not be left to float High using the on die termination. The WDQS should only toggle on data transfers.

The time between the WRITE command and the first valid rising edge of WDQS (tDQSS) is specified relative to the write latency (WL - 0.25CK and WL + 0.25CK). All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., tDQSS [MIN] and tDQSS [MAX]) might not be intuitive, they have also been included. Upon completion of a burst, assuming no other command has been initiated, the DQs should remainHi-Z and any additional input data will be ignored.

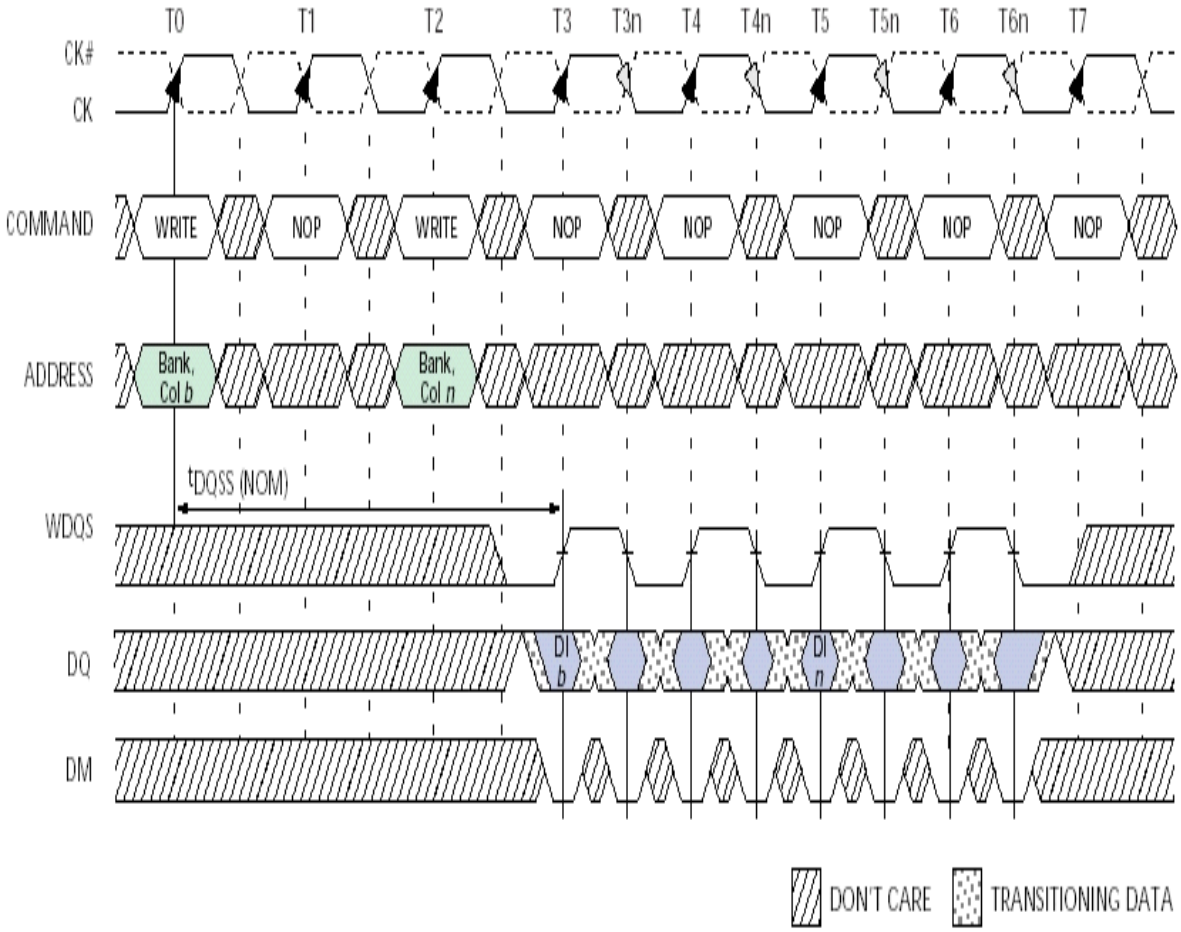
Data for any WRITE burst may not be truncated with any subsequent command.
A subsequent WRITE command can be issued on any positive edge of clock following the previous WRITE command assuming the previous burst has completed. The subsequent WRITE command can be issued x cycles after the previous WRITE command, where x equals the number of desired nibbles x2 (nibbles are required by 4n-prefetch architecture) i.e. BL/2. A subsequent READ command can be issued once tWTR is met or a subsequent PRECHARGE command can be issued once tWR is met. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.



CA= Column Address
BA= Bank Address
EN AP= Enable Auto Precharge
DIS AP= Disable Auto Precharge

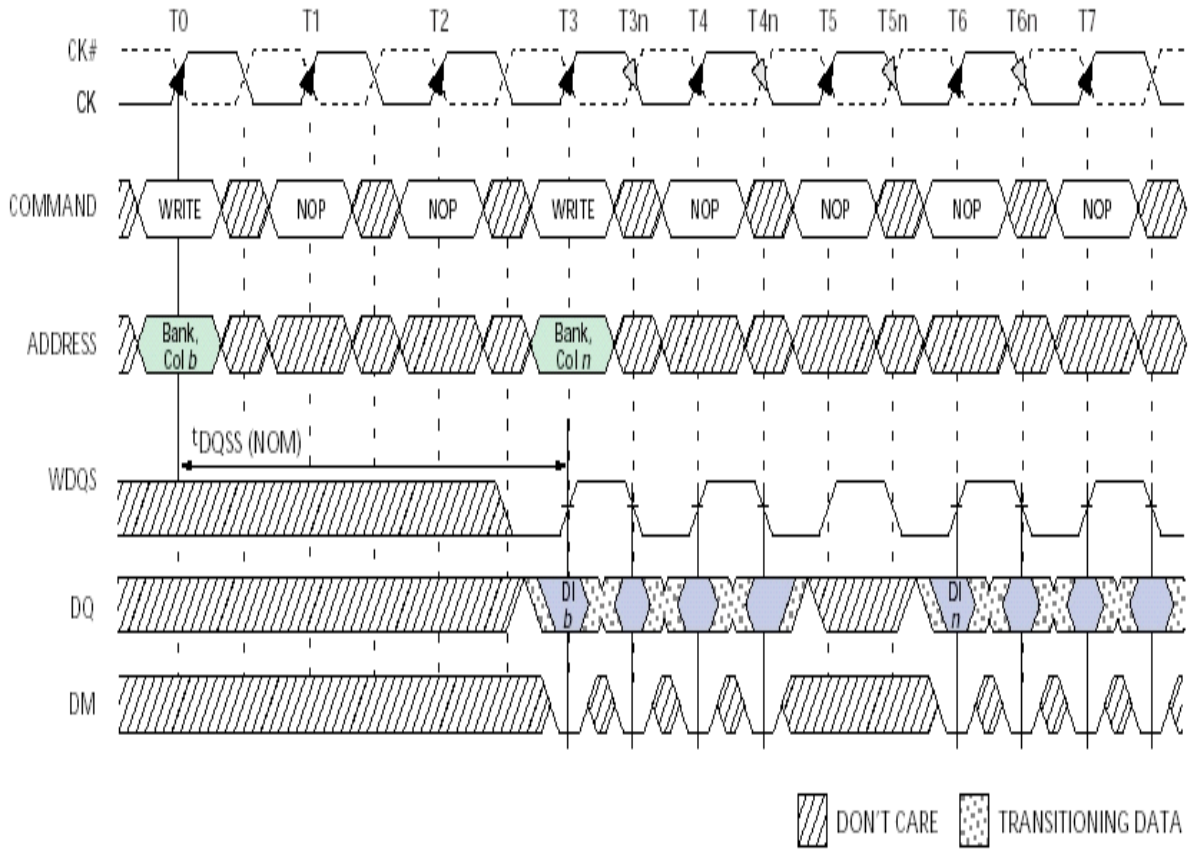
DON'T CARE

Figure 14
WRITE Command



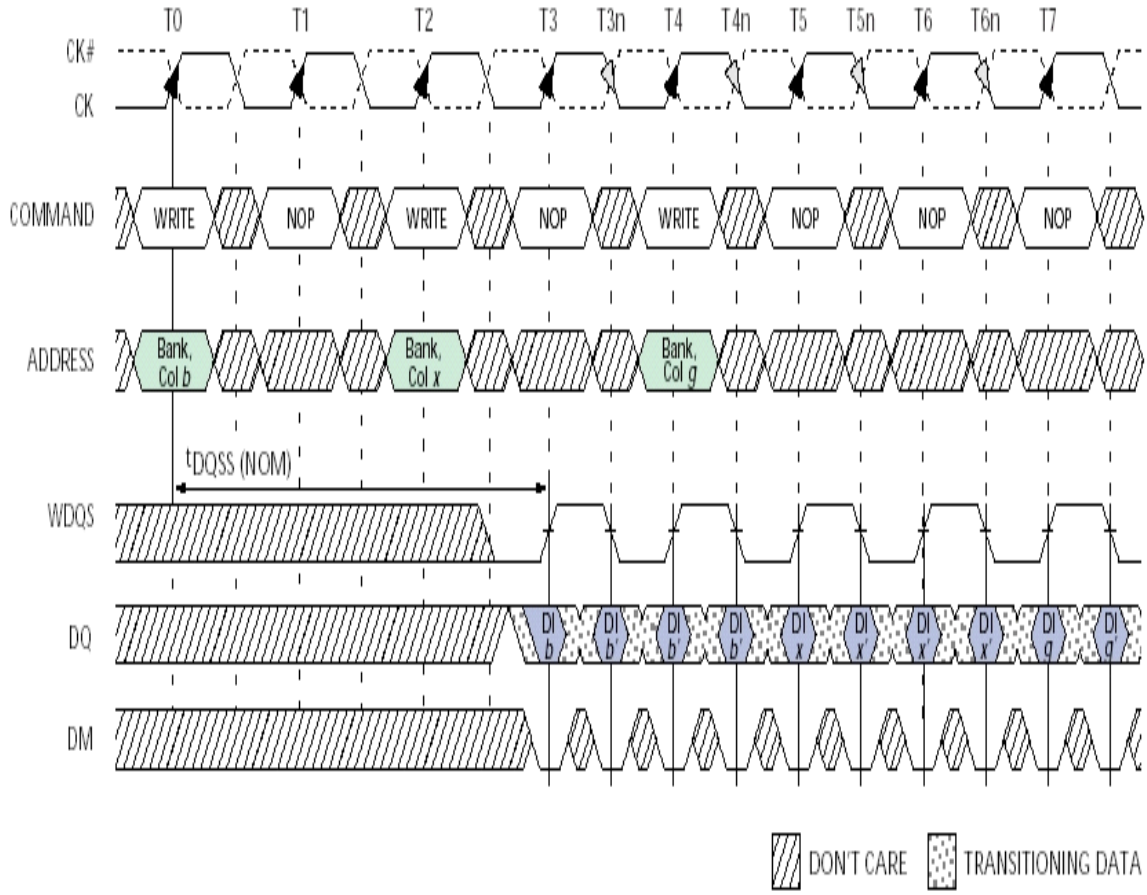
NOTE:
1. DI b, etc.=data-in for column b, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. Three subsequent elements of data-in are applied in the programmed order following DI n.
4. Burst of 4 is shown.
5. Each WRITE command may be to any bank of the same device.
6. WRITE latency is set to 3

Figure 16
Consecutive WRITE to WRITE



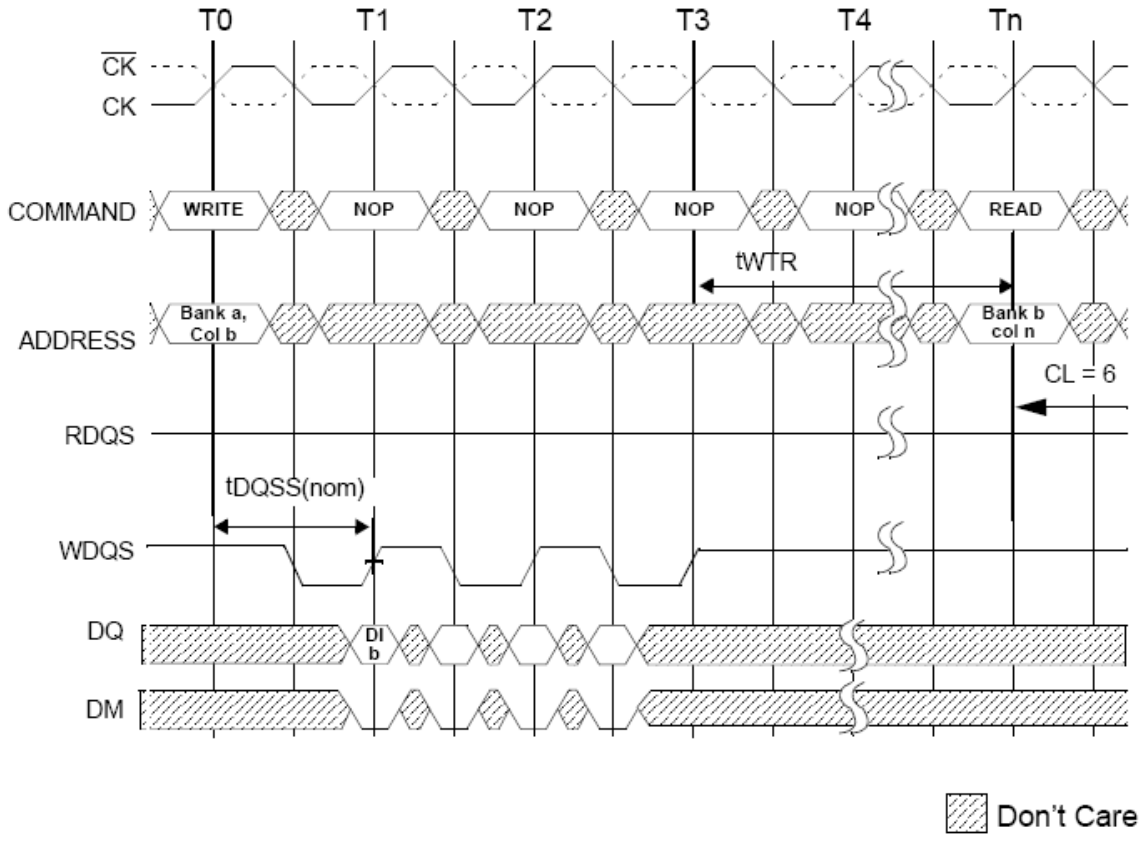
NOTE:
1. DI b, etc.=data-in for column b, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. Three subsequent elements of data-in are applied in the programmed order following DI n.
4. A Burst of 4 is shown.
5. Each WRITE command may be to any bank.
6. WRITE latency is set to 3.

Figure 17
Nonconsecutive WRITE to WRITE



NOTE:
1. DI b, etc.=data-in for column b, etc.
2. b', etc.=the next data-in following DI b, etc., according to the programmed burst order.
3. Programmed burst length=4 cases is shown.
4. Each WRITE command may be to any bank.
5. Last write command will have the rest of the nibble on T8 and T8n
6. WRITE latancy is set to 3

Figure 18
Random WRITE Cycle

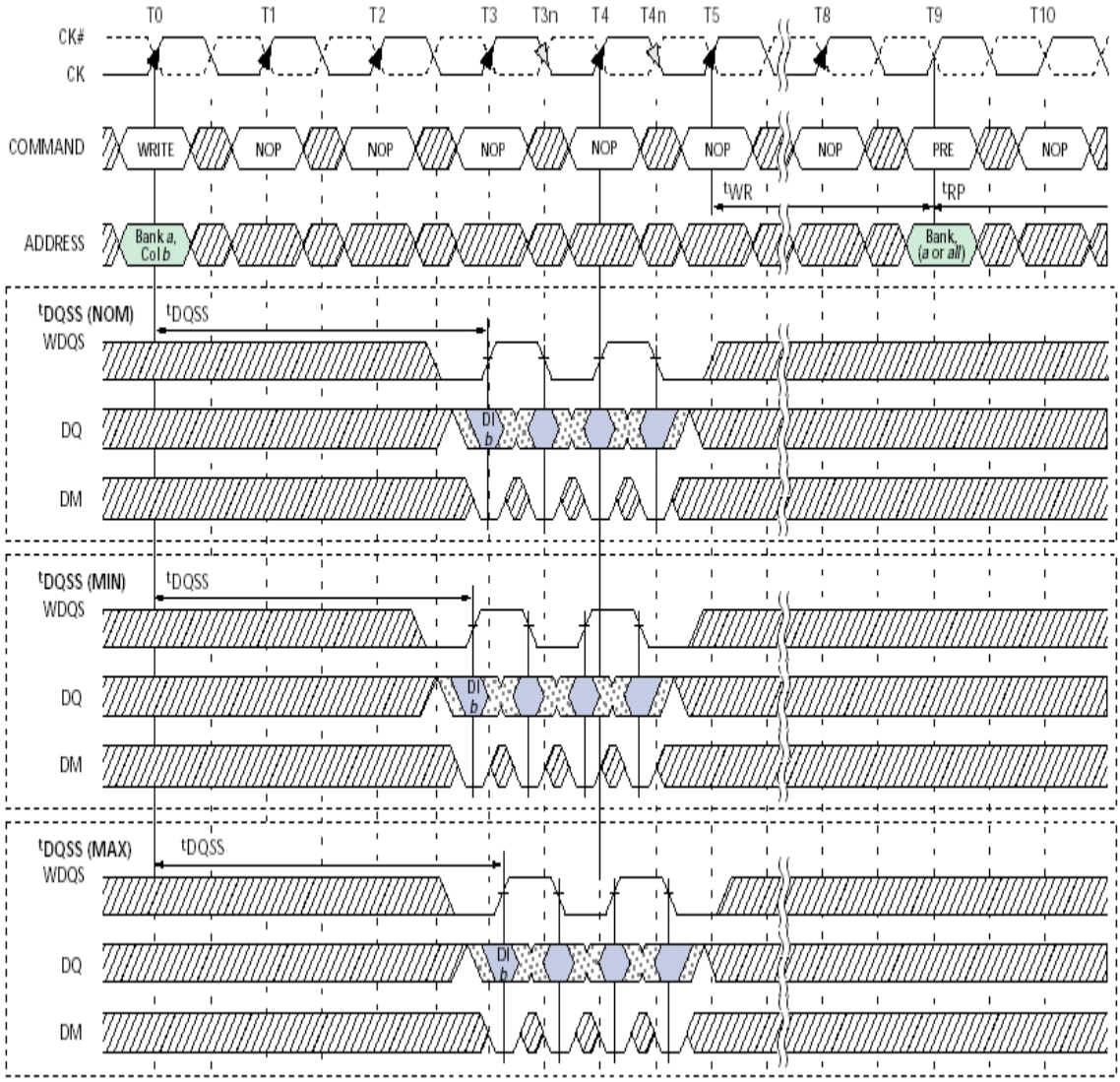


NOTE:

1. DI b = Data In for column b
2. Three subsequent elements of Data In are applied following D1 b
3. tWTR is referenced from the first positive CK edge after the last Data In
4. The READ and WRITE commands may be to any bank.
5. WRITE Latency is set to 1

Figure 19

WRITE to READ Timing



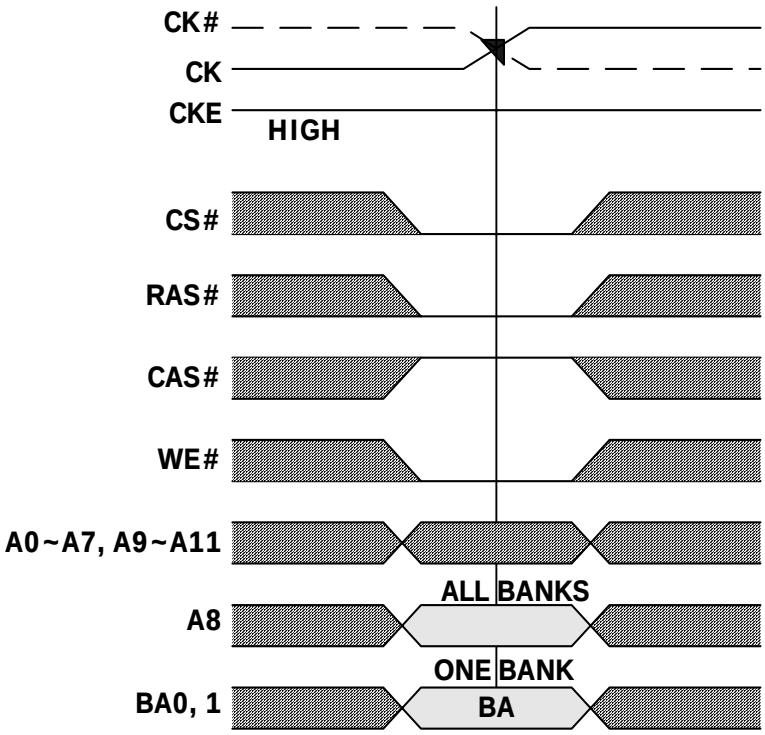
NOTE:

1. DI b, etc.=data-in for column b.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. A burst of 4 is shown.
4. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
5. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case ^{t}WTR is now required and the READ command could be applied earlier.
6. A8 is LOW with the WRITE command (auto precharge is disabled).
7. WRITE latancy is set to 3
8. The 4n prefetch architecture requires a 2 clock WRITE to READ turn around time(^{t}WTR)

Figure 22
WRITE to PRECHARGE

PRECHARGE

The PRECHARGE command(Figure 25) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.



BA= Bank Address(if A8 is LOW; otherwise "Don't Care")

Figure 25
PRECHARGE Command

POWER-DOWN (CKE NOT ACTIVE)

Unlike SDR SDRAMs, GDDR3 x32 requires CKE to be active at all times an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined when the Read Postamble is satisfied; For WRITEs, a burst completion is defined BL/2 cyles after the Write Postamble is satisfied.

Power-down (Figure 26) is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is refrered to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK# and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power-down. In that case, the DLL must be enabled and reset after exiting power-down, and 200 clock cycles must occur before a READ command can be issued. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self-refresh mode is preferred over the DLL-disabled power-down mode.

While in power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the GDDR3 DRAM, while all other input signals are "Don't Care."

The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). A valid executable command may be applied four clock cycle later.

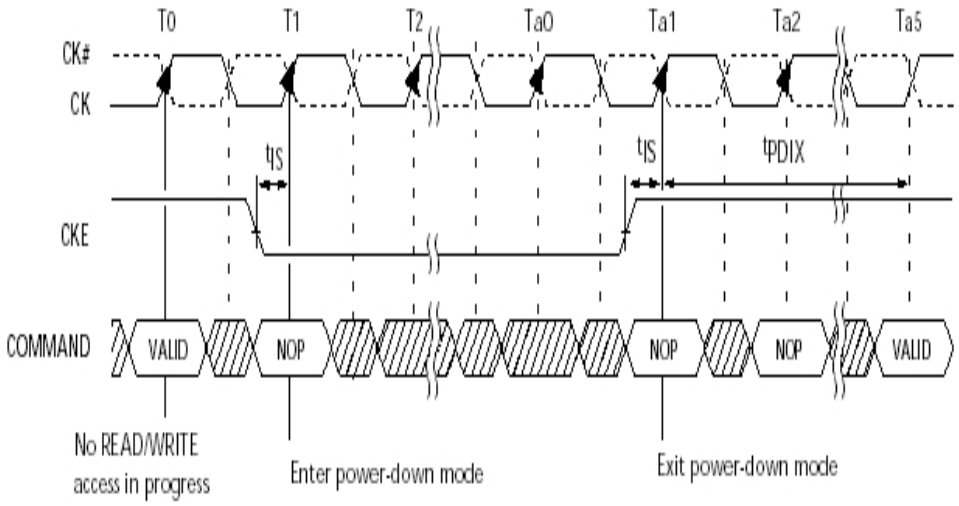


Figure 26
Power-Down

TRUTH TABLE 2 - CKE

(Notes: 1-4)

CKE_{n-1}	CKE_n	CURRENT STATE	$COMMAND_n$	$ACTION_n$	NOTES
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	
		Self Refresh	DESELECT or NOP	Exit Self Refresh	5
H	L	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
		Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
		All Banks Idle	AUTOREFRESH	Self Refresh Entry	

NOTES:

1. CKE_n is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDRII x32immediately prior to clock edge n.
3. $COMMAND_n$ is the command registered at clock edge n, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the ^tXSNR period.
   A minimum of 200 clock cycles is needed before applying a READ command for the DLL to lock.

TRUTH TABLE3-CURRENT STATE BANKn-COMMAND TO BANKn

(Notes: 1-6; notes apeear below and on next page)

CURRENTSTATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
	X	H	L	H	DATA TERMINATOR DISABLE	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTOREFRESH	7
Row Active	L	L	L	L	LOADMODEREGISTER	7
	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto Precharge Disabled)	L	H	L	H	READ (select column and start new READ bursst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (only after the READ burst is complete)	8
Write (Auto Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (only after the WRITE burst is complete	8, 11

NOTE:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH(see Truth Table 2)and after ^tXSNR has been met(if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:

Idle : The bank has been precharged, and ^tRP has met.

Row Active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

Read: A READ burst has been initiated, with auto precharge disabled.

Write: A WRITE burst has been initiated, with auto precharge disabled.

4. The following states must not be interruupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.

Precharging: starts with registration of a PRECHARGE command and ends when ^tRP is met. Once tRP is met, the bank will be in the idle state.

Row Activating: Starts with registration of an ACTIVE command and ends when ^tRCD is met. Once ^tRCD is met, the bank will be in the "row active" state.

Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bannk will be in the idle state.

NOTE (continued):

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Stars with registration of an AUTO REFRESH command and ends when ^{t}RC is met. Once ^{t}RC is met, the DDRII x32 will be in the all banks idle state.

   Accessing Mode

   Register: Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the GDDR3 x32 will be in the all banks idle state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once tRP is met, all banks will be in the idle state.

   READ or WRITE: Starts with the registation of the ACTIVE command and ends the last valid data nibble.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Left blank
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst.

TRUTH TABLE 4-CURRENT STATE BANK n-COMMAND TO BANK m

(Notes: 1-7; notes appear below and on next page)

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND / ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
	X	H	L	H	DATA TERMINATORDISABLE	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Read (Auto Pre-charge Dis-abled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Write (Auto Pre-charge Dis-abled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6,7
	L	H	L	L	WRITE (select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE	
Read (With Auto Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Write (With Auto Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Truth Table 2) and after ^tXSNR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m, assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

Idle: The bank has been precharged, and ^tRP has been met.
Row Active: A row in the bank has been activated, and ^tRCD has been met.
No data bursts/accesses and no register accesses are in progress.
Read: A READ burst has been initiated, with auto precharge disabled.
Write: A WRITE burst has been initiated, with auto precharge disabled.

Read with Auto
Precharge Enabled: See following text

NOTE (continued):

Write with Auto
Precharge Enabled: See following text

3a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRE CHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins.
During the precharge period of the read with auto precharge enabled or write with auto precharge enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

3b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different is summarized below.

From Command	To Command	Minimum delay (with concurrent auto precharge)
WRITE w/AP	READ or READ w/AP WRITE or WRITE w/AP PRECHARGE ACTIVE	[WL+(BL/2)] ^{t}CK+^{t}WTR (BL/2) ^{t}CK 1 ^{t}CK 1 ^{t}CK
READ w/AP	READ or READ w/AP WRITE or WRITE w/AP PRECHARGE ACTIVE	(BL/2)*^{t}CK [CL$_{RU}$+(BL/2)]+2-WL ^{t}CK 1 ^{t}CK 1 ^{t}CK

CL$_{RU}$=CAS Latency (CL) rounded up to the next integer
BL=Bust Length

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. All states and sequences not shown are illegal or reserved.
6. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
7. Requires appropriate DM masking.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
Relative to V_{SS} ---------- -0.5V to +2.5V
Voltage on V_{DDQ} Supply
Relative to V_{SS} ---------- -0.5V to +2.5V
Voltage on V_{REF} and Inputs
Relative to V_{SS} ---------- -0.5V to +2.5V
Voltage on I/O Pins
Relative to V_{SS} ---------- -0.5V to V_{DDQ} +0.5V
MAX Junction Temperature, T_J ----------+125℃
Storage Temperature (plastic) ------ -55℃ to +150℃
Power Dissipation ---------- TBD
Short Circuit Output Current ---------- 50mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these of any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

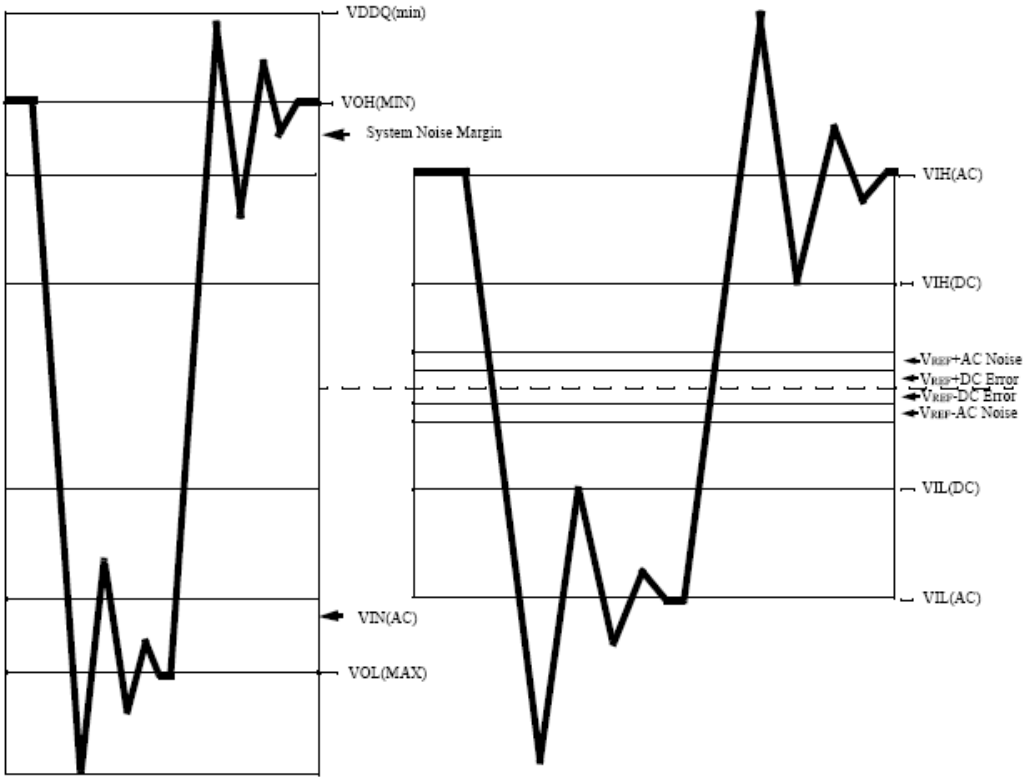
DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	1.9	2.0	2.1	V
I/O Supply Voltage	V_{DDQ}	1.9	2.0	2.1	V
I/O Reference Voltage	V_{REF}	0.69xV_{DDQ}	0.70xV_{DDQ}	0.71xV_{DDQ}	V
Input High(Logic 1) Voltage	$V_{IH(DC)}$	V_{REF}+0.15	-	-	V
Input Low(Logic 0) Voltage	$V_{IL(DC)}$	-	-	V_{REF}-0.15	V
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ VDD (All other pins not under test=0V)	I_I	-5	-	5	uA
OUTPUT LEAKAGE CURRENT (DQs ARE DISABLED; 0V ≤ VOUT ≤ VDDQ)	I_{OZ}	-5	-	5	uA
OUTPUT Logic Low	$V_{OL(DC)}$	-	-	0.76	V

AC INPUT OPERATING

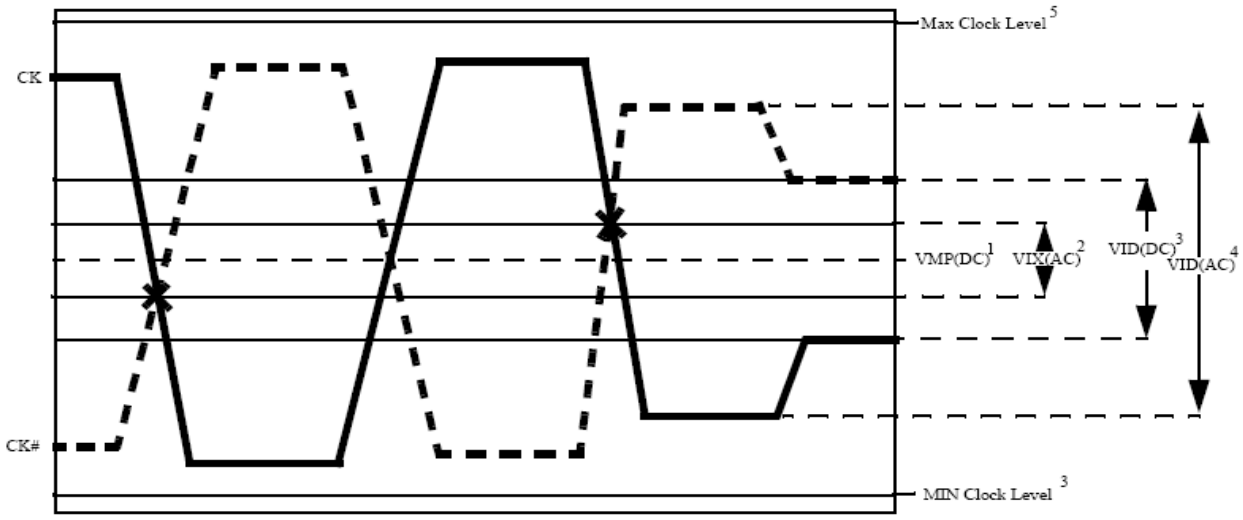
PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Input High (Logic 1) Voltage; DQ	$V_{IH(AC)}$	V_{REF}+0.250	-	-	V
Input Low (Logic 0) Voltage; DQ	$V_{IL(AC)}$	-	-	V_{REF}-0.250	V
Clock Input Differential Voltage; CK and CK#	$V_{ID(AC)}$	0.5	-	VDDQ+0.5	V
Clock Input Crossing Pointl Voltage; CK and CK#	$V_{IX(AC)}$	V_{REF}-0.15	0.70xVDDQ	V_{REF}+0.15	V

INPUT AND OUTPUT VOLTAGE WAVEFORM



CLOCK INPUT OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Clock Input Mid-Point Voltage; CK and CK#	$V_{MP(DC)}$	1.16	1.26	1.36	V
Clock Input Voltage Level; CK and CK#	$V_{IN(DC)}$	0.42	-	V_{DDQ}+0.3	V
Clock Input Differential Voltage; CK and CK#	$V_{ID(DC)}$	0.22		V_{DDQ}	V
Clock Input Differential Voltage; CK and CK#	$V_{ID(AC)}$	0.5		V_{DDQ}+0.5	V
Clock Input Crossing Point Voltage; CK and CK#	$V_{IX(AC)}$	VREF-0.15	0.70xVDDQ	VREF+0.15	V



NOTE:
1. This provides a minimum of 1.16V to a maximum of 1.36V, and is always 70% of VDDQ.
2. CK and CK# must cross in this region.
3. CK and CK# must meet at least VIN(DC) MIN when static and is centered around VMP(DC).
4. CK and CK# must have a minimum 600mV peak-to-peak swing.
5. CK or CK# may not be more positive than VDDQ + 0.5V or lower than 0.22V.
6. For AC operation, all DC clock requirements must also be satisfied.
7. Numbers in diagram reflect nominal values.

Figure 28
Clock Input

CAPACITANCE
(Note: 13)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance: DQs, DQS, DM	DC_{IO}	-	0.20	pF	24
Delta Input Capacitance: Command and Address	DC_{I1}	-	0.40	pF	29
Delta Input Capacitance: CK, CK#	DC_{I2}	-	0.10	pF	29
Input/Output Capacitance: DQs, DQS, DM	C_{IO}	2.5	3.5	pF	
Input Capacitance: Command and Address	C_{I1}	2.0	3.0	pF	
Input Capacitance: CK, CK#	C_{I2}	2.0	3.0	pF	
Input Capacitance: CKE	C_{I3}	2.0	3.0	pF	
Input Capacitance: RES	C_{I4}	1.0	2.0	pF	

IDD SPECIFICATIONS AND CONDITIONS I
(Notes: 1-5, 10, 12, 14, 40;notes on pages 47-50)(0℃ ≤ Tc ≤ +85℃; VDDQ=+2.0V ± 0.1V, VDD=+2.0V ± 0.1V)

PARAMETER/CONDITION	SYMBOL	MAX				UNITS	NOTES
		-12	-13	-14	-15		
OPERATING CURRENT: One bank;Active-Pre-charge;$^{t}RC=^{t}RC(MIN)$; $^{t}CK=^{t}CK(MIN)$; DQ, DM, and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle; WL=4	I_{DD0}	500	480	450	420	mA	22
OPERATING CURRENT:One bank;Active-Read-Precharge; Burst=4;$^{t}RC=^{t}RC(MIN)$;$^{t}CK=^{t}CK(MIN)$;I_{OUT}=0mA; Address and control inputs changing once per clock cycle; WL=4	I_{DD1}	530	500	480	450	mA	22
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Poweer-down mode; $^{t}CK=^{t}CK$ MIN; CKE=LOW;	I_{DD2P}	70	70	70	70	mA	32
IDLE STANDBY CURRENT: CS#=HIGH;All banks idle; $^{t}CK=^{t}CK$ (MIN); CKE=HIGH; Address and other control inputs changing once per clock cycle	I_{DD2N}	205	195	185	175	mA	
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $^{t}CK=^{t}CK(MIN)$; CKE=LOW' WL=4	I_{DD3P}	70	70	70	70	mA	32
ACTIVE STANDBY CURRENT: CS#=HIGH; CKE=HIGH;address One bank; Active-Precharge; $^{t}RC=^{t}RAS$ (MAX); $^{t}CK=^{t}CK$ (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I_{DD3N}	440	420	400	380	mA	22
OPERATING CURRENT: Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^{t}CK=^{t}CK$ (MIN); I_{OUT}=0mA; WL=4	I_{DD4R}	1300	1250	1200	1150	mA	
OPERATING CURRENT: Burst=2;Writes;Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^{t}CK=^{t}CK(MIN)$; DQ, DM and DQS inputs changing twice per clock cycle; WL=4	I_{DD4W}	1300	1250	1200	1150	mA	
AUTO REFRESH CURRENT	I_{DD5}	540	520	500	480	mA	22
SELF REFRESH CURRENT:CKE<0.2V Standard	I_{DD6}	20	20	20	20	mA	11

IDD SPECIFICATIONS AND CONDITIONS II

(Notes: 1-5, 10, 12, 14, 40;notes on pages 47-50)(0℃ ≤ Tc ≤ +85℃; VDDQ=+2.0V ± 0.1V, VDD=+2.0V ± 0.1V)

PARAMETER/CONDITION	SYMBOL	MAX				UNITS	NOTES
		-16	-18	-2	-22		
OPERATING CURRENT: One bank;Active-Pre-charge;^{t}RC=^{t}RC(MIN); ^{t}CK=^{t}CK(MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle; WL=4	I_{DD0}	400	380	360	340	mA	22
OPERATING CURRENT:One bank;Active-Read-Precharge; Burst=4;^{t}RC=^{t}RC(MIN);^{t}CK=^{t}CK(MIN);I_{OUT}=0mA; Address and control inputs changing once per clock cycle; WL=4	I_{DD1}	425	400	370	350	mA	22
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Poweer-down mode; ^{t}CK=^{t}CK MIN; CKE=LOW;	I_{DD2P}	70	70	70	70	mA	32
IDLE STANDBY CURRENT: CS#=HIGH;All banks idle; ^{t}CK=^{t}CK (MIN); CKE=HIGH; Address and other control inputs changing once per clock cycle	I_{DD2N}	165	155	145	135	mA	
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; ^{t}CK=^{t}CK(MIN); CKE=LOW' WL=4	I_{DD3P}	70	70	70	70	mA	32
ACTIVE STANDBY CURRENT: CS#=HIGH; CKE=HIGH;address One bank; Active-Precharge; ^{t}RC=^{t}RAS (MAX); ^{t}CK=^{t}CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I_{DD3N}	370	360	350	340	mA	22
OPERATING CURRENT: Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; ^{t}CK=^{t}CK (MIN); I_{OUT}=0mA; WL=4	I_{DD4R}	1100	1050	1000	950	mA	
OPERATING CURRENT: Burst=2;Writes;Continuous burst; One bank active; Address and control inputs changing once per clock cycle; ^{t}CK=^{t}CK(MIN); DQ, DM and DQS inputs changing twice per clock cycle; WL=4	I_{DD4W}	1100	1050	1000	950	mA	
AUTO REFRESH CURRENT	I_{DD5}	470	450	430	420	mA	22
SELF REFRESH CURRENT:CKE<0.2V — Standard	I_{DD6}	20	20	20	20	mA	11

Note

1. Measured with outputs open and ODT off
2. Refresh period is 32ms
3. Measured current at VDD & VDDQ = 2.0V

ELECTRICAL CHARACTERISTICS AND AC OPERATING CONDITIONS I

(Notes: 1-5, 14-17, 33, 40; notes on pages 47-50) (0℃ ≤ Tc ≤ +85℃; VDDQ=+2.0 ± 0.1V, VDD=+2.0V ± 0.1V)

AC CHARACTERISTICS	SYMBOL	-12		-13		-14		-15		UNITS	NOTES
PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Access window of DQs and RDQS from CK/CK#	tAC	-0.25	+0.25	-0.25	+0.25	-0.26	+0.26	-0.26	+0.26	tCK	
CK high-level width	tCH	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK	30
CK low-level width	tCL	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK	30
Clock cycle time	CL=9	1.2	3.3	1.3	3.3	-	-	-	-	ns	
	CL=8	-	-	-	-	1.4	3.3	1.5	3.3	ns	
WRITE Latency	tWL	2	3	2	3	2	3	2	3	tCK	43
DQ and DM input hold time relative to DQS	tDH	0.16		0.16		0.18		0.18		ns	26, 31
DQ and DM input setup time relative to DQS	tDS	0.16		0.16		0.18		0.18		ns	26, 31
DQS input high pulse width	tDQSH	0.45		0.45		0.45		0.45		tCK	
DQS input low pulse width	tDQSL	0.45		0.45		0.45		0.45		tCK	
DQS-DQ skew	tDQSQ	-0.14	0.14	-0.15	0.15	-0.16	0.16	-0.17	0.17	ns	25, 26
Write command to first DQS latching transition	tDQSS	WL -0.25	WL +0.25	WL -0.25	WL +0.25	WL -0.25	WL +0.25	WL -0.25	WL +0.25	tCK	
DQS falling edge to CK rising-setup time	tDSS	0.25		0.25		0.25		0.25		tCK	
DQS falling edge from CK rising-hold time	tDSH	0.25		0.25		0.25		0.25		tCK	
Half strobe period	tHP	tCH min or tCL min		tCH min or tCL min		tCH min or tCL min		tCH min or tCL min		tCK	34
Data-out high-impedance window from CK/CK#	tHZ	-0.3		-0.3		-0.3		-0.3		ns	18
Data-out low-impedance window from CK/CK#	tLZ	-0.3		-0.3		-0.3		-0.3		ns	18
Address and control input hold time	tIH	0.3		0.3		0.35		0.35		ns	14
Address and control input setup time	tIS	0.3		0.3		0.35		0.35		ns	14
Address and control input pulse width	tIPW	0.9		0.9		1.0		1.0		ns	
LOAD MODE REGISTER command cycle time	tMRD	7		7		6		6		tCK	
Data output hold	tQH	tHP-0.14		tHP-0.14		tHP-0.16		tHP-0.16		ns	25, 26, 34

- CONTINUE -

AC CHARACTERISTICS	SYMBOL	-12		-13		-14		-15		UNITS	NOTES
PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVE to PRECHARGE command	tRAS	25	100K	23	100K	22	100K	20	100K	tCK	35
ACTIVE to ACTIVE/AUTO REFRESH command period	tRC	36		33		31		29		tCK	
AUTO REFRESH command period	tRFC	45		42		39		36		tCK	
REFRESH to REFRESH command interval	tREFC		70		70		70		70	us	23
Average periodic refresh interval	tREFI		7.8		7.8		7.8		7.8	us	23
Row Address to Column Address Delay for Read	tRCDR	12		11		10		10		tCK	
Row Address to Column Address Delay for Write	tRCDW	8		7		6		6		tCK	
PRECHARGE command period	tRP	11		10		9		9		tCK	
DQS Read preamble	tRPRE	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
ACTIVE bank a to ACTIVE bank b command	tRRD	5		5		5		5		tCK	42
Exit Power Down	tPDEX	7+tIS		7+tIS		6+tIS		6+tIS		tCK	
DQS Write preamble	tWPRE	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS Write preamble setup time	tWPRES	0		0		0		0		ns	20, 21
DQS Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	19
Write recovery time	tWR	10		9		9		8		tCK	
Internal WRITE to READ command delay	tWTR	5		5		5		5		tCK	
RES to CKE setup	tATS	10		10		10		10		ns	
RES to CKE hold	tATH	10		10		10		10		ns	
Exit Self Refresh to Non-Read command	tXSNR	66		66		66		66		ns	
Exit Self Refresh to Read command	tXSRD	200		200		200		200		tCK	

ELECTRICAL CHARACTERISTICS AND AC OPERATING CONDITIONS II

(Notes: 1-5, 14-17, 33, 40; notes on pages 47-50) (0℃ ≤ Tc ≤ +85℃; VDDQ=+2.0 ± 0.1V, VDD=+2.0V ± 0.1V)

AC CHARACTERISTICS	SYMBOL	-16		- 18		- 2		- 22		UNITS	NOTES
PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Access window of DQs and RDQS from CK/CK#	tAC	-0.28	+0.28	-0.28	+0.28	-0.3	+0.3	-0.3	+0.3	tCK	
CK high-level width	tCH	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK	30
CK low-level width	tCL	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK	30
Clock cycle time	CL=7	1.6	3.3	-	-	-	-	-	-	ns	
	CL=6			1.8	3.3	2.0	3.3	-	-	ns	
	CL=5	-	-	-	-	-	-	2.2	3.3	ns	
WRITE Latency	tWL	2	3	1	3	1	3	1	3	tCK	43
DQ and DM input hold time relative to DQS	tDH	0.25		0.25		0.25		0.30		ns	26, 31
DQ and DM input setup time relative to DQS	tDS	0.25		0.25		0.25		0.30		ns	26, 31
DQS input high pulse width	tDQSH	0.45		0.45		0.45		0.45		tCK	
DQS input low pulse width	tDQSL	0.45		0.45		0.45		0.45		tCK	
DQS-DQ skew	tDQSQ	-0.18	0.18	-0.2	0.2	-0.225	0.225	-0.25	0.25	ns	25, 26
Write command to first DQS latching transition	tDQSS	WL -0.25	WL +0.25	WL -0.25	WL +0.25	WL -0.25	WL +0.25	WL -0.25	WL +0.25	tCK	
DQS falling edge to CK rising-setup time	tDSS	0.25		0.25		0.25		0.25		tCK	
DQS falling edge from CK rising-hold time	tDSH	0.25		0.25		0.25		0.25		tCK	
Half strobe period	tHP	tCH min or tCL min		tCH min or tCL min		tCH min or tCL min		tCH min or tCL min		tCK	34
Data-out high-impedance window from CK/CK#	tHZ	-0.3		-0.3		-0.3		-0.35		ns	18
Data-out low-impedance window from CK/CK#	tLZ	-0.3		-0.3		-0.3		-0.35		ns	18
Address and control input hold time	tIH	0.45		0.45		0.5		0.5		ns	14
Address and control input setup time	tIS	0.45		0.45		0.5		0.5		ns	14
Address and control input pulse width	tIPW	1.2		1.2		1.3		1.5		ns	
LOAD MODE REGISTER command cycle time	tMRD	5		5		4		4		tCK	
Data output hold	tQH	tHP-0.16		tHP-0.19		tHP-0.225		tHP-0.225		ns	25, 26, 34

- CONTINUE -

AC CHARACTERISTICS	SYMBOL	- 16		- 18		- 2		- 22		UNITS	NOTES
PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVE to PRECHARGE command	tRAS	19	100K	17	100K	15	100K	14	100K	tCK	35
ACTIVE to ACTIVE/AUTO REFRESH command period	tRC	27		24		21		19		tCK	
AUTO REFRESH command period	tRFC	34		30		27		25		tCK	
REFRESH to REFRESH command interval	tREFC		70		70		70		70	us	23
Average periodic refresh interval	tREFI		7.8		7.8		7.8		7.8	us	23
Row Address to Column Address Delay for Read	tRCDR	9		8		7		7		tCK	
Row Address to Column Address Delay for Write	tRCDW	5		5		4		4		tCK	
PRECHARGE command period	tRP	8		7		6		6		tCK	
DQS Read preamble	tRPRE	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
ACTIVE bank a to ACTIVE bank b command	tRRD	5		5		5		5		tCK	42
Exit Power Down	tPDEX	6+ tIS		4+ tIS		4+ tIS		4+ tIS		tCK	
DQS Write preamble	tWPRE	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS Write preamble setup time	tWPRES	0	-	0	-	0	-	0	-	ns	20, 21
DQS Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	19
Write recovery time	tWR	8		7		7		6		tCK	
Internal WRITE to READ command delay	tWTR	4		4		3		3		tCK	
RES to CKE setup	tATS	10		10		10		10		ns	
RES to CKE hold	tATH	10		10		10		10		ns	
Exit Self Refresh to Non-Read command	tXSNR	66		66		66		66		ns	
Exit Self Refresh to Read command	tXSRD	200		200		200		200		tCK	

NOTES

1. All voltages referenced to V_{SS}.

2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

3. Outputs measured into equivalent load of 10pf terminated with 60ohms to VDDQ:

4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.0V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 3V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.

5. The AC and DC input level specifications are an open drain design for improved high speed signalling.

6. V_{REF} is expected to equal 70% of V_{DDQ} for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2 percent of the DC value. Thus, from 70% of V_{DDQ}, V_{REF} is allowed ± 25mV for DC error and an additional ± 25mV for AC noise.

7. Reserved for future use.

8. VID is the magnitude of the difference between the input level on CK and the input level on CK#

9. The value of V_{IX} is expected to equal 70% V_{DDQ} for the transmitting device and must track variations in the DC level of the same.

10. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at minimum CAS Latency. Outputs are open during IDD measurments.

11. Enables on-chip refresh and address counters.

12. I_{DD} specifications are tested after the device is properly initialized.

13. This parameter is sampled. V_{DD}=+2.0V ± 0.1V, V_{DDQ}=+2.0V ± 0.1V, V_{REF}=V_{SS}, f=500MHz, T_A=25℃, $V_{OUT(DC)}$=0.75*V_{DDQ}, V_{OUT} (peack to peak)=0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.

14. Input and output slew rate=3V/ns. If the input slew rate is less than 3V/ns, input timing may be compromised. All slew rates are measured between Vih and Vil.

15. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.

16. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, MF, CKE<0.3x V_{DDQ} is recognized as LOW.

17. Reserved for future use..

18. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).

19.The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

20. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.

21. It is recommended that WDQS be valid(HIGH or LOW) on or before the WRITE command. The case shown (WDQS going from High-z to logic LOW) on or before the WRITE command.
The case shown (WDQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress, WDQS could be HIGH during this time, depending on ^{t}DQSS.

22. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS MAX for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for tRAS.

23. The refresh period is 4K every 32ms. This equates to an average refresh rate of 7.8us.

24. The I/O capacitance per DQS and DQ byte/ group will not differ by more than this maximum amount for any given device.

25. The valid data window is derived by achieving other specifications-^{t}DQHP, and ^{t}DQSQ, [^{t}DQHP-0.38ns (-18),^{t}DQHP, and ^{t}DQSQ, ^{t}DQHP=0.45ns (-22)]. The data valid window derates directly proportional with the strobe duty cycle and a practical data valid window can be derived.
The strobe is allowed a maximum duty cycle variation of 48/52. Functionality is uncertain when operating beyond a 48/52 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 48/52 based off the optional READ strobe.

26. Referenced to each output group: RDQS0 with DQ0-DQ7, RDQS1 with DQ8-DQ15, RDQS2 with DQ16-DQ23, and RDQS3 with DQ24-DQ31

27. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC[MIN]) else CKE is LOW(i.e., during standby).

28. The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge and the driver should achieve the same slew rate through the AC values.

29. The Input capacitance per pin group will not differ by more than this maximum amount for any given device..

30. CK and CK# input slew rate must be $\geq$ 3V/ns.

31. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQS slew rate is less than 3V/ns, timing referenced to the mid-point but to the $V_{IL(AC)}$ maximum and $V_{IH(AC)}$ minimum points.

32. V_{DD} must not vary more than 4% if CKE is not active while any bank is active.

33. The clock is allowed up to $\pm$ 90ps of peak to peak jitter. Each timing parameter is allowed to vary by the same amount.

34. ^{t}HP (MIN) is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK/ inputs, collectively during bank active.

35. READs and WRITEs with autoprecharge are not allowed to be issued until ^{t}RAS(MIN) can be satisfied prior to the internal precharge command being issued.

36. Progamable Drive Curves 40ohm example:

a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure A

b) The vaariation in ddriver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure A.

c) The full variation in drive pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure B.

d) The variation in driver pull-up current within nal limits of voltage and temperature is expected, but not guaran teed, to lie within the inner bounding lines of the V-I curve of Figure B.

37. Programable Terminator Curves 60ohm, 120ohm and 240ohm examples:

a) The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure C, D and E.

b) The vaariation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure C, D and E.

38. The voltage levels used are derived from the refernced test load. Inpractice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.

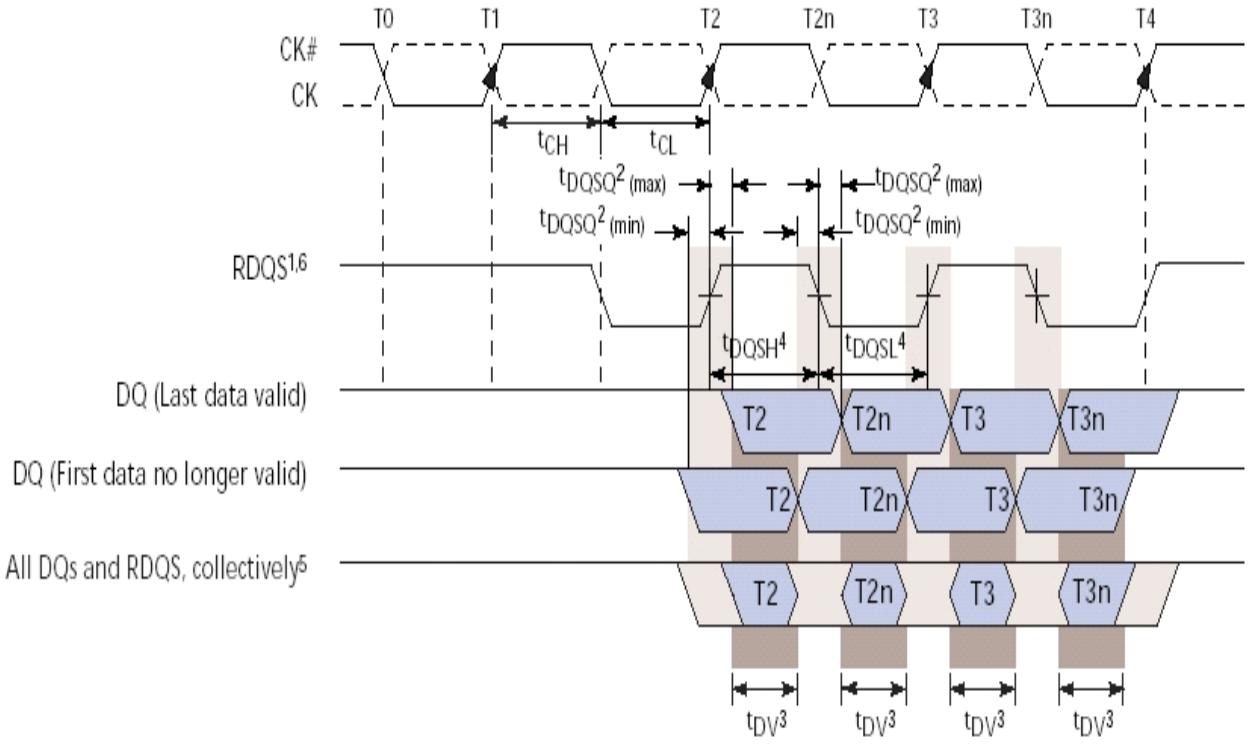
39. V_{IH} overshoot: VIH (MAX)=V_{DDQ}+0.5V for a pulse width $\leq$ 500ps and the pulse width can not be greater than 1/3 of the cycle rate. V_{IL} undershoot: V_{IL}(MIN)=0.0V for a pulse width $\leq$ 500ps and the pulse width can not be greater than 1/3 of the cycle rate.

40. The DLL must be reset when changing the frequency followed by 200 clock cycles

41. Junction temperature is a function of total device power dissipation and devicemounting environment. Measured per SEMI G38-87.

42. The Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number. These parameters are not tested in production.

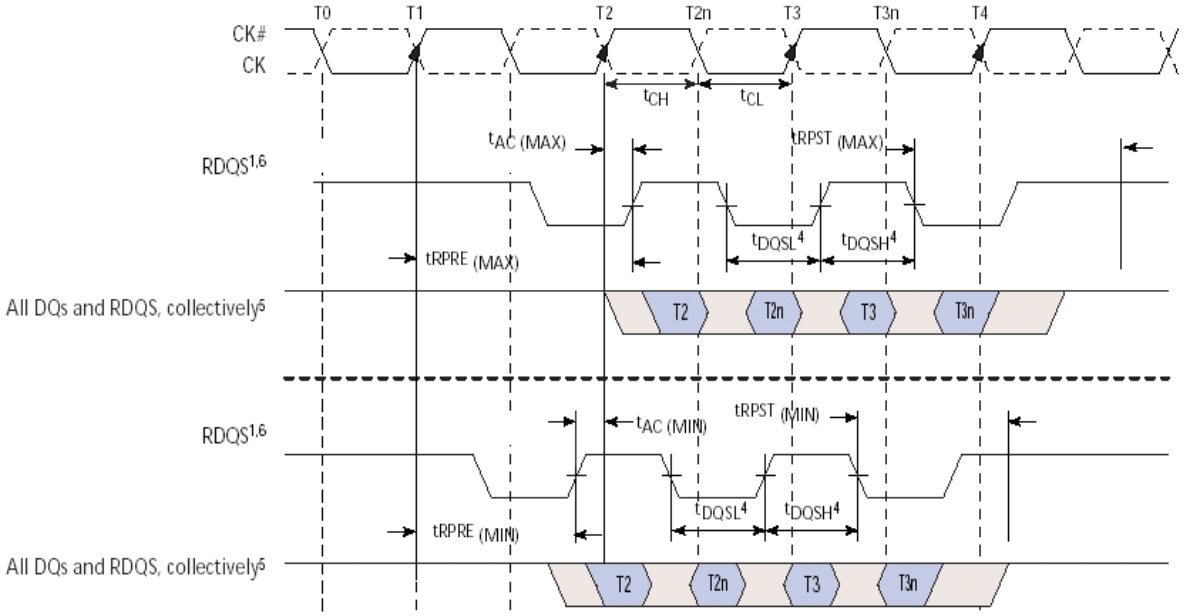
43. The WRITE latency can be set from 1 to 3 clocks but can never be less than 2ns for latencies of 1, 2 and 3 clocks. When the WRITE latency is set to 1, 2 or 3 clocks the input buffers are turned on during the ACTIVE commands reducing the latency but added power.



NOTE:

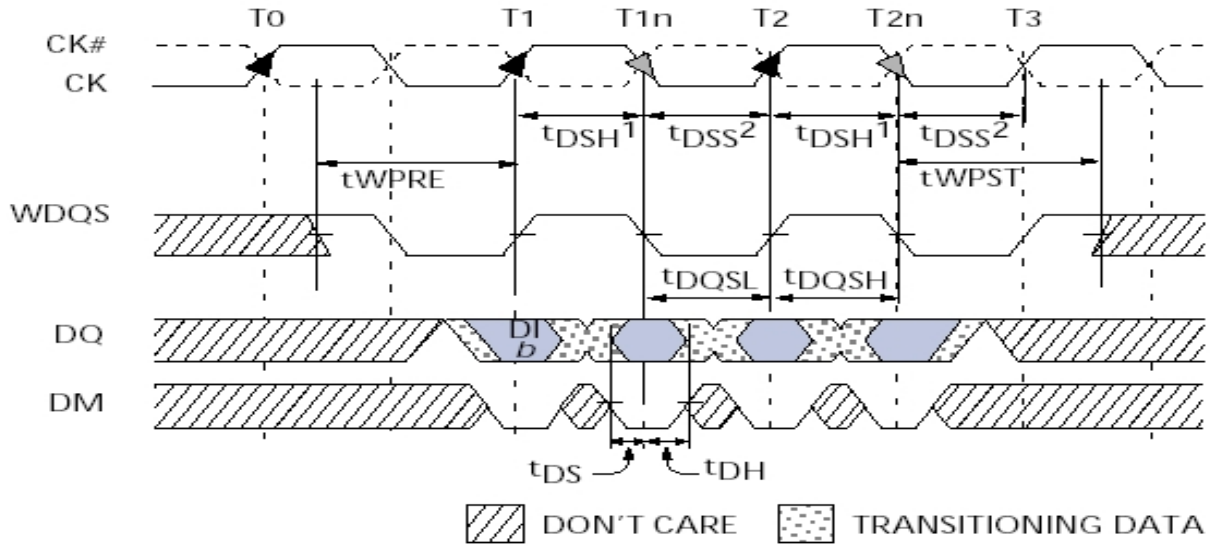
1. ^{t}DQSQ represents the skew between the 8 DQ lines and the respective RDQS pin.
2. ^{t}DQSQ is derived at each RDQS clock edge and is not cumulative over time and begins with first DQ transition and ends with the last valid transition of DQs.
3. ^{t}AC is shown in the nominal case
4. ^{t}DQHP is the lesser of ^{t}DQSL or ^{t}DQSH strobe transition collectively when a bank is active.
5. The data valid window is derived for each RDQS transitions and is defined by ^{t}DV.
6. There are 4RDQS pins for this device with RDQS0 in relation to DQ(0-7), RDQS1 in relation DQ(8-15), RDQS2 in relation to DQ(16-24) and RDQS3 in relation to DQ(25-31).
7. This diagram only represents one of the four byte lanes.

Figure 29
Data Output Timing-^{t}DQSQ, ^{t}QH and Data Valid Window



NOTE: 1. tAC represents the relationship between DQ, RDQS to the crossing of CK and CK#

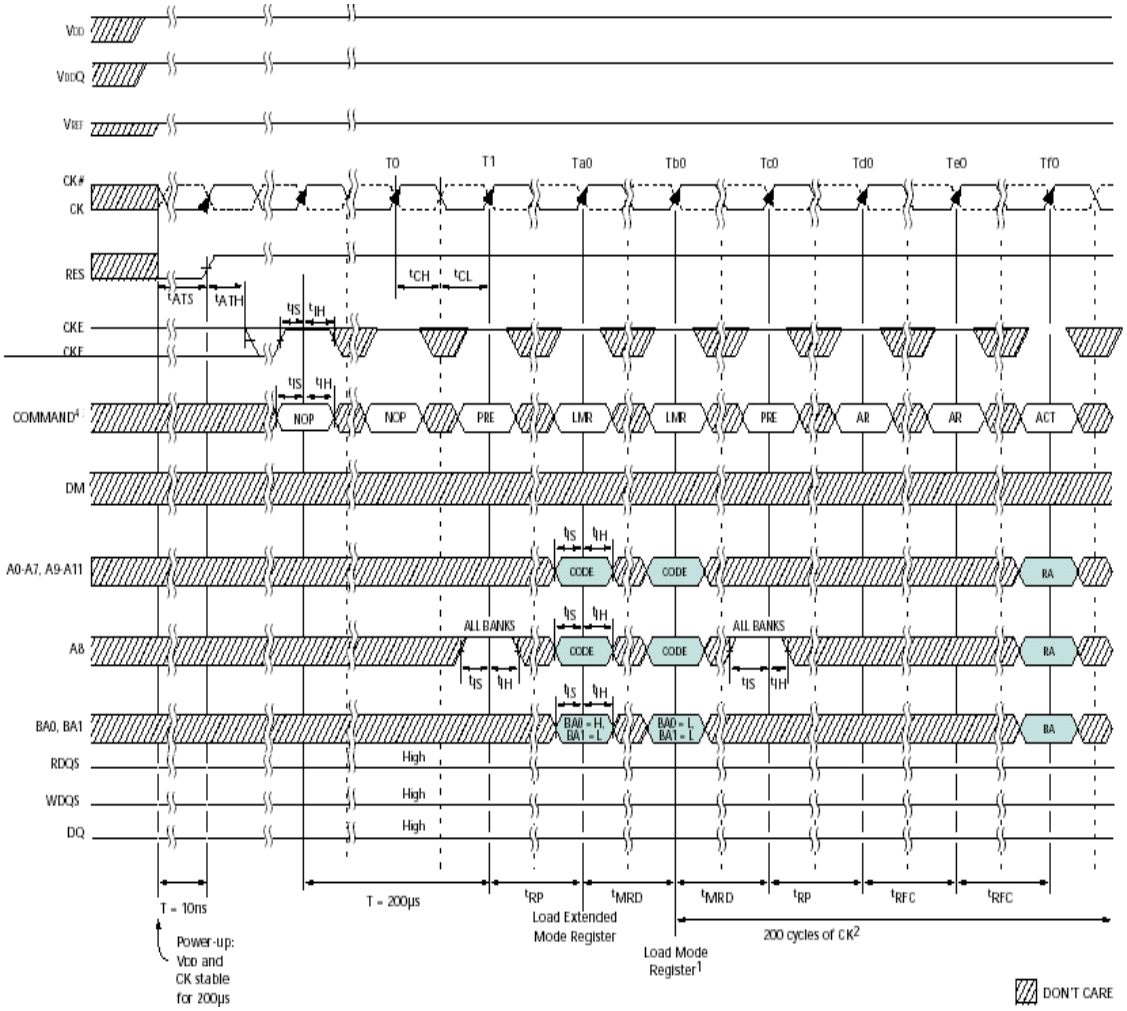
Figure 30
DATA OUTPUT TIMING-TAC, TRPRE, TRPST AND TDQSCK



NOTE:
1. tDSH(MIN) generally occurs during tDQSS(MIN).
2. tDSS(MIN) generally occurs during tDQSS(MAX).

Figure 31
DATA INPUT TIMING

Figure 32
INITIALIZATION AND LOAD MOAD REGISTERS



NOTE:

1. A DLL reset with A8=H is required after enabling the DLL.

2. ^{t}MRD is required before any command can be applied, and 200 cycles of CK are required before a READ command can be issued.

3. The two AUTO REFRESH commands at Tc0 and Td0 may be applied after the LOAD MODE REGISTER(LMR) command at Ta0.

4. PRE=PRECHARGE command, LMR=LOAD MODE REGISTER command, AR=AUTO REFRESH command, ACT=ACTIVE command,RA=Row Address, BA=Bank Address

Figure A

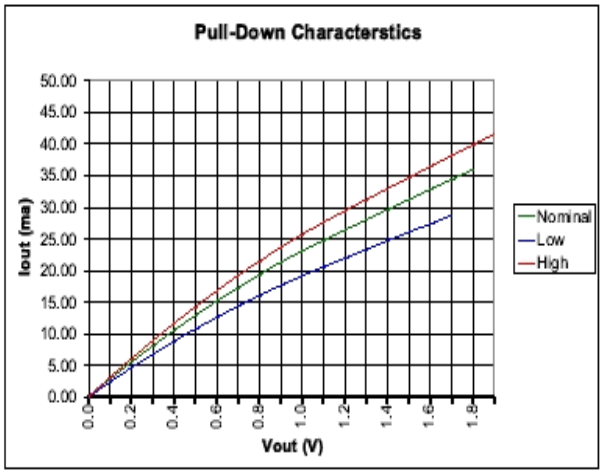
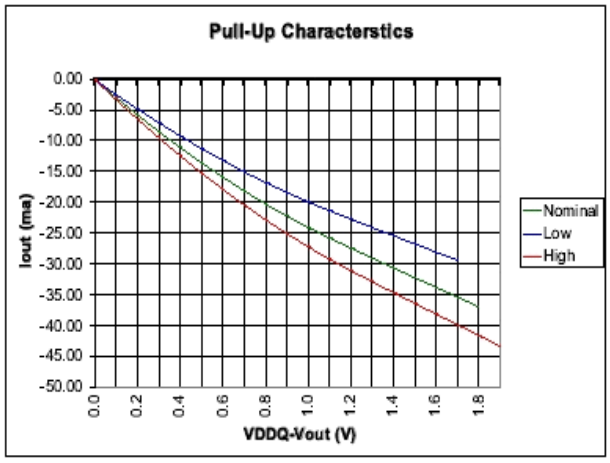


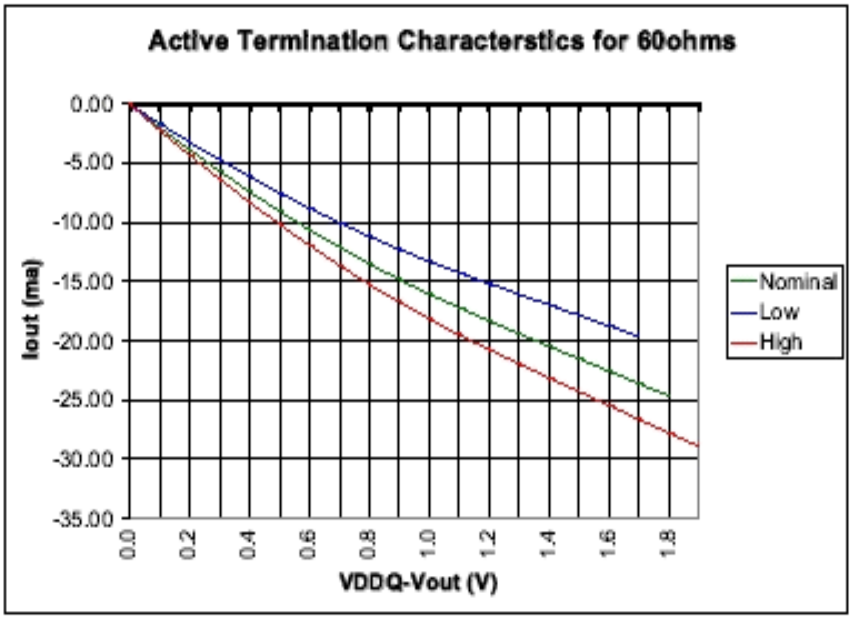
Figure B



PROGRAMED DRIVE CHARACTERISTICS AT 40 OHMS

VOLTAGE (V)	PULL-DOWN CURRENT (mA)			PULL-UP CURRENT (mA)		
	NOMINAL	MINIMUM	MAXIMUM	NOMINAL	MINIMUM	MAXIMUM
0.1	2.77	2.32	3.04	-2.93	-2.44	-3.27
0.2	5.44	4.56	5.98	-5.75	-4.79	-6.42
0.3	8.02	6.70	8.82	-8.46	-7.03	-9.45
0.4	10.49	8.75	11.56	-11.05	-9.18	-12.37
0.5	12.86	10.71	14.19	-13.52	-11.23	-15.17
0.6	15.12	12.57	16.72	-15.87	-13.17	-17.83
0.7	17.27	14.35	19.14	-18.10	-15.01	-20.37
0.8	19.31	16.03	21.44	-20.21	-16.74	-22.78
0.9	21.24	17.63	23.61	-22.18	-18.37	-25.04
1.0	23.04	19.13	25.66	-24.03	-19.90	-27.17
1.1	24.74	20.55	27.57	-25.77	-21.34	-29.17
1.2	26.38	21.94	29.39	-27.42	-22.72	-31.04
1.3	27.99	23.31	31.16	-29.03	-24.07	-32.85
1.4	29.59	24.67	32.91	-30.62	-25.40	-34.62
1.5	31.18	26.03	34.65	-32.21	-26.73	-36.37
1.6	32.77	27.38	36.38	-33.78	-28.06	-38.11
1.7	34.36	28.73	38.11	-35.35	-29.37	-39.85
1.8	35.94	-	39.83	-36.92	-	-41.58
1.9	-	-	41.55	-	-	-43.30

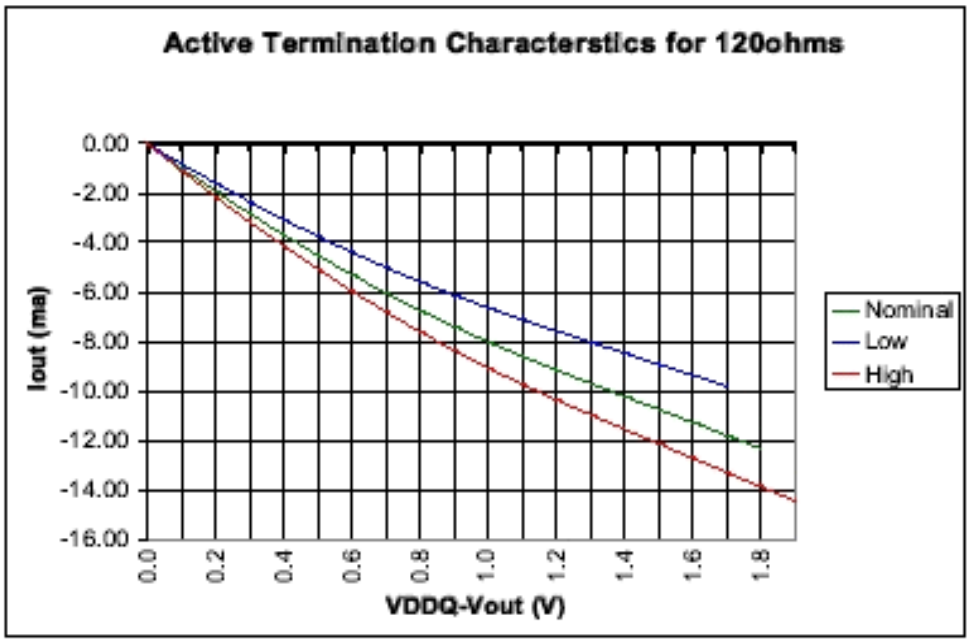
Figure C



PROGRAMED DRIVE CHARACTERISTICS AT 60 OHMS

VOLTAGE (V)	TERMINATOR PULL-UP CURRENT (mA)					
	NOMINAL	MINIMUM	MAXIMUM			
0.1	-1.95	-1.63	-2.18			
0.2	-3.83	-3.19	-4.28			
0.3	-5.64	-4.69	-6.30			
0.4	-7.36	-6.12	-8.25			
0.5	-9.01	-7.49	-10.11			
0.6	-10.58	-8.78	-11.89			
0.7	-12.07	-10.01	-13.58			
0.8	-13.47	-11.16	-15.18			
0.9	-14.79	-12.25	-16.70			
1.0	-16.02	-13.27	-18.12			
1.1	-17.18	-14.23	-19.44			
1.2	-18.28	-15.14	-20.70			
1.3	-19.35	-16.04	-21.90			
1.4	-20.41	-16.94	-23.08			
1.5	-21.47	-17.82	-24.25			
1.6	-22.52	-18.70	-25.41			
1.7	-23.57	-19.58	-26.56			
1.8	-24.61	-	-27.72			
1.9	-	-	-28.87			

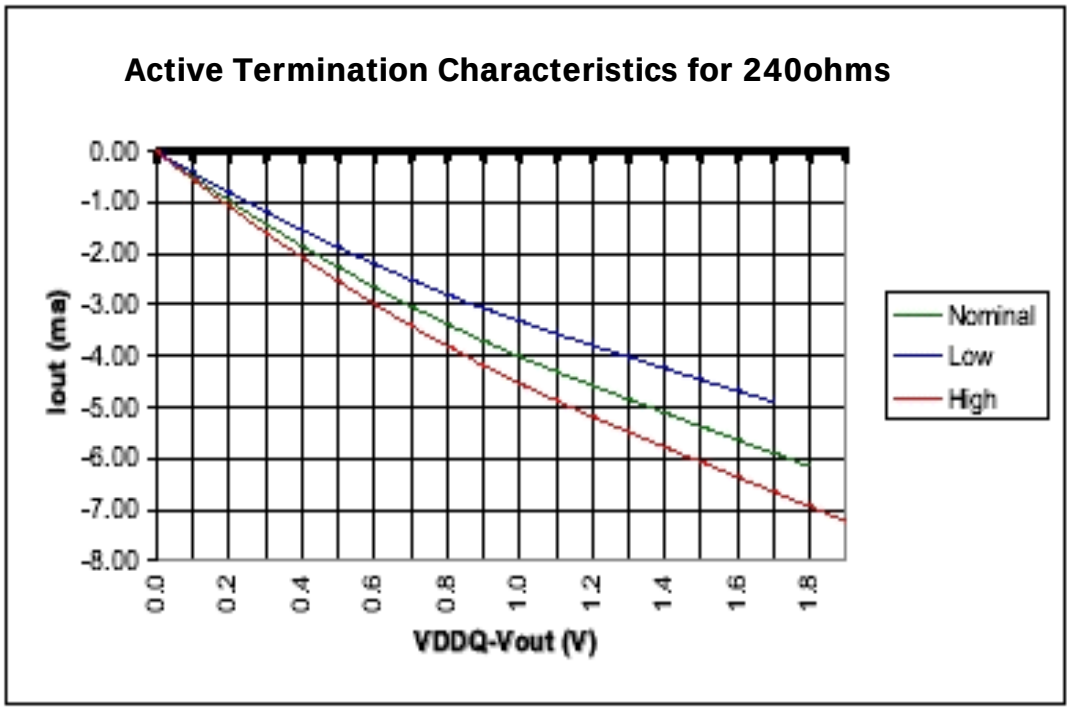
Figure D



PROGRAMED DRIVE CHARACTERISTICS AT 120 OHMS

VOLTAGE (V)	TERMINATOR PULL-UP CURRENT (mA)					
	NOMINAL	MINIMUM	MAXIMUM			
0.1	-0.98	-0.81	-1.09			
0.2	-1.92	-1.60	-2.14			
0.3	-2.82	-2.34	-3.15			
0.4	-3.68	-3.06	-4.12			
0.5	-4.51	-3.74	-5.06			
0.6	-5.29	-4.39	-5.94			
0.7	-6.03	-5.00	-6.79			
0.8	-6.74	-5.58	-7.59			
0.9	-7.39	-6.12	-8.35			
1.0	-8.01	-6.63	-9.06			
1.1	-8.59	-7.11	-9.72			
1.2	-9.14	-7.57	-10.35			
1.3	-9.68	-8.02	-10.95			
1.4	-10.21	-8.47	-11.54			
1.5	-10.74	-8.91	-12.12			
1.6	-11.26	-9.35	-12.70			
1.7	11.78	-9.79	-13.28			
1.8	-12.31	-	-13.86			
1.9	-	-	-14.43			

Figure E

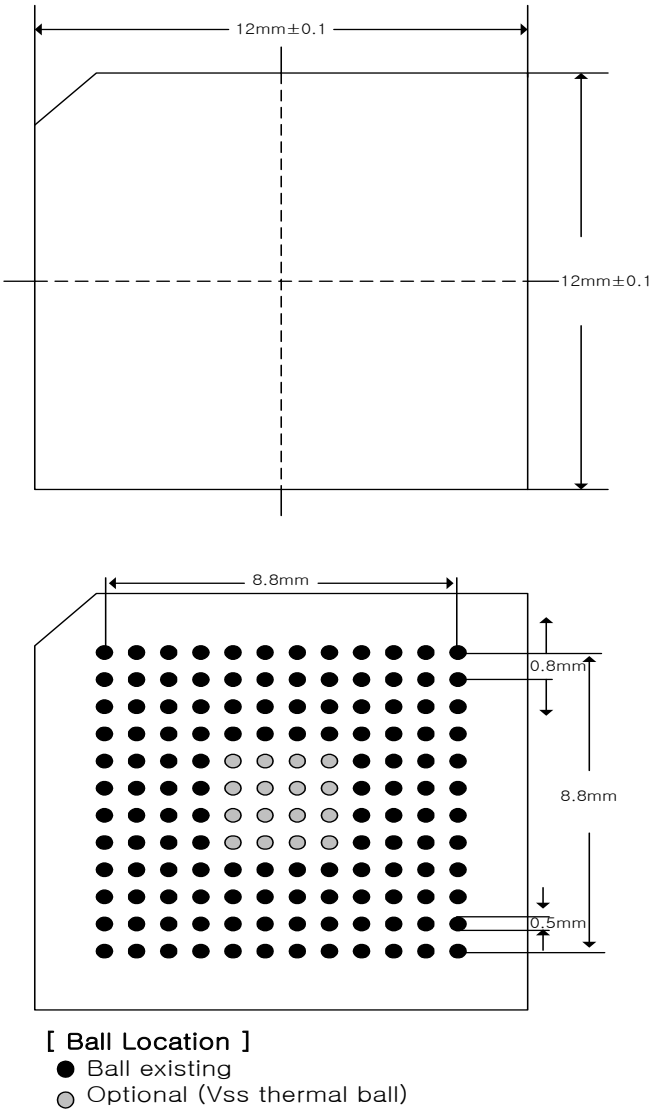


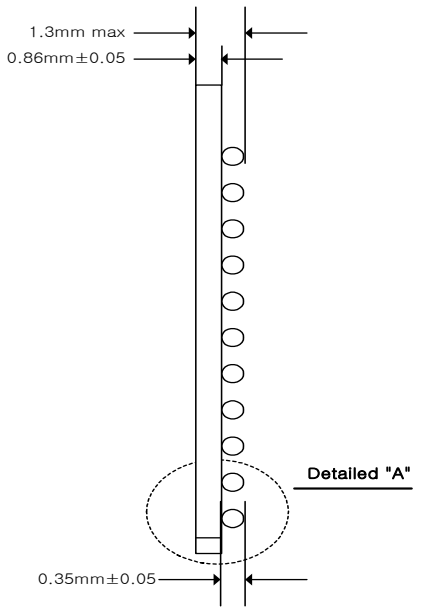
PROGRAMED DRIVE CHARACTERISTICS AT 240 OHMS

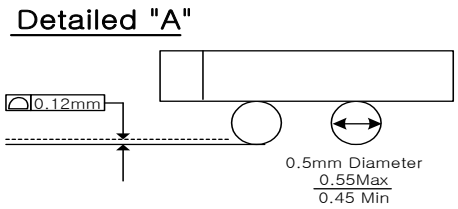
VOLTAGE (V)	TERMINATOR PULL-UP CURRENT (mA)					
	NOMINAL	MINIMUM	MAXIMUM			
0.1	-0.49	-0.41	-0.54			
0.2	-0.96	-0.80	-1.07			
0.3	-1.41	-1.71	-1.58			
0.4	-1.84	-1.53	-2.06			
0.5	-2.25	-1.87	-2.53			
0.6	-2.65	-2.02	-2.97			
0.7	-3.02	-2.50	-3.40			
0.8	-3.37	-2.79	-3.80			
0.9	-3.70	-3.06	-4.17			
1.0	-4.01	-3.32	-4.53			
1.1	-4.29	-3.56	-4.86			
1.2	-4.57	-3.79	-5.17			
1.3	-4.84	-4.01	-5.47			
1.4	-5.10	-4.23	-5.77			
1.5	-5.37	-4.46	-6.06			
1.6	-5.63	-4.68	-6.35			
1.7	-5.89	-4.90	-6.64			
1.8	-6.15	-	-6.93			
1.9	-	-	-7.22			

PACKAGE INFORMATION

12mm x 12mm, 144ball Fine-pitch Ball Grid Array





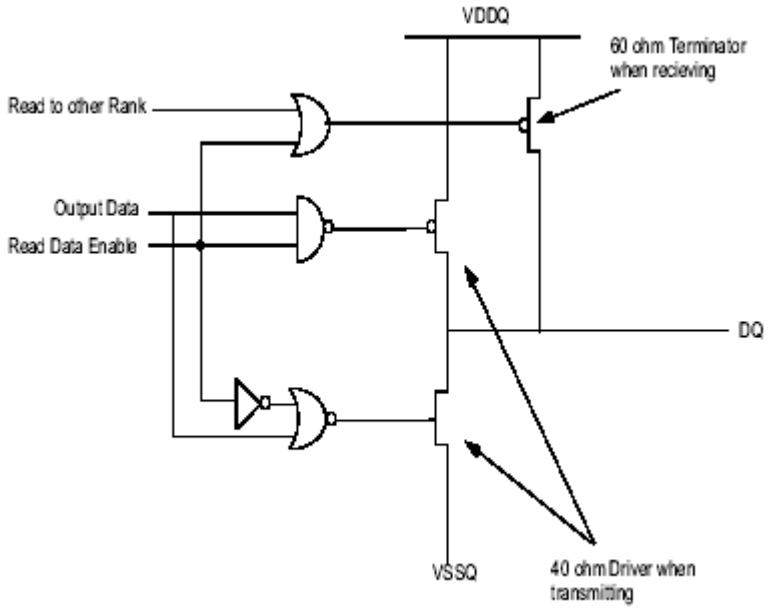


NOTES

1. DIMENSIONS ARE IN MILLMETERS.
2. SOLDER BALL MATERIAL: EUTECTIC 63% Sn, 37% Pb, OR 62% Sn, 36% Pb, 2% Ag.
3. MOLD COMPOUND: EPOXY NOVOLAC.
4. SUBSTRATE MATERIAL: PLASTIC LAMINATE.
5. SOLDER BALL PAD 0.33.
6. SOLDER BALL DIAMETER REFERS TO POST REFLOW CONDITION.
THE PRE-REFLOW DIAMETER IS 0.40.

APENDIX A
I/O DRIVER AND TERMINATION

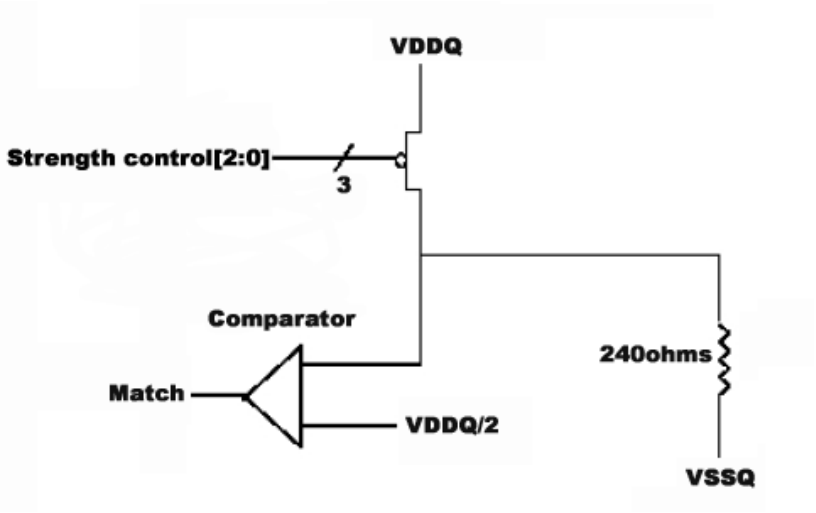
The following diagram shows the general GDDR3 driver and terminator



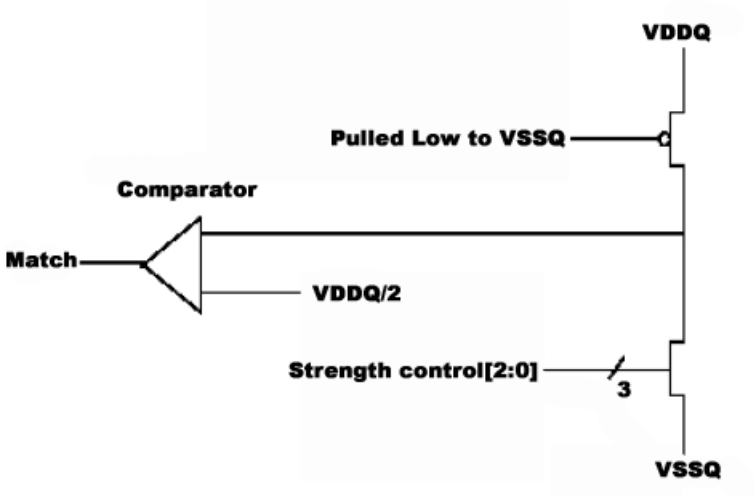
Self Calibration flow for Driver and Terminator

- First calibrate Pmos device against 240ohm resister to VSS via ZQ pin
- This calibrates one Pmos leg to 240 ohms
- Use 1 Pmos leg for 240 ohm terminator
- Use 2 Pmos leg for 120 ohm terminator
- Use 4 Pmos leg for 60 ohm terminator
- Use 6 Pmos leg for 40 ohm pullup driver
- Next calibrate one Nmos leg against the already calibrated 240 ohm Pmos leg
- This calibrates one Nmos leg to 240 ohms
- Use 6 Nmos legs for 40 ohm driver

Self Calibration of Pmos Leg



Self Calibration of Nmos Leg



When Match Nmos leg is calibrated to 240ohms