



DAC0630/DAC0631

Triple 6-Bit Video DAC with Color Palette

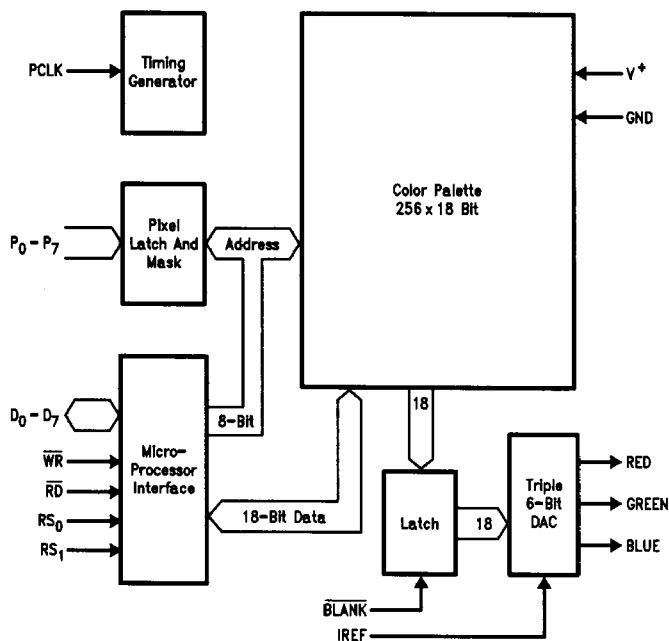
General Description

The DAC0630 and DAC0631 are monolithic triple 6-bit video digital-to-analog converters with on-chip 256 x 18 bit color palettes and are intended for graphics applications. The color palette makes possible the display of 256 colors selected from a total of 256K possible colors through the internal 6-bit video DACs. The DACs are capable of driving 75Ω or 37.5Ω loads to normal video levels at pixel rates of 50 MHz (DAC0630) and 35 MHz (DAC0631). The DAC0630 and DAC0631 provide a bi-directional microprocessor interface with TTL compatible inputs. The DAC0630 and DAC0631 are pin- and functionally-compatible with the Inmos IMS G171-50 and IMS G171-35 and IMS G176-50 and IMS G176-35.

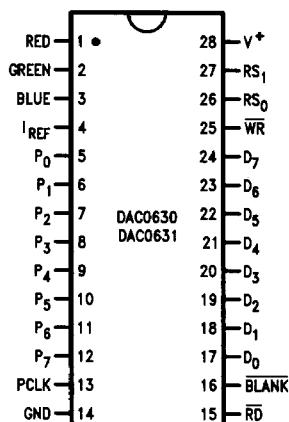
Features

- Pixel rates of 50 MHz (DAC0630) and 35 MHz (DAC0631)
- 256 x 18 bit color palette
- 256K possible colors
- Color palette read-back
- Three internal 6-bit DACs
- Directly drives (75Ω) video cable
- RGB analog output
- Composite blank
- Single +5V supply
- Low power, high performance CMOS/bipolar processing
- TTL compatible inputs
- Full asynchronous μ P interface
- 28-pin package

Block and Connection Diagrams



Dual-In-Line Package



TL/H/9636-2

Top View

Order Number
DAC0630CCD or DAC0631CCD
See NS Package Number D28D

Order Number DAC0631CCN
See NS Package Number N28B

TL/H/9636-1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage (V^+)	GND – 0.3V to 7V
Voltage at Logic Inputs (Note 3)	GND – 0.5V to $V^+ + 0.5V$
Voltage at Analog Pins 1–4 (Note 3)	GND – 0.5V to $V^+ + 0.5V$
Analog Output Current, Pins 1–3	45 mA
Reference Current, Pin 4	15 mA
DC Digital Output Current (Note 4)	25 mA

Power Dissipation (Note 5)	1.0W
ESD Susceptibility (Note 6)	2000V
Soldering Information	
D Package (10 sec)	300°C
N Package (10 sec)	260°C
Storage Temperature	–65°C to 150°C

Operating Ratings (Notes 1 & 2)

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
Positive Supply Voltage	4.5 to 5.5V

AC and DC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}** ; all other limits $T_A = 25^\circ\text{C}$.

Symbol	Parameter		Conditions	DAC0630 DAC0631			Units
				Typical (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
I_{REF}	Reference Current	Minimum			–3		mA
		Maximum			–10		mA
I_{AVE}	Maximum Average Supply Current	DAC0630 DAC0631	$P_{CLK} = 50\text{ MHz}$ $P_{CLK} = 35\text{ MHz}$ $I_{REF} = 10\text{ mA}$ Digital Outputs Unloaded		160 150		mA mA
V_{REFmin}	Minimum Reference Voltage at I_{REF} Pin		$V^+ = 4.5V$ $I_{REF} = 8.88\text{ mA}$		$V^+ - 3$		V
I_{IN}	Maximum Digital Input Current (Pins 5–13, 15, 16, 25–27)		$V^+ = 5.5V$ $GND \leq V_{IN} \leq V^+$		± 10		μA
I_{OZ}	Maximum Tri-State Digital Output Current (Pins 17–24)		$V^+ = 5.5V$ $GND \leq V_{IN} \leq V^+$		± 50		μA
V_{OH}	Minimum Logic “1” Output Voltage		$V^+ = 4.5V, I_O = -5\text{ mA}$		2.4		V
V_{OL}	Maximum Logic “0” Output Voltage		$V^+ = 4.5V, I_O = +5\text{ mA}$		0.4		V
V_{IH}	Minimum Logic “1” Input Voltage		$4.5V \leq V^+ \leq 5.5V$		2		V
V_{IL}	Maximum Logic “0” Input Voltage		$4.5V \leq V^+ \leq 5.5V$		0.8		V
	DAC Resolution				6		Bits
V_{OUT}	Minimum Output Voltage Compliance (Pins 1–3)		$I_{OUT} \leq 10\text{ mA}$		1.5		V

AC and DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = +5V$, unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}** ; all other limits $T_A = 25^\circ C$.

Symbol	Parameter		Conditions	DAC0630 DAC0631			Units
				Typical (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
I_{OUT}	Maximum Output Current Compliance (Pins 1–3)		$V_{OUT} \leq 1V$ $I_{REF} \leq 10\text{ mA}$		21		mA
	Full-Scale Gain Error (Note 10)		$Z_L = 75\Omega + 30\text{ pF}$ $I_{REF} = 4.44\text{ mA}$ $Z_L = 37.5\Omega + 30\text{ pF}$ $I_{REF} = 8.88\text{ mA}$		$-8, +2$ $-14, -4$		% %
	DAC-to-DAC Mismatch		$Z_L = 75\Omega + 30\text{ pF}$ $I_{REF} = 4.44\text{ mA}$ (See Note 11)		± 2		%
	Integral Non-Linearity (Note 12)		$Z_L = 75\Omega + 30\text{ pF}$ $I_{REF} = 4.44\text{ mA}$		± 0.5		LSB
t_{ON}	Rise Time (Note 13)		$Z_L = 75\Omega + 30\text{ pF}$ $I_{REF} = 4.44\text{ mA}$			8	ns
	Maximum Full-Scale Settling Time	DAC0630 DAC0631	$Z_L = 75\Omega + 30\text{ pF}$ $I_{REF} = 4.44\text{ mA}$ (See Note 14)			20 28	ns ns
	Maximum Glitch Energy		$Z_L = 75\Omega + 30\text{ pF}$ $I_{REF} = 4.44\text{ mA}$ (See Note 15)	± 200		± 400	pV-sec
C_{IN}	Digital Input Capacitance (Pins 5–13, 15, 16, 25–27)			7			pF
C_{OUT}	Digital Output Capacitance (Pins 17–24)		$\overline{RD} = \text{Logic High}$	7			pF
C_{OUTA}	Analog Output Capacitance (Pins 1–3)		$\overline{BLANK} = \text{Logic Low}$	10			pF
$V_{OUTBLANK}$	Maximum Blanking Output Voltage		$\overline{BLANK} = \text{Logic Low}$ $Z_L = 75\Omega + 30\text{ pF}$ $I_{REF} = 4.44\text{ mA}$		± 0.5		LSB
	Unadjusted Output Offset Error		$\overline{BLANK} = \text{Logic High}$ $Z_L = 75\Omega + 30\text{ pF}$ $I_{REF} = 4.44\text{ mA}$		± 0.5		LSB
	Clock Feedthrough (Note 16)	DAC0630D DAC0631D DAC0631N	$P_{CLK} = 50\text{ MHz}$ $P_{CLK} = 35\text{ MHz}$ $P_{CLK} = 35\text{ MHz}$ $Z_L = 75\Omega + 30\text{ pF}$ $I_{REF} = 4.44\text{ mA}$			-30 -35 -30	dB dB dB
PSS	Power Supply Sensitivity		$4.5V \leq V^+ \leq 5.5V$ $I_{OUT} = \text{Full Scale}$ $Z_L = 75\Omega + 30\text{ pF}$ $I_{REF} = 4.44\text{ mA}$		6		%/V

AC Electrical Characteristics The following specifications apply for $V^+ = +5V$. **Boldface limits apply for T_{MIN} to T_{MAX} ; all other limits $T_A = 25^\circ C$. Design Limits apply for $4.5V \leq V^+ \leq 5.5V$.**

Symbol	Parameter	Conditions	DAC0630			DAC0631			Units
			Typical (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typical (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
t_{CHCH}	Minimum PCLK Period			20	20		28	28	ns
Δt_{CHCH}	Maximum PCLK Jitter	(Note 17)	± 2.5			± 2.5			%
t_{CLCH}	Minimum PCLK Width Low			6	6		9	9	ns
t_{CHCL}	Minimum PCLK Width High			6	6		7	7	ns
t_{PVCH}	Minimum Pixel Word Setup Time	(Note 18)		4	4		4	4	ns
t_{CHPX}	Minimum Pixel Word Hold Time	(Note 18)		4	4		4	4	ns
t_{BVCH}	Minimum \overline{BLANK} Setup Time	(Note 18)		4	4		4	4	ns
t_{CHBX}	Minimum \overline{BLANK} Hold Time	(Note 18)		4	4		4	4	ns
t_{CHAV}	PCLK to Valid DAC Output	Minimum		5	5		5	5	ns
		Maximum		30	30		30	30	
Δt_{CHAV}	Maximum Differential Output Delay	(Note 20)	1			1			ns
t_{WLWH}	Minimum \overline{WR} Pulse Width Low			50	50		50	50	ns
t_{RLRH}	Minimum \overline{RD} Pulse Width Low			50	50		50	50	ns
t_{SVWL}	Minimum Register Select Setup Time	(Write Cycle)		10	10		15	15	ns
t_{SVRL}	Minimum Register Select Setup Time	(Read Cycle)		10	10		15	15	ns
t_{WLSX}	Minimum Register Select Hold Time	(Write Cycle)		10	10		15	15	ns
t_{RLSX}	Minimum Register Select Hold Time	(Read Cycle)		10	10		15	15	ns
t_{DVWH}	Minimum \overline{WR} Data Setup Time			10	10		15	15	ns
t_{WHDX}	Minimum \overline{WR} Data Hold Time			10	10		15	15	ns
t_{RLQX}	Minimum Output Turn-On Delay			5	5		5	5	ns
t_{RLQV}	Maximum \overline{RD} Enable Access Time			40	40		40	40	ns
t_{RHQX}	Minimum Output Hold Time			5	5		5	5	ns
t_{RHQZ}	Maximum Output Turn-Off Delay	(Note 21)		20	20		20	20	ns
t_{WHWL1}	Minimum Successive Write Interval			$3(t_{CHCH})$	$3(t_{CHCH})$		$3(t_{CHCH})$	$3(t_{CHCH})$	
t_{WHRL1}	Minimum \overline{WR} followed by Read Interval			$3(t_{CHCH})$	$3(t_{CHCH})$		$3(t_{CHCH})$	$3(t_{CHCH})$	
t_{RHRL1}	Minimum Successive Read Interval			$3(t_{CHCH})$	$3(t_{CHCH})$		$3(t_{CHCH})$	$3(t_{CHCH})$	
t_{RHWL1}	Minimum \overline{RD} followed by Write Interval			$3(t_{CHCH})$	$3(t_{CHCH})$		$3(t_{CHCH})$	$3(t_{CHCH})$	
t_{WHWL2}	Minimum \overline{WR} after Color Write	(Note 22)		$3(t_{CHCH})$	$3(t_{CHCH})$		$3(t_{CHCH})$	$3(t_{CHCH})$	

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = +5V$. **Boldface limits apply for T_{MIN} to T_{MAX} ; all other limits $T_A = 25^\circ C$. Design Limits apply for $4.5V \leq V^+ \leq 5.5V$.**

Symbol	Parameter	Conditions	DAC0630			DAC0631			Units
			Typical (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typical (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
t _{WHRL2}	Minimum \overline{RD} after Color Write	(Note 22)		3(t_{CHCH})	3(t_{CHCH})		3(t_{CHCH})	3(t_{CHCH})	
t _{RHRL2}	Minimum \overline{RD} after Color Read	(Note 22)		6(t_{CHCH})	6(t_{CHCH})		6(t_{CHCH})	6(t_{CHCH})	
t _{RHWL2}	Minimum \overline{WR} after Color Read	(Note 22)		6(t_{CHCH})	6(t_{CHCH})		6(t_{CHCH})	6(t_{CHCH})	
t _{WHRL3}	Minimum \overline{RD} after Read Address Write	(Note 22)		6(t_{CHCH})	6(t_{CHCH})		6(t_{CHCH})	6(t_{CHCH})	
	Maximum Write/Read Enable Transition Time				50			50	ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: All voltages are measured with respect to ground, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 20 mA.

Note 4: One output at any time. The maximum time for this output level is one second.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125^\circ C$, and the typical thermal resistance (θ_{JA}) of the DAC0630/0631CCD when board mounted is $40^\circ C/W$. The typical thermal resistance for the DAC0630/631CCN when board mounted is $85^\circ C/W$.

Note 6: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 7: Typicals are at $25^\circ C$ and represent most likely parametric norm.

Note 8: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Design limits are guaranteed to National's AOQL (Average Outgoing Quality Level) but not 100% tested.

Note 10: Full-Scale Gain Error is defined as $\{ [(F.S. I_{OUT})R_L - 2.1(I_{REF})R_L] / [2.1(I_{REF})R_L] \} \times 100\%$. $V_{BLACK LEVEL} = 0V$.

Note 11: The listed value is relative to the midpoint of the full-scale distribution of the internal three DACs.

Note 12: Zero and full-scale adjusted linearity error = $[V_{out} - V_{offset} - (D \times V_{LSB})] / V_{LSB}$. $V_{LSB} = (V_{full scale} - V_{offset}) / 63$.

Note 13: The rise time is measured from 10% to 90% of the full scale transition.

Note 14: The output signal's settling time is measured from a 2% change at the transition's initial value until it has settled to within 2% of the final value, excluding clock feedthrough.

Note 15: This value is determined using triangle approximation: glitch energy = (area of positive transient) - (area of negative transient).

Note 16: The value shown is the ratio of the RMS value of any PCLK signal on the analog outputs to the full-scale output voltage (700 mV).

Note 17: This parameter is the allowed variation in the pixel clock frequency. It does not permit the pixel clock period to vary below the minimum value for pixel clock (t_{CHCH}) period specified above.

Note 18: It is necessary that the color palette's pixel address be a valid logic level with the appropriate setup and hold times at each rising edge of P_{CLK} (this requirement includes the blanking period).

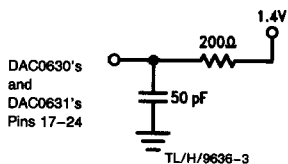
Note 19: A valid analog output is defined as the 50% point between successive values. This parameter is stable with time but can vary between different devices and may vary with different dc operating conditions.

Note 20: This applies to different analog outputs on the same device.

Note 21: Measured at ± 200 mV from initial steady state output voltage.

Note 22: This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

AC Test Conditions Digital Output Load



Input Pulse Levels GND to 3V
 Input Rise and Fall Times (10% to 90%) 2.5 ns
 Digital Input Timing Reference Level 1.5V
 Digital Output Timing Reference Level 0.8V and 2.4V

Timing Waveforms

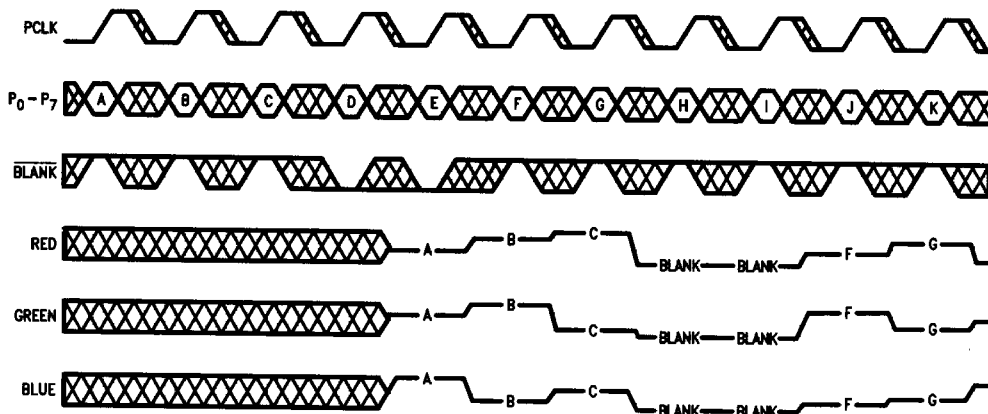


FIGURE 1. System Timing Diagram

TL/H/9636-4

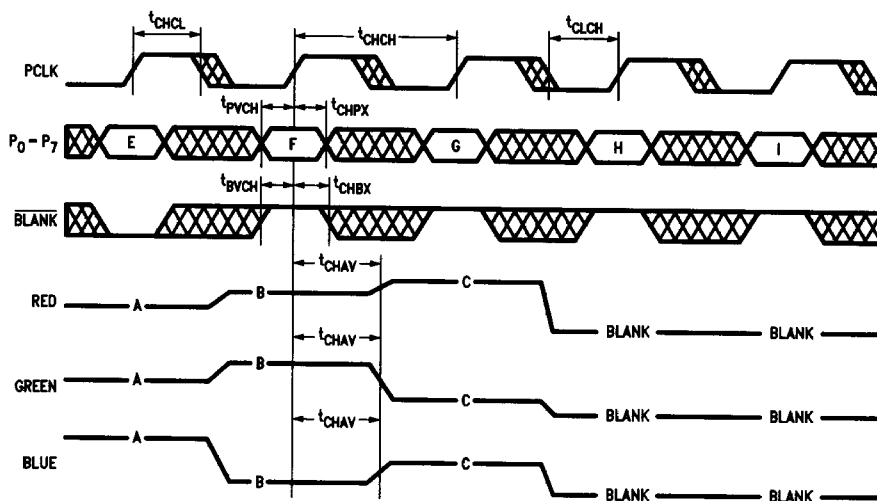


FIGURE 2. Expanded Timing Diagram Detailing Timing Specifications

TL/H/9636-5

Timing Waveforms (Continued)

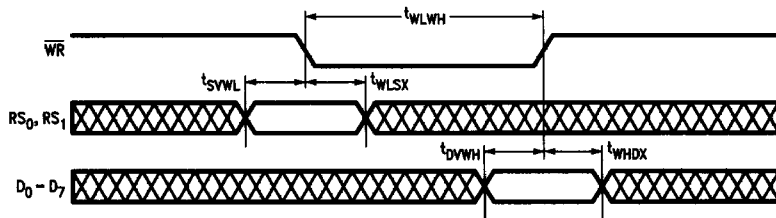


FIGURE 3. Basic Write Cycle

TL/H/9636-6

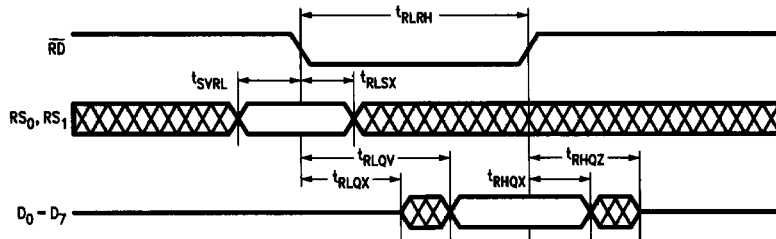


FIGURE 4. Basic Read Cycle

TL/H/9636-7

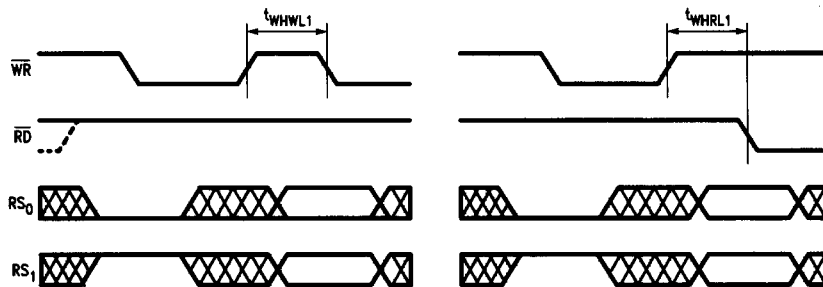


FIGURE 5. Write to Pixel Mask Register Followed by a) Write, b) Read

TL/H/9636-8

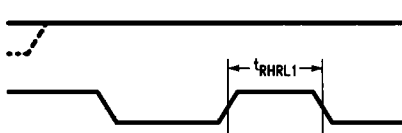


FIGURE 6a. Read from Pixel Mask or Pixel Address Register (Read or Write Mode) Followed by Read

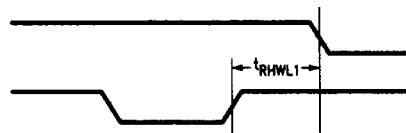


FIGURE 6b. Read from Pixel Mask or Pixel Address Register (Read or Write Mode) Followed by Write

TL/H/9636-9

Timing Waveforms (Continued)

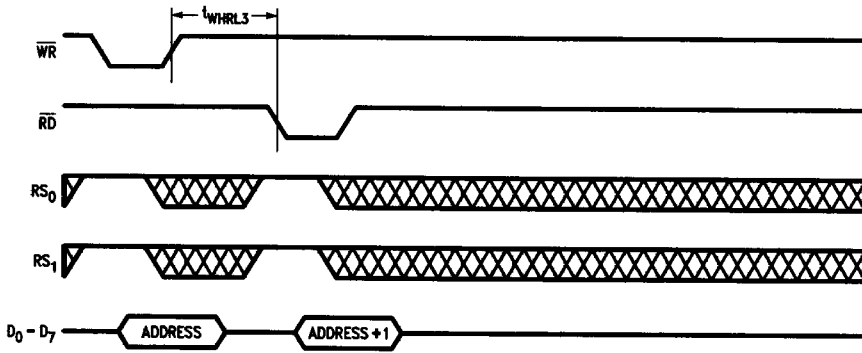


FIGURE 7. Write and Read Back Pixel Address Register (Read Mode)

TL/H/9636-10

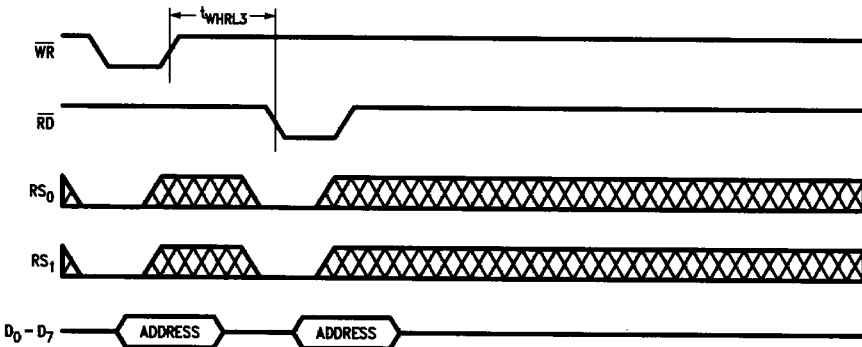


FIGURE 8. Write and Read Back Pixel Address Register (Write Mode)

TL/H/9636-11

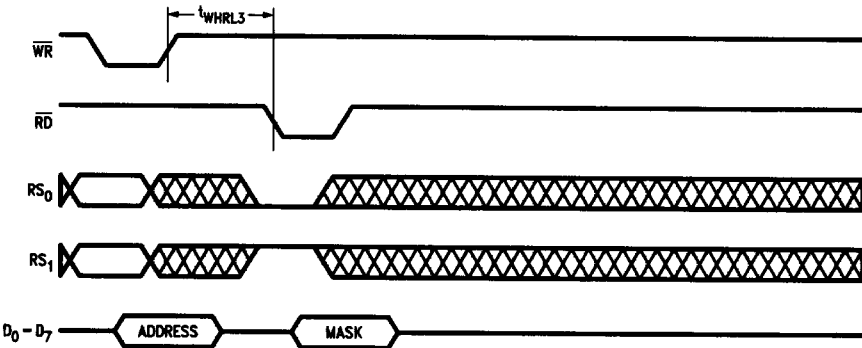


FIGURE 9. Write Pixel Address Register (Read or Write Mode) then Read Pixel Mask Register

TL/H/9636-12

Timing Waveforms (Continued)

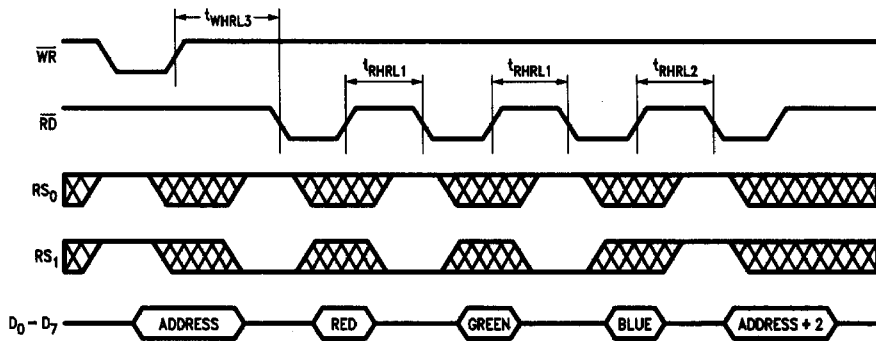


FIGURE 10. Read Color Value then Read Pixel Address Register (Read Mode)

TL/H/9636-13

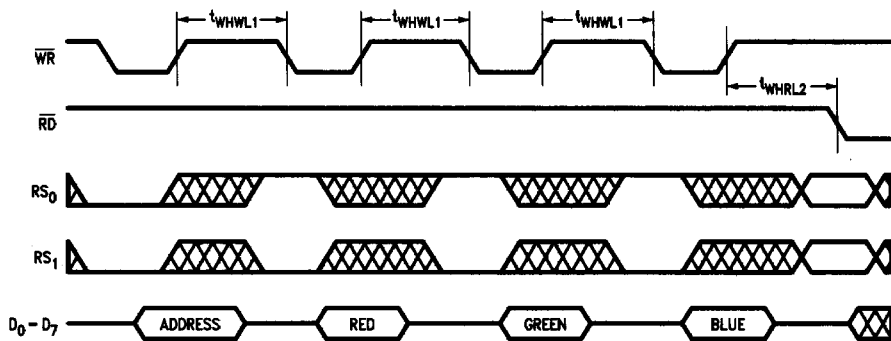


FIGURE 11. Color Value Write Followed by Any Read

TL/H/9636-14

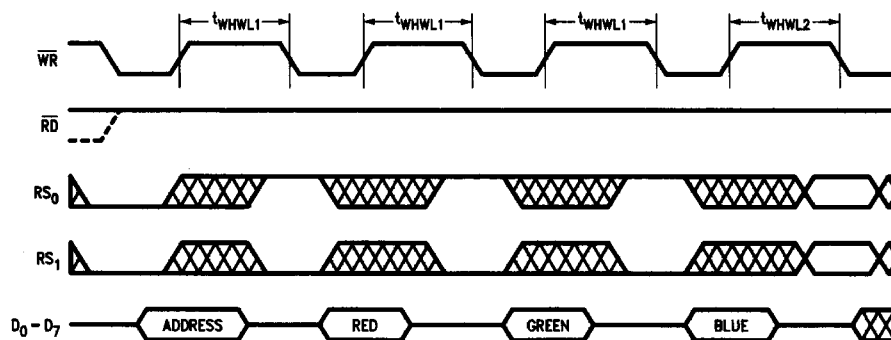


FIGURE 12. Color Value Write Followed by Any Write

TL/H/9636-15

Timing Waveforms (Continued)

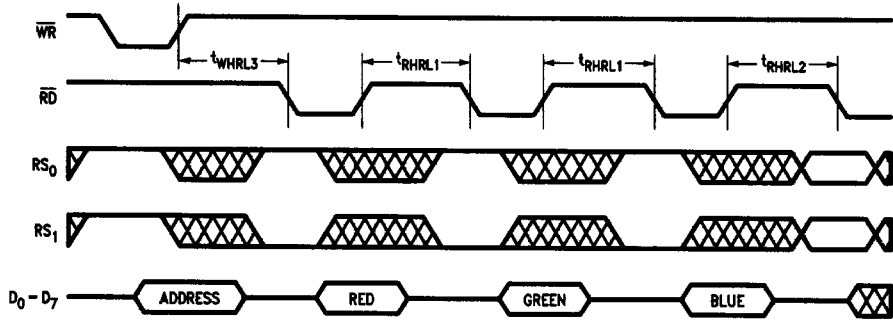


FIGURE 13. Color Value Read Followed by Any Read

TL/H/9636-16

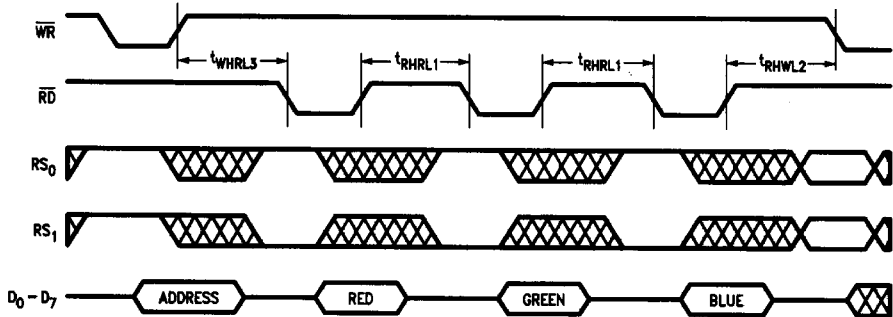
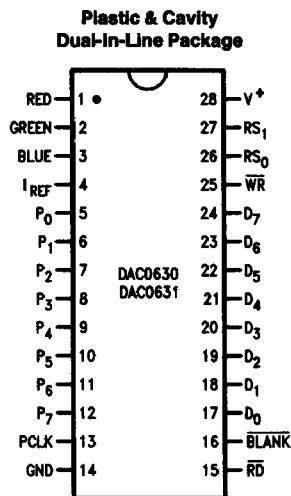


FIGURE 14. Color Value Read Followed by Any Write

TL/H/9636-17

Connection Diagram



TL/H/9638-18

Pin Descriptions

RED (1),

GREEN (2),

BLUE (3)

These are the analog output pins of the 6-bit DACs. The output currents from these pins flow through the terminating resistors and develop the RGB (red, green and blue) voltages that drive the monitor. Each DAC is composed of 63 current sources. The output of each of these current sources is summed together according to the applied 6-bit binary value.

I_{REF} (4)

This is the Reference Current input. The current forced out of this pin to ground determines the current sourced by each of the 63 current sources in each of the three 6-bit DACs. Each current source produces 1/30 of I_{REF} when activated by the 6-bit digital input code.

P₀-P₇ (5-12)

These are the high-speed Pixel Address inputs. This byte-wide information is latched and masked by the Pixel Mask Register. The resulting value is used as an address of a location in the Color Palette RAM.

PCLK (13)

The high-speed Pixel Clock signal is applied to this pin. The rising edge controls the latching of the Pixel Address and Blanking inputs. It also controls the progress of these values through the three stage pipeline of the Color Palette and through the DACs to the outputs.

GND (14)

This is the ground power supply connection.

RD (15)

This is the active low Read bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D₀-D₇.

BLANK (16)

This is an active low signal that forces the DAC's outputs to zero. When BLANK is asserted a video monitor's screen becomes black and the DACs ignore any output values from the Color Palette. However, the Color Palette can still be updated through D₀-D₇.

D₀-D₇ (17-24)

These are the bidirectional Data I/O lines used by the host microprocessor to write information (using the active low WR) into and read information (using the active low RD) from the DAC0630 and DAC0631's internal registers (Pixel Address register, Color Value register, and Pixel Mask register).

During the write cycle, the rising edge of WR latches the data into the selected register.

The rising edge of RD determines the end of the read cycle.

With RD and WR equal to a logic high, the Data I/O lines will no longer contain information from the selected register and will go into a tristate mode.

WR (25)

This is the active low Write signal. It controls the timing of the write operations on the microprocessor interface inputs, D₀-D₇. When active, any information present on the external data bus is available to the Data I/O lines, D₀-D₇.

RS₀, RS₁ (26, 27)

These are the Register Select lines which control the selection of one of the three internal registers. These two lines are sampled during the falling edges of the enable signals (RD or WR). See Functional Description for more information regarding the internal registers.

V⁺ (28)

This is the positive supply pin. It is normally connected to +5 Vdc and bypassed with a 10 μF tantalum capacitor and a 0.1 μF chip capacitor.

Functional Description

The DAC0630 (or DAC0631) forms the output stage for high resolution raster scan RGB video systems. It contains a Color Palette with 256 memory locations that are 18 bits wide. The color palette's output is connected to three high speed current output 6-bit video DACs. The devices use on-board registers to interface easily with microprocessors.

MICROPROCESSOR INTERFACE

The DAC0630 and DAC0631's microprocessor interface consists of three internal registers; Pixel Address register, Color Value register, and Pixel Mask register. These are individually accessed by register select signals, RS₀ and RS₁. The following table defines which of the three internal registers is selected by each of the four combinations of logic states of RS₀ and RS₁.

RS ₀	RS ₁	Register
0	0	Pixel Address (Write Mode)
1	1	Pixel Address (Read Mode)
1	0	Color Value
0	1	Pixel Mask

The contents of the color palette can be accessed through the Color Value and Pixel Address registers.

All of the operations on the microprocessor interface can take place asynchronously to the pixel information currently being processed by the Color Palette.

The **Pixel Address** register is a byte-wide latch that receives and latches address information applied to pins 17–24. It can be used in either the Read and Write mode depending on the logic state of RS₀ and RS₁. With RS₀ = RS₁ = 0 (register select = 0,0), the Pixel address register is in the **write** mode. Two events normally precede **writing** one or more new color definitions to the color palette. The first is the specification of a color palette address. Second, the Color Value register must be loaded with a color definition. The sequence of data transfer is 1) the desired color palette address (this address is stored in the Pixel Address register) and 2) the color definitions: red, green and blue. Refer to *Figures 11 and 12*.

When RS₀ = RS₁ = 1 (register select = 1,1), the Pixel Address register is in the **read** mode. Once again, two events take place and normally precede **reading** one or more color definitions in the color palette. The first action is to specify an address within the color palette, the second is to load the Color Value register with the contents of the color palette location whose address is stored in the Pixel Address Register. The color definition data transfer sequence is red, green and blue. Refer to *Figures 10, 13 and 14*.

The **Color Value** register is an internal 18-bit wide register used as a buffer between the microprocessor interface and the color palette. It is accessed by setting RS₀ = 1 and RS₁ = 0. A color definition can be read from or written to this register by a sequence of three byte-wide transfers to this register address. When a byte is written to this register, only the least significant six bits (D₀–D₅) contain color information. When a byte is read from this register address, only the six least significant bits contain information—the most significant two bits are set to zero. Refer to *Figures 10–14*.

After the write sequence is completed, the Color Value register's contents are written to the specified color palette address stored in the Pixel Address register. Finally, the Pixel Address register is automatically incremented.

It is possible to read the color definitions stored in the DAC's color palette. After setting RS₀ and RS₁ equal to 1, the desired color palette address is stored in the Pixel Address register. The color definition (18-bits) in the desired color palette location is then automatically transferred to the Color Value register and the Pixel Address is auto-incremented. With successive read cycles, the color definitions pointed to by the incremented address are transferred to the color value register. Refer to *Figure 13*.

The **Pixel Mask** register is a byte-wide latch. by setting RS₀ = 0 and RS₁ = 1, the Pixel Mask register can be accessed by the microprocessor interface, D₀–D₇. This register is used to mask selected bits of the pixel address values applied to the Pixel Address inputs (P₀–P₇). A "1" in any location in the Pixel Mask register leaves the corresponding bit in the pixel address unchanged. A "0" will reset the corresponding bit to zero. The operation of the Pixel Mask register does not affect the address of the color definition when the microprocessor accesses the color palette. The masking operation makes it possible to alter the displayed colors without altering the contents of external video memory or the DAC0630/631's color palette.

WRITING TO THE COLOR PALETTE

A new color definition can be stored in the color palette by first specifying the initial address while in **write** mode (RS₀ = RS₁ = \overline{WR} = 0). This address is stored in the Pixel Address register. The initial address is followed by the red, green and blue color definition data (RS₀ = 1, RS₁ = \overline{WR} = 0). These three six-bit values are collected together in the Color Value register for a total of 18 bits. The internal logic then transfers this new color definition to the location pointed to by the address stored in the Pixel Address register. As soon as this transfer is completed, the Pixel Address register is auto-incremented. This allows consecutive color palette locations to be updated without the microprocessor specifying each address. All that is necessary is to continue supplying the red, green and blue data for each consecutive address. Refer to *Figures 11 and 12*.

Attempting to update the color palette when \overline{BLANK} is not asserted results in the data from the Color Value register taking precedence over the DAC0630 and DAC0631's bit mapping operation. The output of the three 6-bit DACs will be based on the color definition from the memory location specified by the pixel address register and not the address found on P₀–P₇. This conflict results in the DAC's generating unexpected output levels. This can last as long as two PCLK periods.

READING FROM THE COLOR PALETTE

To read a location in the color palette an address is sent on the Data I/O lines (D₀–D₇) while in read mode (RS₀ = RS₁ = 1, \overline{WR} = 0) and stored in the Pixel Address register. The color definition in the specified color palette location is then transferred to the Color Value register and the Pixel Address register is auto-incremented. The color definition can now be retrieved with three sequential read operations (RS₀ = 1, RS₁ = \overline{RD} = 0). The first byte placed on the Data I/O lines contains the red value. The next is green, and the last is blue. The two most significant bits are set to zero in each case. Once again, the Pixel Address register is auto-incremented, and consecutive color palette locations can be read simply by specifying the beginning address and reading the color palette one or more times. Refer to *Figures 10, 13 and 14*.

Functional Description (Continued)

If the Pixel address register is ever updated during a read or write operation, the current data sequence is terminated and a new read or write operation is initialized.

VIDEO PATH

The video path consists of the Pixel Latch and Mask (inputs P_0 – P_7), color palette (256 x 18-bit wide RAM), 18-bit wide bus, and an 18-bit wide latch on the inputs of the three 6-bit high-speed video DACs. The video path uses a three clock cycle (P_{CLK}) pipeline for the pixel address and BLANK inputs. These signals are latched on the rising edge of P_{CLK} .

At each rising edge of P_{CLK} , the Color Palette address applied to P_0 – P_7 is stored in the Pixel Latch and defines a location in the Color Palette. The color definition in that location is then transferred to the three 6-bit DAC input latches.

ANALOG OUTPUTS

The analog outputs are designed to drive 75Ω loads with I_{REF} set to 4.44 mA or 37.5Ω loads with I_{REF} set to 8.88 mA. For both loads the peak-white amplitude is 0.7V.

The analog outputs can be set to zero by using the BLANK input. This is an active low signal that forces the analog outputs to ground by placing all zeros on the DACs' inputs. The color definition selected by the pixel address is ignored.

The DAC0630/631's DACs use switched current sources that are summed together, thus generating the output current. Each 6-bit DAC consists of 63 current sources, each of which has a magnitude of $I_{REF}/30$. The digital input code determines the number of current sources that are active and contributing to the total output current. This output current, in conjunction with a termination resistance connected between each DAC output and ground, sets the full-scale magnitude of the output voltage as determined by

$$V_{PEAK\ WHITE} = 2.1(I_{REF})R_L \\ V_{BLACK\ LEVEL} = 0V$$

Application Hints

POWER SUPPLY

The DAC0630 and DAC0631 draw large transient currents from the power supply. To ensure proper operation it is necessary to utilize standard high frequency board layout and power supply distribution techniques.

The transient currents drawn by the DAC0630 and DAC0631 dictate that the ac impedance at the supply pins must be kept to a minimum. This is accomplished by using the recommended decoupling capacitors, C1 and C2, as shown in Figure 15. These capacitors must have leads that are as short as possible. High frequency decoupling is accomplished with a 0.1 μF chip capacitor, C1. A bead tantalum, between 10 μF to 47 μF, should be used for C2.

Differential ground noise can be created when a voltage difference appears between pin 14 and the ground of the digital devices driving the DAC0630 or DAC0631. This voltage difference is caused by series impedance in the ground path and the current transients drawn by the DAC0630 or DAC0631. The differential ground noise can be minimized by using large, low inductance ground paths between the digital devices that drive the DAC0630 or DAC0631 and pin 14. Therefore, a ground plane layout is recommended.

ANALOG OUTPUT—LINE DRIVING

The connection between the DAC's outputs and the RGB inputs of the video monitor it is driving should be viewed as a transmission line. Impedance changes along this line will result in the reflection of part of the video signal back to the DAC's outputs. These reflections may result in a degradation of the picture quality displayed on the monitor.

To ensure good signal fidelity, RF techniques should be observed. Any traces connecting the DAC0630 or DAC0631 to an on-board connector should form a transmission line of 75Ω impedance. However, the need to ensure that the connecting traces form a transmission line can be eliminated by placing the DAC's output termination resistors at the output connector instead of the DAC's output pins.

The coaxial cable that connects the DAC's outputs to a video monitor should have a characteristic impedance of 75Ω. Connectors on the coaxial line can cause impedance change. Any connectors used with the coaxial cable should match its characteristic impedance.

There are four different methods of terminating the DAC outputs:

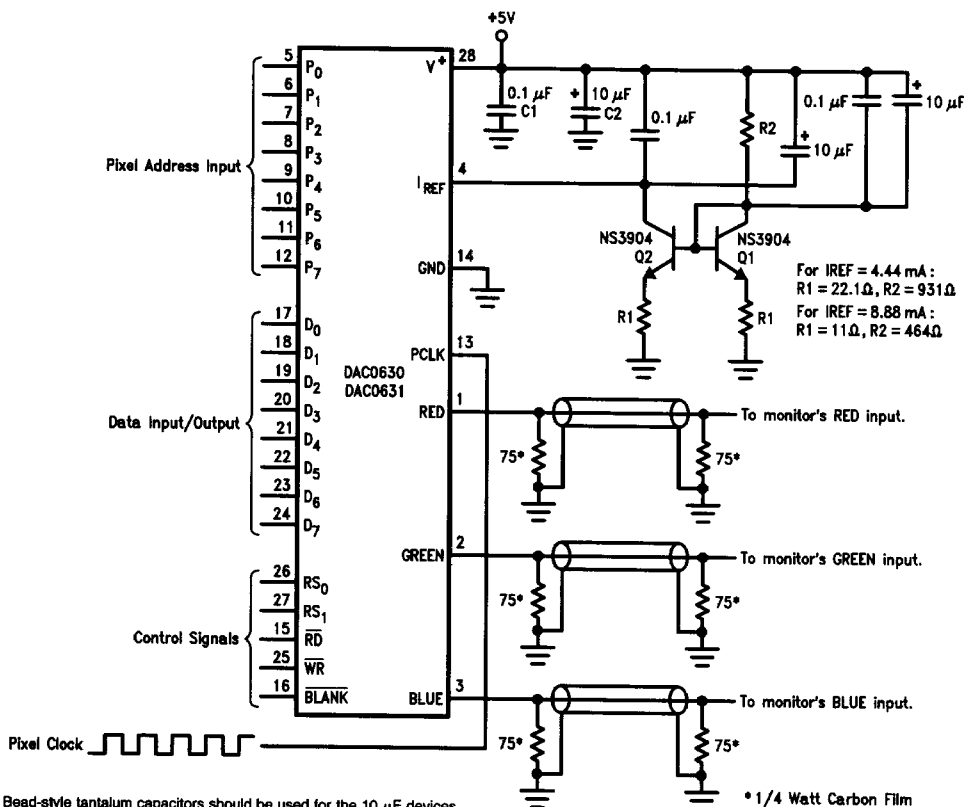
- 1) Single termination at the DAC (75Ω)
- 2) Single termination at the destination (75Ω)
- 3) Double termination (37.5Ω)
- 4) Buffered signal

1) Single termination at the source involves placing a single termination resistor at each DAC output of the DAC0630 and DAC0631 (or at the connector, as described above). No other terminating load is present. Therefore, a high-input impedance monitor should be used. The ac load driven by the DAC's outputs is the transmission line impedance in parallel with the load resistor. The transmission line's impedance should match the impedance of the load resistor. Thus, the DAC's output has an initial signal amplitude that is half the dc value expected. This half-amplitude signal is 100% reflected by the open circuit presented by the monitor input. This restores the signal amplitude to the expected value. The reflections from the monitor propagate back towards the DAC outputs. The load resistor at each DAC output presents a correctly terminated transmission line so no further reflections occur. This arrangement is relatively tolerant to mismatches in the transmission line between the DAC and the monitor because no reflections occur at the DAC end of the transmission line. However, multiple monitors should not be connected in parallel despite each monitor's high input impedance.

2) Single termination at the destination has the termination impedance at the input of the monitor acting as both the load resistor for the DAC and the termination impedance of the cable (transmission line). If the connection between the DAC0630/631 is correctly terminated there will be no reflections. However, if there are any line impedance variations along the cable, reflections will occur and create "ghost images" on the display. This occurs because there is a reflection from the point where the mismatch occurs back to the DAC's output. The signal then reflects off the DAC's output back toward the monitor. It arrives with a significant time delay following the original signal, and "ghosting" results.

3) Double termination of the DAC outputs allow each end of the transmission line to be correctly matched. This results in the least amount of reflection and the highest signal and display fidelity. This termination method also allows for the

Application Hints (Continued)



Note: Bead-style tantalum capacitors should be used for the $10 \mu\text{F}$ devices. Thermally connect the NPN transistors together with a Wakefield 259 series Equalizing Link.

FIGURE 15. Typical Connection Showing I_{REF} Generator and Double Termination

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fastest fall time. The DAC termination's RC time constant sets the outputs' fall time. The greater the time constant, the slower the fall time. Therefore, the fall time will be minimized since the impedance using this termination technique is less than that achieved with single termination. With double-termination it is necessary to increase I_{REF} to 8.88 mA to ensure a full-scale output voltage of 700 mV.

4) By placing a buffer at the DAC's output, the DAC0630 and DAC0631 will be able to drive large capacitive loads such as long lossy cables. The buffer requires a high input impedance, a condition that is satisfied with LM1203 RGB Video Amplifier System. A 75Ω load is placed at the buffer's input. The buffer's low output impedance should be matched to the interconnecting cable with a series resistor. The cable should then be terminated with the same resistance at the monitor.

ANALOG OUTPUT—PROTECTION

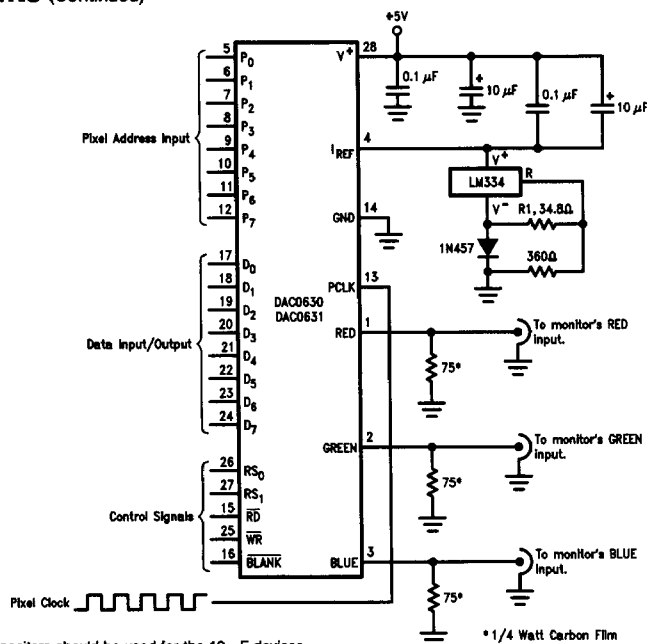
The DAC0630 and DAC0631 have on-chip electrostatic discharge (ESD) protection on each pin. However, the same precautions should be taken as with any other CMOS integrated circuit during manufacturing to reduce the possibility of ESD damage.

GENERATING I_{REF}

An active current source for I_{REF} is recommended to ensure that the DACs have predictable and stable output currents. There are numerous methods available to generate the reference current. The voltage drop from V^+ to the I_{REF} pin increases with increasing I_{REF} current. The circuit used to generate I_{REF} must be designed to operate at the minimum voltage ($V_{REFmin} = V^+ - 3V$) expected from the I_{REF} pin to ground. For any application, V_{REFmin} will be smallest when I_{REF} is maximum and supply voltage is minimum. For $I_{REF} = 8.8 \text{ mA}$ and $V^+ = 4.5V$, the I_{REF} generator will have to operate with 1.5V or less across it. I_{REF} generators that require a voltage drop greater than 1.5V may be used if a negative supply is available.

A simple I_{REF} generator circuit is shown with the DAC0630/DAC0631 in Figure 15. As shown, this I_{REF} generator will sink $\approx 4.44 \text{ mA}$ (single termination) with $R1 = 22.1\Omega$ and $R2 = 931\Omega$. For applications that use double termination, $R1 = 11\Omega$ and $R2 = 464\Omega$. The diode connected transistor, Q1, across Q2's base-emitter junction performs a first-order compensation for thermal variations. It is important to keep the lead lengths as short as possible. This will help reduce stray capacitance and the amount of P_{CLK} that is fed into the I_{REF} pin.

Application Hints (Continued)



Note: Bead-style tantalum capacitors should be used for the 10 μF devices.

* 1/4 Watt Carbon Film

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FIGURE 16. Single Termination with LM334 Current Source I_{REF} Generator

Figure 16 shows an alternative method of generating I_{REF} . The LM334 precision current source is used in a temperature compensated configuration. The reference current is set by a single resistor, $R1$, independent of V^+ . The current's value is

$$I_{REF} \approx 160 \text{ mV}/R1$$

DECOUPLING I_{REF}

The magnitude of the current flowing through the internal current sources depends not only on I_{REF} , but also on the voltage at pin 4 relative to V^+ . Therefore, voltage variations between V^+ and the I_{REF} input can result in variations in the DAC's output current. These variations can be greatly attenuated by using a high frequency capacitor in parallel with a larger electrolytic capacitor to couple the I_{REF} input to V^+ .