4-BIT D-TYPE REGISTERS

- THREE-STATE OUTPUTS
- INPUT DISABLED WITHOUT GATING THE CLOCK
- GATED OUTPUT CONTROL LINES FOR ENABLING OR DISABLING THE OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4076B** (extended temperature range) and **HCF 4076B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package, ceramic flat package and plastic micropackage.

The **HCC/HCF 4076B** types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

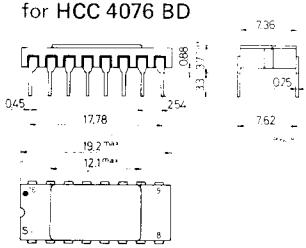
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

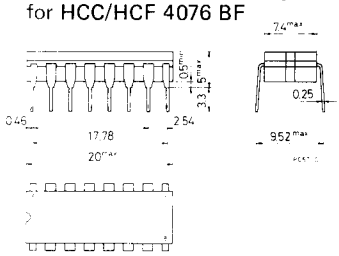
HCC 4076 BD for dual in-line ceramic package
HCC 4076 BF for dual in-line ceramic package, frit seal
HCC 4076 BK for ceramic flat package
HCF 4076 BE for dual in-line plastic package
HCF 4076 BF for dual in-line ceramic package, frit-seal
HCF 4076 BM for plastic micropackage

MECHANICAL DATA (dimensions in mm)

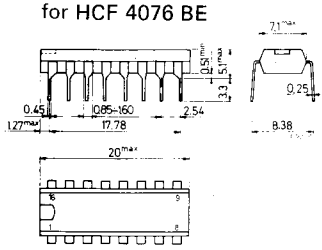
Dual in-line ceramic package for HCC 4076 BD



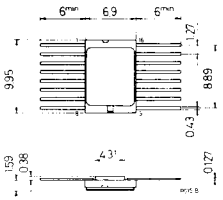
Dual in-line ceramic package for HCC/HCF 4076 BF



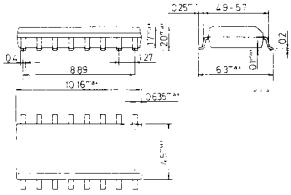
Dual in-line plastic package for HCF 4076 BE



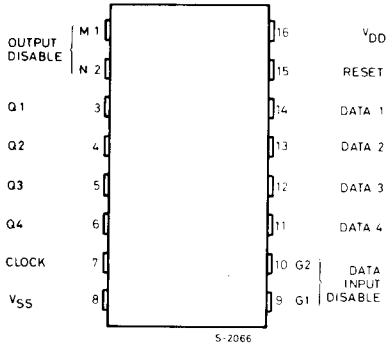
Ceramic flat package for HCC 4076 BK



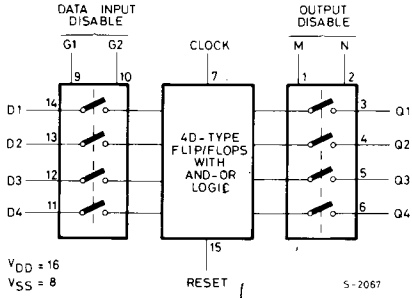
Plastic micropackage for HCF 4076 BM



CONNECTION DIAGRAM



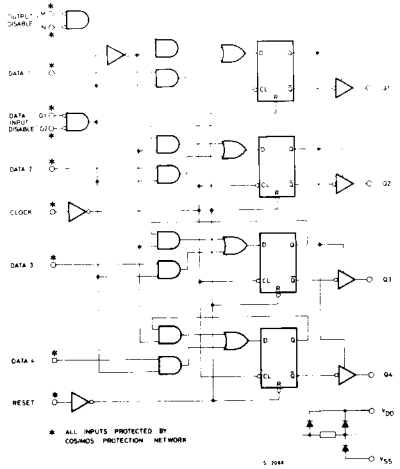
FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC DIAGRAM



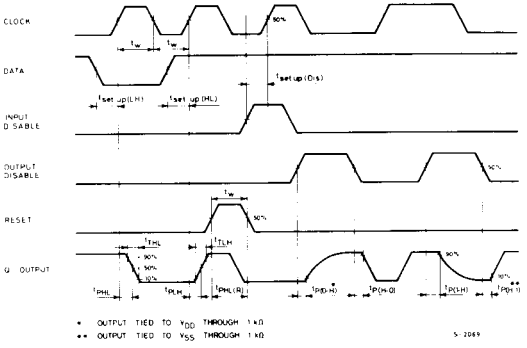
TRUTH TABLE

Reset	Clock	Data Input Disable G1	G2	Data D	Next State Output Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	⌒	1	X	X	Q	NC
0	⌒	X	1	X	Q	NC
0	⌒	0	0	1	1	
0	⌒	0	0	0	0	
0	1	X	X	X	Q	NC
0	⌒	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

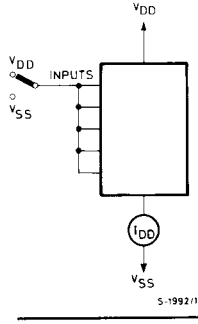
1 ≡ High Level
0 ≡ Low Level
X = Don't Care
NC = No Change

WAVEFORMS

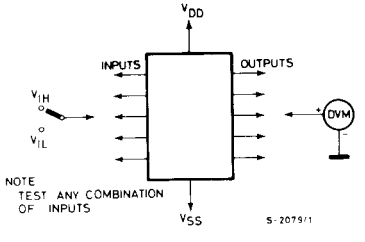


TEST CIRCUITS

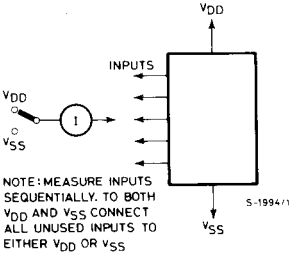
Quiescent device current



Noise immunity



Input leakage current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

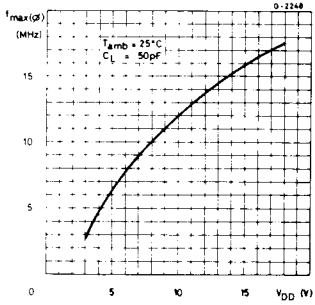
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		± 1	
I_{OH}, I_{OL}	3-state output leakage current	HCC types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
		HCF types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = − 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

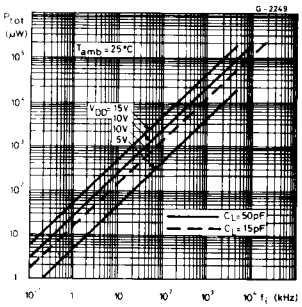
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	V_{DD} (V)	Values Min.	Typ.	Max.	Unit
t_{PLH}, t_{PHL} Propagation delay time (clock to Q output)		5		300	600	ns
		10		125	250	
		15		90	180	
t_{PHL}(R) Propagation delay time (Reset)		5		230	460	ns
		10		100	200	
		15		75	150	
$t_{P(1-H)}$, $t_{P(0-H)}$ 3-state output 1 or 0 to high impedance	R_L = 1 kΩ	5		150	300	ns
		10		75	150	
		15		60	120	
$t_{P(H-1)}$, $t_{P(H-0)}$ 3-state high impedance to 1 or 0 output	R_L = 1 kΩ	5		150	300	ns
		10		75	150	
		15		60	120	
t_{TLH}, t_{THL} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	
t_W Clock pulse width		5	200	100		ns
		10	100	50		
		15	80	40		
t_W Reset pulse width		5	120	60		ns
		10	50	25		
		15	40	20		
t_{setup} Data setup time		5	200	100		ns
		10	80	40		
		15	60	30		
t_{setup} Data input disable setup time		5	180	90		ns
		10	100	50		
		15	70	35		
f_{max} Maximum clock frequency		5	3	6		MHz
		10	6	12		
		15	8	16		
t_r, t_f Clock input rise or fall time		5	15			μs
		10	5			
		15	5			

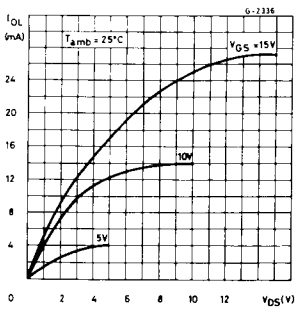
Typical maximum clock input frequency vs. supply voltage



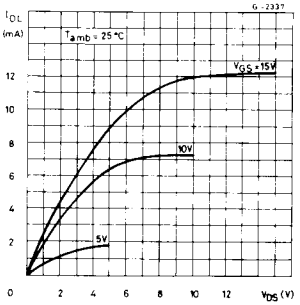
Typical dynamic power dissipation vs. frequency



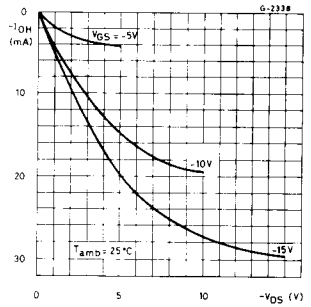
Typical output low (sink) current characteristics



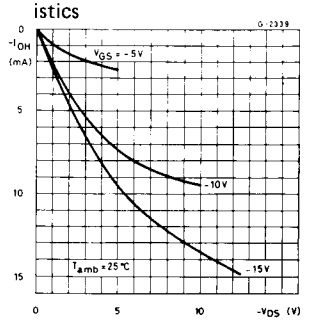
Minimum output low (sink) current characteristics



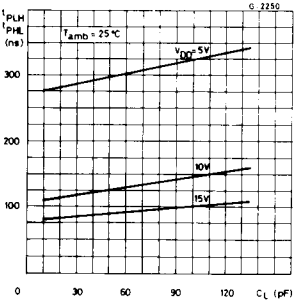
Typical output high (source) current characteristics



Minimum output high (source) current characteristics



Typical propagation delay time vs. load capacitance



Typical transition time vs. load capacitance